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(54) Display controller.

(57) A display controller (10) controls an aspect ratio of an image displayed on a screen of a scanning type display device (12). A horizontal counter (13) counts a clock pulse - (CP) to output column address data for a video RAM (V-RAM) (11), and a vertical counter (14) counts a decoded signal of the column address data to generate row address data for the V-RAM (11). Each time the row address data becomes equal to a predetermined value, a correction circuit (17) prevent the decoded signal from being supplied to the vertical counter (14) for a time interval corresponding to one horizontal scanning line, whereby an additional horizontal scanning line is displayed with the same image data as the horizontal scanning line displayed immediately before. Vertical lines can also be added in the similar manner to control an aspect ratio of the displayed image.

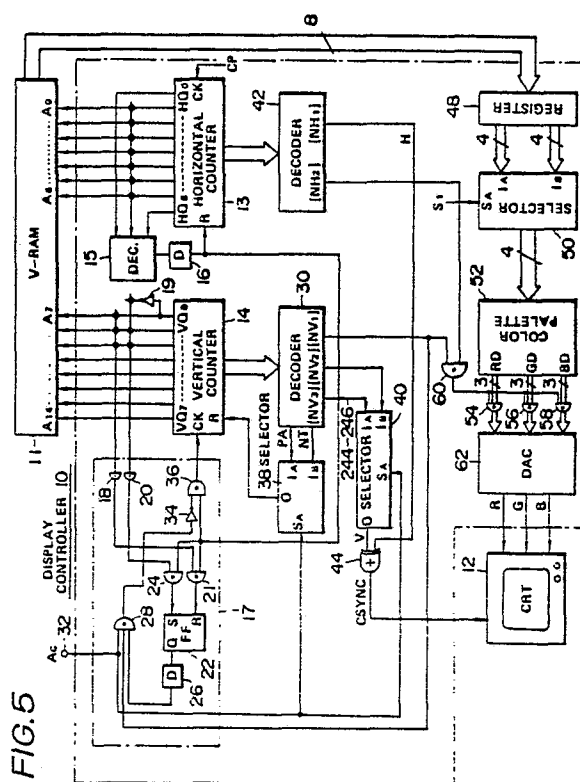


FIG.5

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DISPLAY CONTROLLER

This invention relates generally to a display controller for displaying an image on a screen of a scanning-type display unit such as a CRT display unit, and in particular to such a display controller in which an aspect ratio of the displayed image can be changed.

There has been proposed a display controller adapted to be connected to a central processing unit and a color television set or a display unit to display an image representative of a variety of information. The color television set connected to such a display controller may be one of those manufactured in accordance with NTSC, PAL and SECAM standards. A display of image according to NTSC standard uses 262 or 525 horizontal scanning lines, while a display of image according to either of PAL and SECAM standards uses 313 or 625 horizontal scanning lines.

Conventionally, when an image provided in accordance with NTSC standard need be displayed on a screen of a PAL-type display unit, the NTSC image is converted into a PAL image in such a manner that the number of horizontal scanning lines is simply increased to "625", leaving the width of the image in the horizontal direction unchanged.

However, a display area F_N on the screen provided in accordance with NTSC standard shown in Fig. 1 and a display area on the screen provided in accordance with PAL standard shown in Fig. 2 differ in aspect ratio from each other. More specifically, even if a horizontal width H_N of the NTSC display area F_N is rendered equal to a horizontal width H_P of the PAL display area F_P , a vertical width V_P of the PAL display area F_P is 0.84 times shorter than a vertical width V_N of the NTSC display area F_N . As a result, when an NTSC image is converted into a PAL image in accordance with the aforesaid conversion method, the vertical width of the resultant PAL image is decreased.

For example, when an NTSC image representative of a circle shown in Fig. 3 is converted into a PAL image in the conventional method, an ellipse shown in Fig. 4 is displayed. In Figs. 3 and 4, reference characters P represent intensified dots on the screen.

The reason why the converted image is thus deformed is that the NTSC image and the PAL image differ in aspect ratio from each other. For example, in the case of an NTSC-type display unit having a cathode ray tube of a specific size, the vertical width of a display area containing 190 horizontal scanning lines is 163 mm, while in the case of a PAL-type display unit having a cathode ray tube of the same size as the NTSC-type display unit, the width of a display area containing 190 horizontal scanning lines is 142 mm. Thus, the vertical width of an image displayed on the PAL-type display unit is 0.871 (or 142/163) times shorter than that of an image displayed on the NTSC-type display unit. In other words, the vertical compaction ratio of the image converted from NTSC to PAL is 0.871.

As described above, when an NTSC image containing therein characters is converted into a PAL image in the conventional method, the characters are compacted in the vertical direction, so that the quality of the characters is deteriorated.

The conventional display controller is also disadvantageous in that when an image, of which data is provided for a specific display unit, is displayed on another display unit different in screen size or display characteristic from the specific display unit, the image is liable to be deformed. And in particular, when the image contains characters and when the screen is smaller, the displayed characters are not easy to see because of the small spaces between the characters.

It is therefore an object of the invention to provide a display controller which can change an aspect ratio of an image to be displayed;

It is another object of the invention to provide a display controller which can display an image with little deformation on a display unit of any kind.

According to an aspect of the present invention, there is provided a display controller for use with a scanning-type display device for providing a plurality of display dots on a screen thereof and a memory having a plurality of addresses for storing an array of a plurality of display data each corresponding to a respective one of the display dots, the display controller characterized by the provision of address data generating means for generating address data which varies in synchronization with the scanning of the screen, the generated address data being supplied to the memory to sequentially read the plurality of display data; address detection means for detecting a coincidence of the generated address data with a predetermined value to output a detection signal; and correction circuit means responsive to the detection signal for causing the address generating means to keep at least part of the generated address data unchanged to display predetermined ones of the plurality of display dots in accordance with the same display data. The display controller may further comprise receiving means for receiving a certain control signal, and wherein the address detection means is enabled to output the detection signal only when the certain control signal is received by the receiving means.

The invention will be described in detail below with reference to drawings which illustrate only specific embodiments, in which:-

Fig. 1 is an illustration showing a display area provided in accordance with NTSC standard;

Fig. 2 is an illustration showing a display area provided in accordance with PAL standard;

Fig. 3 is an illustration showing an image displayed in accordance with NTSC standard;

Fig. 4 is an illustration showing the same image as that shown in Fig. 3 displayed in accordance with PAL standard;

Fig. 5 is a block diagram of a display controller 10 provided in accordance with a first embodiment of the present invention;

Fig. 6 is a timing chart of the various signals appearing in the display controller 10 of Fig. 5;

Fig. 7 is an illustration showing a display area on a screen of the display unit 12 shown in Fig. 5;

Fig. 8 is an illustration showing horizontal scanning lines additionally provided on the screen every eight horizontal scanning lines;

Fig. 9 is an illustration showing an image converted from NTSC to PAL by the display controller 10 of Fig. 5;

Fig. 10 is an illustration showing dot-matrix character patterns before conversion;

Fig. 11 is an illustration showing the dot-matrix character

patterns after conversion by the display controller 10;

Fig. 12 is a block diagram of a display controller 10a provided in accordance with a second embodiment of the present invention; and

Fig. 13 is an illustration showing the dot-matrix character patterns after conversion by the display controller 10a.

A display controller provided in accordance with a first embodiment of the invention will now be described.

Referring now to Fig. 5, the display controller 10 is connected to a video memory (hereinafter referred to as "V-RAM") 11 and a CRT display unit 12 of a PAL-type. The V-RAM 11 is written, by an external control unit such as a central processing unit (not shown), with image data provided in accordance with NTSC standard and representative of, for example, characters or graphic image.

The image data are sequentially read from the V-RAM 11 on an eight-bit basis in accordance with seven-bit column or horizontal address data A_0 to A_6 and eight-bit row or vertical address data A_7 to A_{14} . The column address data A_0 to A_6 and the row address data A_7 to A_{14} are generated by a horizontal counter 13 and a vertical counter 14, respectively. The horizontal counter 13 is arranged so as to have a count range of between "0" and "341" (decimal) and the vertical counter 14 is arranged so as to selectively have a count range of between "0" and "261" (decimal) and a count range of between "0" and "312".

The horizontal counter 13 counts clock pulses CP applied to a clock terminal CK thereof, of which period corresponds to a time interval required to display each of dots constituting an image on the display unit 12, to output a nine-bit count output HQ_0 to HQ_8 . The seven bits HQ_1 to HQ_7 , of the count output of the horizontal counter 13 are supplied to the V-RAM 11 as the column address data A_0 to A_6 , and an eight-bit count output VQ_0 to VQ_7 , of the vertical counter 14 is supplied to the V-RAM 11 as the row address data A_7 to A_{14} .

All the bits HQ_0 to HQ_8 of the count output of the horizontal counter 13 are supplied to a decoder 15 which outputs a "1" signal to a delay circuit 16 when the supplied count output is equal to "340" in decimal, that is to say, one clock pulse CP before the horizontal counter 13 outputs the final count output equal to "341". The "1" signal outputted from the decoder 15 is delayed at the delay circuit 16 by a time interval equal to one cycle of the clock pulse CP, and thence supplied to a reset terminal R of the horizontal counter 13 and to a correction circuit 17.

The correction circuit 17 is arranged such that an additional horizontal scanning lines are provided on the screen of the display unit 12 at a predetermined interval in the vertical direction and that an appropriate portion of the image data is read from the V-RAM 11 for each additional horizontal scanning line.

The correction circuit 17 will now be more fully described.

The lower three bits VQ_0 to VQ_2 of the count output of the vertical counter 14 are supplied to input terminals of a three-input AND gate 18, and the bits VQ_1 and VQ_2 and an inversion of the lowermost bit VQ_0 by an inverter 19 are supplied to input terminals of another three-input AND gate 20. Thus, the AND gate 18 outputs a "1" signal when the lower three bits VQ_0 to VQ_2 are "1", "1" and "1", respectively, and the AND gate 20 outputs a "1" signal when the lower three bits VQ_0 to VQ_2 are "0", "1" and "1", respectively. The output signals of the AND gate 18 and the delay

circuit 16 are supplied to input terminals of a two-input AND gate 21. An output of this AND gate 21 is supplied to a reset terminal R of an RS flip-flop (hereinafter referred to as "FF") 22. Also, the output of the AND gate 20 and the output of the delay circuit 16 are supplied to an AND gate 24 to form a logical product thereof which is supplied to a set terminal S of the FF 22. A non-inverted output Q of the FF 22 is delayed at a delay circuit 26 by a time interval equal to one cycle of the clock pulse CP and thence supplied to a first input terminal of a three-input AND gate 28. Second and third input terminals of the AND gate 28 are supplied respectively with an output signal NV_1 of a decoder 30, which decodes the count output VQ_0 to VQ_7 of the vertical counter 14, and an aspect ratio selection signal Ac applied to a control input terminal 32 of this display controller 10. The signal NV_1 is rendered "1" when the value of the count output of the vertical counter 14 is between "0" and "191", that is to say, when the actual display area on the screen is scanned. A logical product of the output of the delay circuit 26 and the signals NV_1 and Ac formed by the AND gate 28 is inverted by an inverter 34, and thence supplied together with the output of the delay circuit 16 to input terminals of an AND gate 36. An output of this AND gate 36 is supplied to a clock input terminal CK of the vertical counter 14.

The decoder 30 is arranged so as to output to input terminals I_A and I_B of a selector 38 two change-over signals PA and NT which correspond respectively to PAL and NTSC standards. The signal PA is rendered "1" when the count output of the vertical counter 14 represents "288" in decimal, while the signal NT is rendered "1" when "261". The selector 38 outputs the change-over signal PA when the signal Sa in the state of "1" is supplied to a selection terminal S_A thereof, and outputs the change-over signal NT when the signal Sa is in the state of "0".

The decoder 30 also outputs a signal NV_2 , which corresponds to NTSC standard and is rendered "1" when the value of the count output of the vertical counter 14 is between "219" and "221" in decimal, and a signal NV_3 , which corresponds to PAL standard and is rendered "1" when the value of the count output of the vertical counter 14 is between "244" and "246". The signals NV_2 and NV_3 outputted from the decoder 30 are supplied to input terminals I_B and I_A of a selector 40. The selector 40 outputs the signal NV_3 as a vertical synchronization signal V when the signal Ac is in a "1" state, and outputs the signal NV_2 as the vertical synchronization signal V when the signal Ac is in a "0" state. On the other hand, the count output of the horizontal counter 13 is decoded by a decoder 42 which outputs a signal NH, for use as a horizontal synchronization signal H when the count output is between "277" and "301", and outputs a signal NH_2 when the count output is between "0" and "255". The vertical synchronization signal V is combined by an exclusive-OR (EXOR) gate 44 with the horizontal synchronization signal H to form a composite synchronization signal CSYNC which is supplied to the CRT display unit 12.

On the other hand, each eight-bit image data, which contains two color codes, read from the video memory 11 is loaded into a register 48. Upper half (four bits) of the loaded image data (or one of the two color codes) is supplied to an input terminal I_A of a selector 50, and lower half thereof (the other of the two color codes) is supplied to another input terminal I_B of the selector 50. The selector 50 alternately outputs the two color codes in accordance with a signal S1 produced based on the bit HQ_0 . Each of the color codes thus outputted from the selector 50 is supplied to a color palette 52 which in turn generates therefrom three

color data RD, GD and BD representative of intensity levels of red, green and blue, respectively. The color data RD, GD and BD, each composed of three bits, are supplied respectively to gate circuits 54, 56 and 58 which open when a logical product of the signals NH_2 and NV, formed by an AND gate 60 is "1". The color data RD, GD and BD passed respectively through the gate circuits 54, 56 and 58 are supplied to a digital-to-analog converter (hereinafter referred to as "DAC") 62. The DAC 62 converts the color data RD, GD and BD into corresponding analog color signals R, G and B which are supplied to the CRT display unit 12.

The operation of the display controller 10 will now be described with reference to Fig. 6.

Description will be first given as to the case where the signal Ac is set to "1" to convert an NTSC image into a PAL image.

Fig. 6-(A) represents a display period of a portion of the image on the screen which is composed of four consecutive horizontal lines scanned during the time when the least significant three bits of the count output of the vertical counter 14 vary from "6" to "0", and Figs. 6-(B) to 6-(K) show waveforms of various signals of the display controller 10 in the display period. In order to simplify the description given below, it is assumed that the seventh horizontal line on the screen is scanned when the least significant three bits represent "6", the eighth horizontal line is scanned when "7" and so on.

When the count output HQ_n to HQ_0 applied to the decoder 15 becomes equal to "340", which is one count less than the last count "341", the decoder 15 outputs a "1" signal as shown in Fig. 6-(B). The "1" signal is delayed by one clock time at the delay circuit 16, as shown in Fig. 6-(C), and supplied to the AND gates 21 and 24.

If the least significant three bits of the count output of the vertical counter 14 represent "6", that is to say, if the horizontal line presently scanned is the seventh horizontal line, the AND gate 20 outputs a "1" signal. And therefore, when the delay circuit 16 outputs the delayed "1" signal corresponding to the count output "340" of the horizontal counter 13, the AND gates 24 outputs a "1" signal to the set terminal S of the FF 22 (Fig. 6-(F)). As a result, the FF 22 is brought into a set state, whereby the non-inverted output Q thereof is rendered "1", as shown in Fig. 6-(G). The non-inverted output Q of the FF 22 is delayed at the delay circuit 26 by one clock time, as shown in Fig. 6-(H), and supplied to the first input terminal of the AND gate 28. When the delay circuit 16 outputs the delayed "1" signal corresponding to the count output "340" of the horizontal counter 13, the count output of the horizontal counter 13 is incremented to "341" at a trailing edge thereof. Also, when the output signal of the delay circuit 16 rises to "1", the output of the delay circuit 26 has been in the state of "0" - (Fig. 6-(H)), and therefore the AND gate 36 outputs a "1" signal to the clock terminal CK of the vertical counter 14, as shown in Fig. 6-(K). When the "1" signal outputted from the AND gate falls from "1" to "0" (Fig. 6-(K)), the count output of the vertical counter 14 or the row address of the

V-RAM 11 is incremented by one. As a result, the least significant three bits of the count output of the vertical counter 14 become equal to "7" (Fig. 6-(A)), and also the AND gate 18 opens to enable the AND gate 21 to open, as shown in Fig. 6-(E). Thus, the next horizontal line, which is the eighth horizontal line begins to be scanned.

When the AND gate 28 is supplied at the first input terminal thereof with the "1" signal outputted from the delay circuit 26, the AND gate 28 outputs a "1" signal, since the signal Ac is in the "1" state, as described above, and the signal NV, is "1" in the actual display period. The "1" signal outputted from the AND gate 28 is inverted by the inverter 34 and supplied to the AND gate 36 to disable the AND gate 36.

When the value of the count output of the horizontal counter 13 again becomes equal to "340" during the scanning of the eighth horizontal line (Fig. 6-(B)), the delay circuit 16 outputs a "1" signal, so that the AND gate 21 opens to reset the FF 22, as shown in Fig. 6-(G). In the normal condition, the "1" signal outputted from the delay circuit 16 is supplied to the clock terminal CK of the vertical counter 14 through the AND gate 36. However, the AND gate 36 is closed at present as described above, so that the "1" signal outputted from the delay circuit 16 is prevented from being supplied to the vertical counter 14. As a result, the count output of the vertical counter 14 or the row address of the V-RAM 11 remains unchanged. And therefore, during the scanning of the next horizontal scanning line, which is the ninth horizontal line, the same image data as read for the eighth horizontal scanning line will be again sequentially read from the V-RAM 11 in accordance with the count of the clock pulses CP by the horizontal counter 13. The image data thus read from the V-RAM 11 are supplied through the register 48, selector 50, color palette 52 and the DAC 62 to the CRT display unit 12.

When the "1" signal outputted from the delay circuit 16 during the scanning of the eighth horizontal line is supplied to the AND gate 21, the AND gate 21 opens to reset the FF 22. As a result, the non-inverted output Q of the FF 22 is rendered "0", so that the AND gate 28 is closed one clock time later. Thus, the output of the inverter 34 rises to "1" (Fig. 6-(J)).

When the count output of the horizontal counter 13 again becomes equal to "340" to cause the delay circuit 16 to output a "1" signal during the scanning of the ninth horizontal line, the AND gate 36 opens (Fig. 6-(K)) since the output of the inverter 34 is in the state of "1" at this time. And therefore, the vertical counter 14 is triggered to increment the row address of the V-RAM 11 so that the image data for the next horizontal scanning line are read from the V-RAM 11. Thus, one horizontal scanning line is added every eight horizontal scanning lines on the screen.

Table 1 shows the relation between the count output of the vertical counter 14 and the variation of the row address of the V-RAM 11. And, when the least significant three bits of the row address become equal to "1", "1" and "1", the count operation of the vertical counter 14 is interrupted and one horizontal scanning line is added.

60

65

TABLE 1

vertical count output	row address							
	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈	A ₇
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	1
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	1
8	0	0	0	0	1	0	0	0
9	0	0	0	0	1	0	0	1
10	0	0	0	0	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	1	0	0
13	0	0	0	0	1	1	0	1
14	0	0	0	0	1	1	1	0
15	0	0	0	0	1	1	1	1
16	0	0	0	1	0	0	0	0
17	0	0	0	1	0	0	0	1
18	0	0	0	1	0	0	1	0
19	0	0	0	1	0	0	1	1
20	0	0	0	1	0	1	0	0
21	0	0	0	1	0	1	0	1
22	0	0	0	1	0	1	1	0
23	0	0	0	1	0	1	1	1
24	0	0	0	1	1	0	0	0
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
⋮				⋮				

Fig. 7 shows the actual display area BD on the screen of the CRT display unit 12. In Fig. 7, H_1 represents a left-hand horizontal retrace-line period, H_2 a horizontal actual display period, H_3 a right-hand horizontal retrace-line period, H_4 a horizontal synchronization signal period, V_1 an upper vertical retrace-line period, V_2 a vertical actual display period, V_3 a lower vertical retrace-line period, and V_4 a vertical synchronization signal period. The actual display area BD is thus defined by the horizontal actual display period H_2 and the vertical actual display period V_2 , and horizontal scanning lines are added in the actual display area BD at the predetermined positions, for example, next to the eighth horizontal scanning line, next to the sixteenth scanning line and so on, as indicated by broken lines in Fig. 8, wherein solid lines indicate normal horizontal scanning lines.

Thus, when the display controller 10 operates with the V-RAM 11 storing image data representative of the circle of Fig. 3 based on NTSC standard, an image close to a circle can be displayed on the screen of the PAL-type CRT display unit 12, as shown in Fig. 9.

If the CRT display unit 12 connected to the display controller 10 is of an NTSC type, the signal Ac is held in the "0" state. In this case, the selector 38 outputs the signal NT to the vertical counter 14, so that the maximum count of the vertical counter 14 becomes equal to "262" in decimal. Also, the signal Ac in the state of "0" closes the AND gate 28, and therefore the count output of the vertical counter 14 is incremented by one each time the count output of the horizontal counter 13 reaches "340" in decimal, so that no addition of horizontal scanning lines is performed. When the signal Ac is "0", the selector 40 outputs the signal NV₂, so that the composite synchronization signal CSYNC produced in this case conforms to NTSC standard.

Thus, according to the above-described embodiment, image data based on NTSC standard can be converted into image data based on PAL standard without the aid of processing by a complicated and troublesome software. With the aforesaid display controller 10, twenty four horizontal scanning lines are added in the actual display area of the screen, so that the bottom portion of the displayed image can be disposed outside of the bottom edge of the screen. However, this can be easily corrected.

The above description was given only as to the conversion of an NTSC display image into a PAL display image, however the above embodiment can be used to add one or more horizontal scanning lines at any desired predetermined positions.

With the above-described embodiment, in the case of displaying 8 x 8 dot-matrix characters such as those ("P", "A" and so on) shown in Fig. 10, the characters can be displayed in an easy-to-see manner by adding one horizontal scanning line to each of those horizontal scanning lines which correspond to the bottom rows of dots of the characters (every eight scanning lines in this case), as shown in Fig. 11. In this case, deterioration of shape of each character can also be prevented.

It should also be noted that the above embodiment can easily be modified so that horizontal scanning lines are added at any desired positions on the screen and that the number of additional scanning lines can be set to any desired value. Thus, by modifying the above embodiment, an image represented by the same data can be displayed on the screen at any desired aspect ratio.

A second embodiment of the invention will now be described.

Referring to Fig. 12, there is shown a display controller 10a which differs from the display controller 10 of Fig. 5 in the following respects.

A horizontal counter 13 is arranged so as to selectively have count ranges of between "0" and "341" and between "0" and "313", while a vertical counter 14 has a count range of between "0" and "261". All bits HQ₀ to HQ₈ of the count output of the horizontal counter 13 are supplied to a decoder 15a which outputs "1" signals when the supplied count output becomes equal to "312" and "340", respectively. The two signals representative respectively of the counts "312" and "340" are supplied to input terminals I_A and I_B of a selector 70. The selector 70 outputs one of the two input signals in accordance with a signal Acc supplied through a terminal 32a to a selection terminal S_A thereof. The output signal from the selector 70 is delayed at a delay circuit 16a by a time interval equal to one cycle of the clock pulses CP, and thence supplied to a reset terminal R of the horizontal counter 13 and a clock terminal CK of the vertical counter 14. Thus, the count range of the horizontal counter 13 is set to "314" when the signal Acc is in the state of "1", while the count range is set to "342" when the signal Acc is in the state of "0".

The count output HQ₀ to HQ₈ of the horizontal counter 13 is also supplied to a decoder 42a which decodes the supplied count output and outputs four signals HN₁, HN₂, HN₃ and HN₄. The signal HN₁ becomes "1" when the count output HQ₀ to HQ₈ is between "0" and "255", and the signal HN₂ becomes "1" when the count output is between "0" and "277". Similarly, the signal HN₃ becomes "1" when the count output HQ₀ to HQ₈ is between "261" and "286", and the signal HN₄ becomes "1" when the count output is between "289" and "314".

The count output VQ₀ to VQ₇ is supplied to a decoder 30a which decodes the supplied count output to produce signals VN₁, VN₂ and VN_m. The signal VN₁ becomes "1" when the count output VQ₀ to VQ₇ is between "0" and "191", and the signal VN₂ becomes "1" when the count output is between "219" and "221". The signal VN_m becomes "1" when the count output VQ₀ to VQ₇ is equal to "262". The signal VN_m is supplied to a reset terminal R of the vertical counter 14, so that the count range of this counter 14 is "264".

The signals HN₁ and HN₂ are supplied respectively to input terminals I_A and I_B of a selector 71. The selector 71 outputs the signal HN₁ when the signal Acc applied to a selection terminal S_A thereof is in the state of "1", and outputs the signal HN₂ when the signal Acc is in the state of "0". The output of the selector 71 is supplied to a first input terminal of an AND gate 60 of which second input terminal is supplied with the signal VN₁. The signals HN₃ and HN₄ are supplied respectively to input terminals I_A and I_B of a selector 72. The selector 72 outputs the signal HN₃ when the signal Acc applied to a selection terminal S_A thereof is in the state of "1", and outputs the signal HN₄ when the signal Acc is in the state of "0". The output from the selector 72 is supplied as a horizontal synchronization signal H to a first input terminal of an EXOR gate 44 whose second input terminal is supplied with the signal VH₂ or a vertical synchronization signal V. The output of the EXOR gate 44 is supplied to a CRT display unit 12a as a composite synchronization signal CSYNC.

The bits HQ₁ and HQ₂ of the count output of the horizontal counter 13 and an inversion of the least significant bit HQ₀ by an inverter 19a are supplied to input terminals of an AND gate 73 provided in a correction circuit 74. When the bits HQ₂, HQ₁ and HQ₀ are "1", "1" and "0", respectively, the AND gate 73 outputs a "1" signal

which is delayed at a delay circuit 74 by a time interval equal to one clock cycle of the clock pulses CP. The signal outputted from the delay circuit 74 is supplied to a first input terminal of a three-input AND gate 75 whose second and third input terminals are supplied respectively with the output signal of the selector 71 and the signal Acc. An output of the AND gate 75 is inverted by an inverter 76 and thence supplied to a first input terminal of an AND gate 77 whose second input terminal is supplied with the clock pulses CP.

A selector 50 is supplied at a selection terminal S_A thereof with a selection signal S_2 , and selectively outputs two color codes fed from a register 48 in accordance with the selection signal S_2 . The selection signal S_2 is derived from, for example, the output of the inverter 19a.

The operation of the display controller 10a will now be described.

It is assumed that the signal Acc is now in the state of "1" in order that additional display dots are provided in each horizontal scanning line at a predetermined interval (every eight display dots, in this case). In the normal condition, the AND gate 73 outputs a "0" signal, and therefore, the AND gate 75 is closed, so that the AND gate 77 is enabled to open. As a result, the horizontal counter 13 is triggered by the clock pulses CP. When the least significant three bits HQ_0 , HQ_1 , and HQ_2 become equal respectively to "0", "1" and "1", that is to say, if the dot currently displayed is one of those dots in a horizontal scanning line which correspond to the seventh dot, fourteenth dot and so on, the AND gate 73 outputs a "1" signal which is supplied to the first input terminal of the AND gate 75 one clock time later. Thus, the AND gate 75 opens to output a "1" signal when the least significant three bits HQ_0 , HQ_1 , and HQ_2 are equal respectively to "1", "1" and "1", that is to say, when one of those dots in a horizontal scanning line which correspond to the eighth dot, sixteenth dot and so on, is displayed. The "1" signal outputted from the AND gate 75 is inverted by the inverter 76 and supplied to the AND gate 77 to close it. And therefore, the clock pulse CP is prevented from being supplied to the clock terminal CK of the vertical counter 13, so that the contents of the vertical counter 13 will not be incremented when one of those dots in a horizontal scanning line which correspond to the eighth dot, sixteenth dot and so on is displayed. Consequently, when the next dot or an additional dot is displayed, the same color codes as those presently stored in the register 48 will be read from the V-RAM 11. And therefore, the additional dot, that is, one of those dots which come next to the eighth dot, sixteenth dot and so on, will be displayed in the same color as the dot presently displayed on the screen. When the additional dot is displayed, the output of the delay circuit 74 is "0", so that the AND gate 77 is enabled to open. And therefore, the horizontal counter 13 is triggered by the clock pulse CP.

When the count output of the horizontal counter 13 reaches "312", the horizontal counter 13 is reset to "0" to display dots on the next horizontal scanning line.

Thus, with this construction, additional display dots are provided in each horizontal scanning line at a predetermined interval, that is, next to the eighth dot, next to the sixteenth dot and so on.

When the signal Acc is held in the "0" state, the AND gate 75 is closed, so that the horizontal counter 13 is triggered each time the clock pulse CP is generated. When the count output of the horizontal counter 13 reaches "340", the selector 70 outputs a "1" signal to reset the horizontal counter 13. Thus, no display dot is added in this case.

With the above-described embodiment, in the case of displaying 8 x 8 dot-matrix characters such as those ("P", "A" and so on) shown in Fig. 10, the characters can be displayed in an easy-to-see manner by providing additional display dots in each horizontal scanning line next to those dots which correspond to the right-hand end dots of the characters (or every eight dots in the horizontal scanning line), as shown in Fig. 13.

It should also be noted that the above embodiment can easily be modified so that display dots are added at any desired positions in each horizontal scanning line and that the number of additional dots can be set to any desired value. Thus, by modifying the above embodiment, an image represented by the same data can be displayed on the screen at any desired aspect ratio.

Claims

1. A display controller for use with a scanning-type display device for providing a plurality of display dots on a screen thereof and a memory having a plurality of addresses for storing an array of a plurality of display data each corresponding to a respective one of the display dots, said display controller characterized by the provision of:

address data generating means for generating address data which varies in synchronization with the scanning of said screen, said generated address data being supplied to the memory to sequentially read said plurality of display data;

address detection means for detecting a coincidence of said generated address data with a predetermined value to output a detection signal; and

correction circuit means responsive to said detection signal for causing said address generating means to keep at least part of said generated address data unchanged to display predetermined ones of said plurality of display dots in accordance with the same display data.

2. A display controller according to claim 1 further comprising receiving means for receiving a certain control signal, and wherein said address detection means is enabled to output said detection signal only when said certain control signal is received by said receiving means.

3. A display controller according to claim 1, wherein said address data generating means comprises a first address generator for generating a lower portion of said address data and a second address generator for generating a higher portion of said address data, said address detection means outputting said detection signal when said lower portion of said address data coincide with said predetermined value, said correction circuit means causing said first address generator to keep said generated lower portion of said address data unchanged so that said predetermined display dots are consecutive.

4. A display controller according to claim 1, wherein said address data generating means comprises a first address

generator for generating a lower portion of said address data and a second address generator for generating a higher portion of said address data, said address detection means outputting said detection signal when said higher portion of said address data coincide with said predetermined value, said correction circuit means causing said second address generator to keep said generated higher portion of said address data unchanged so that said predetermined display dots are displayed every N dots, wherein N is a positive integer.

5. A display controller according to claim 1, wherein said

address data generating means comprises clock generator means for generating a clock signal synchronized with the scanning of said screen, gate circuit means for causing said clock signal to selectively pass therethrough, and counter means for counting said clock signal fed from said gate circuit means to produce a count output as said address data, said gate circuit means preventing said clock signal from passing therethrough in response to said detection signal.

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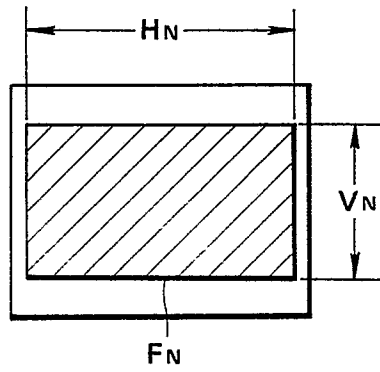
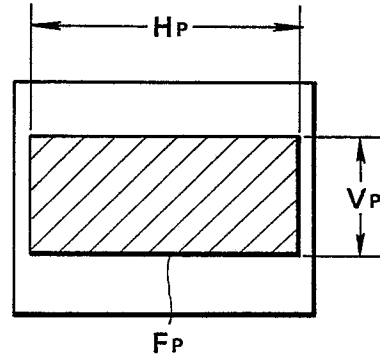
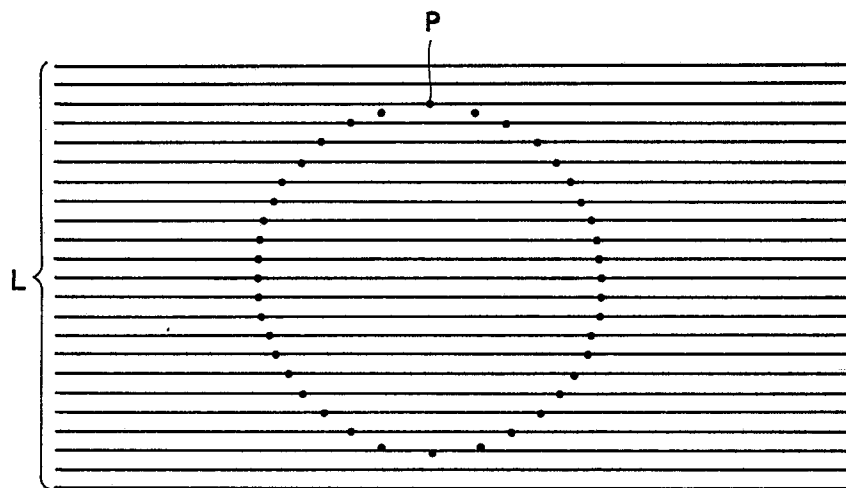
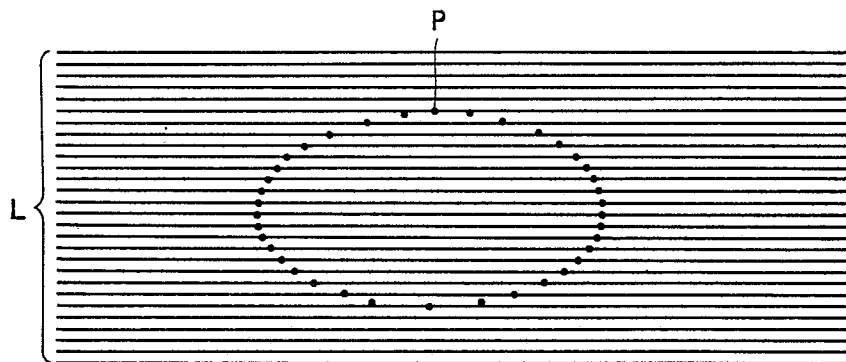
*FIG. 1**FIG. 2**FIG. 3**FIG. 4*

FIG. 5

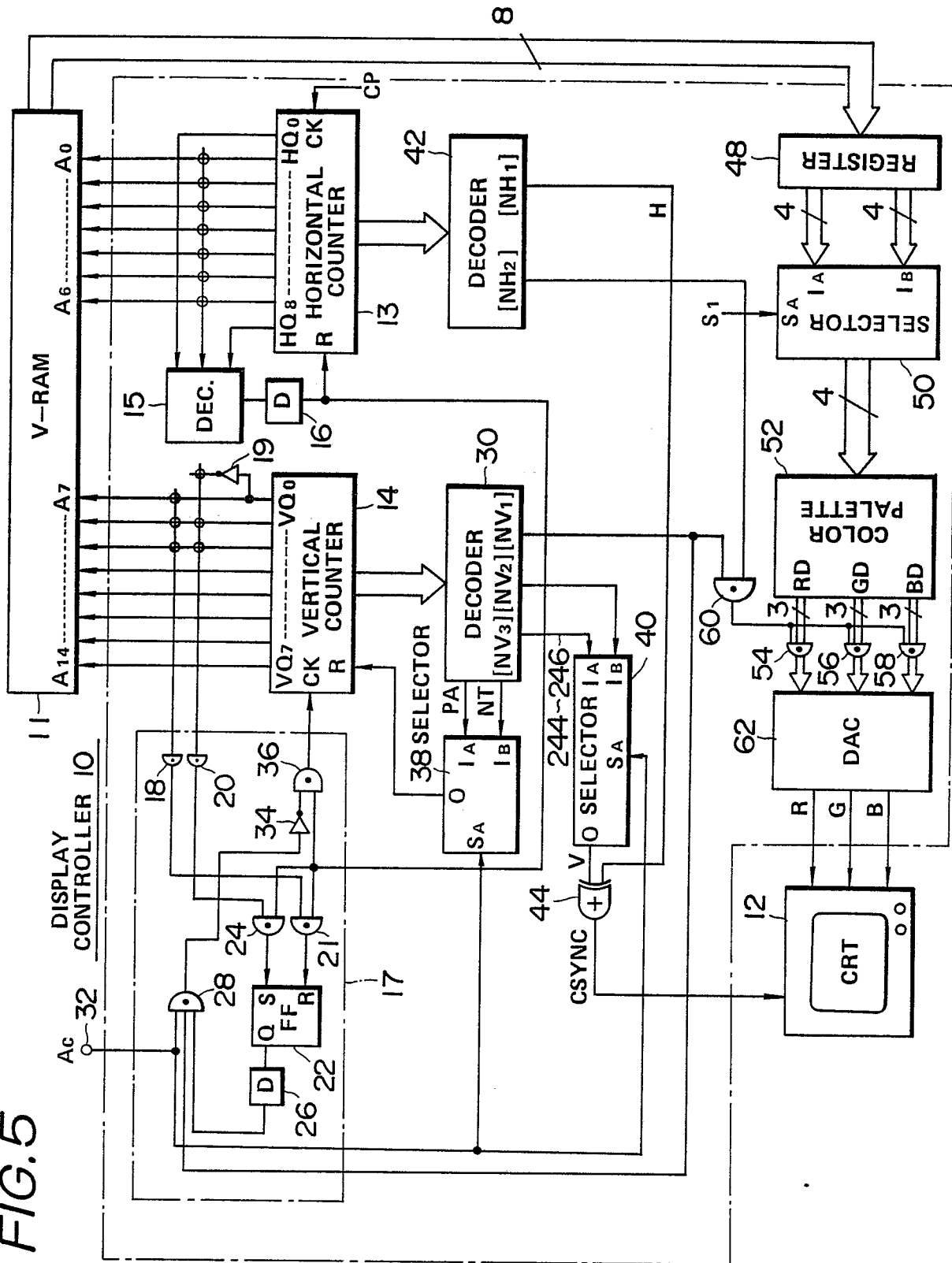
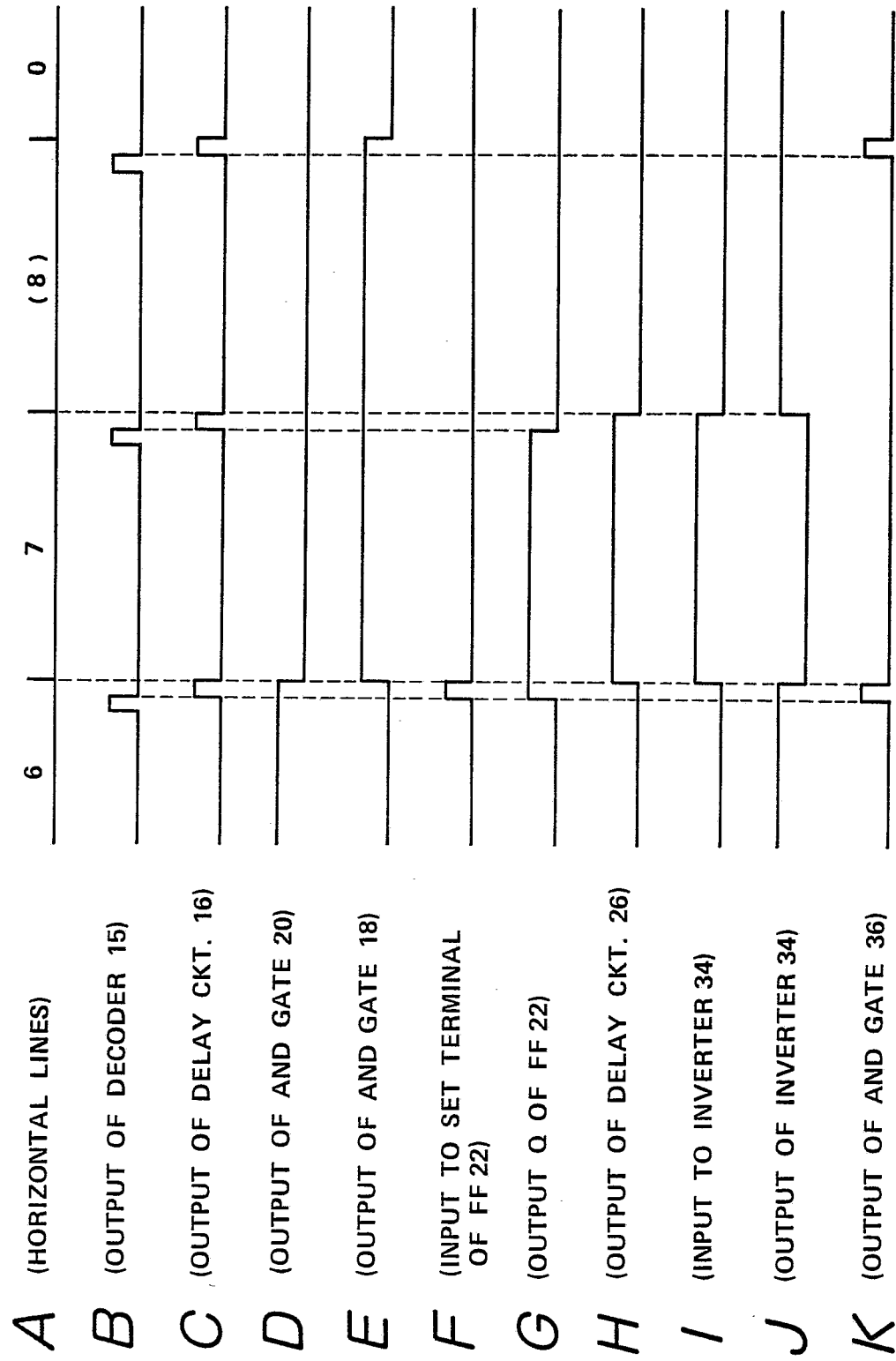
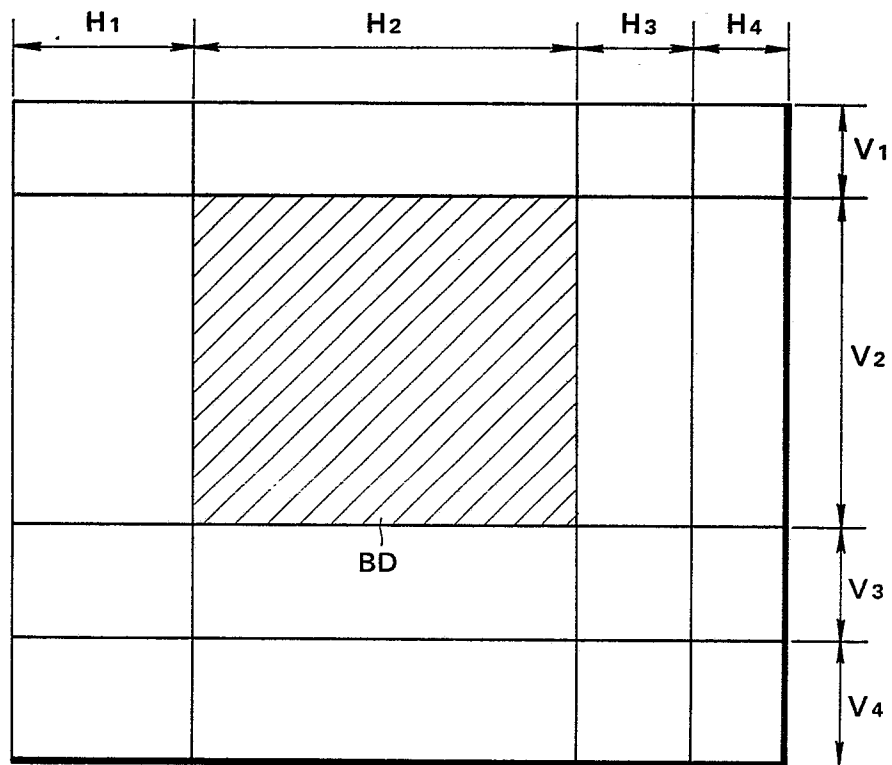




FIG. 6



*FIG. 7*

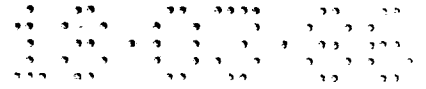
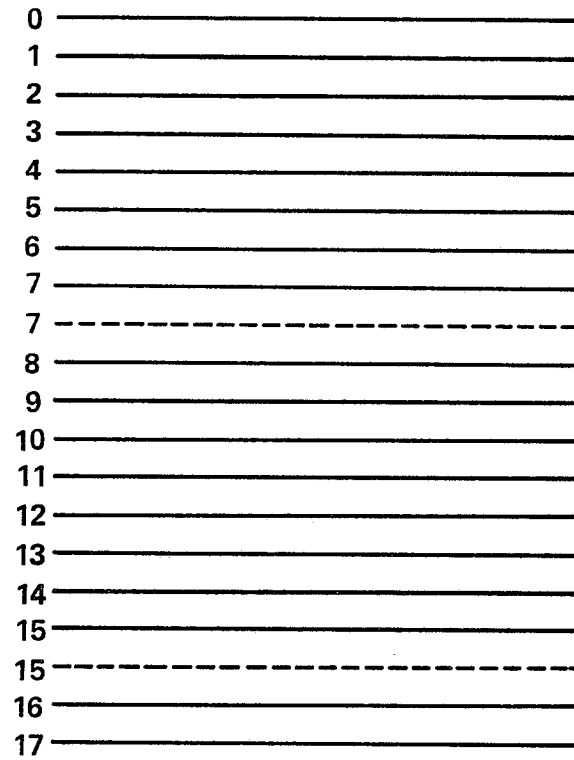
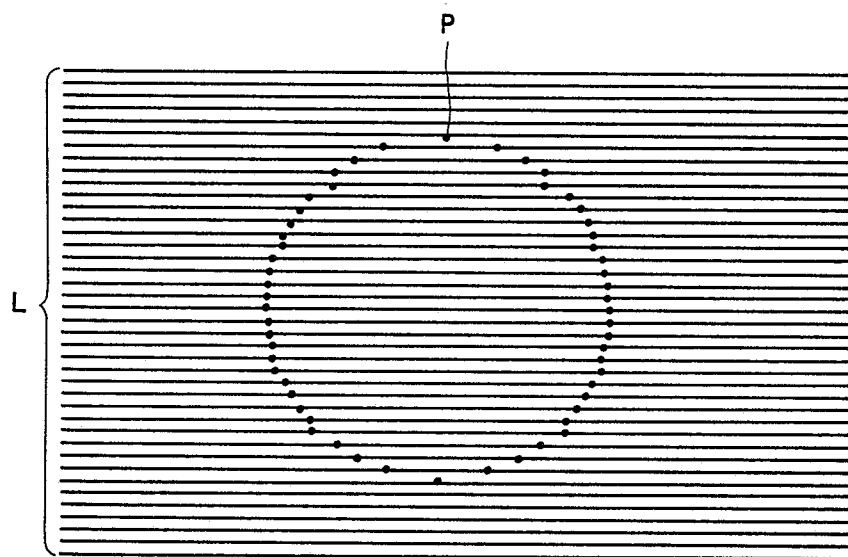
*FIG.8**FIG.9*

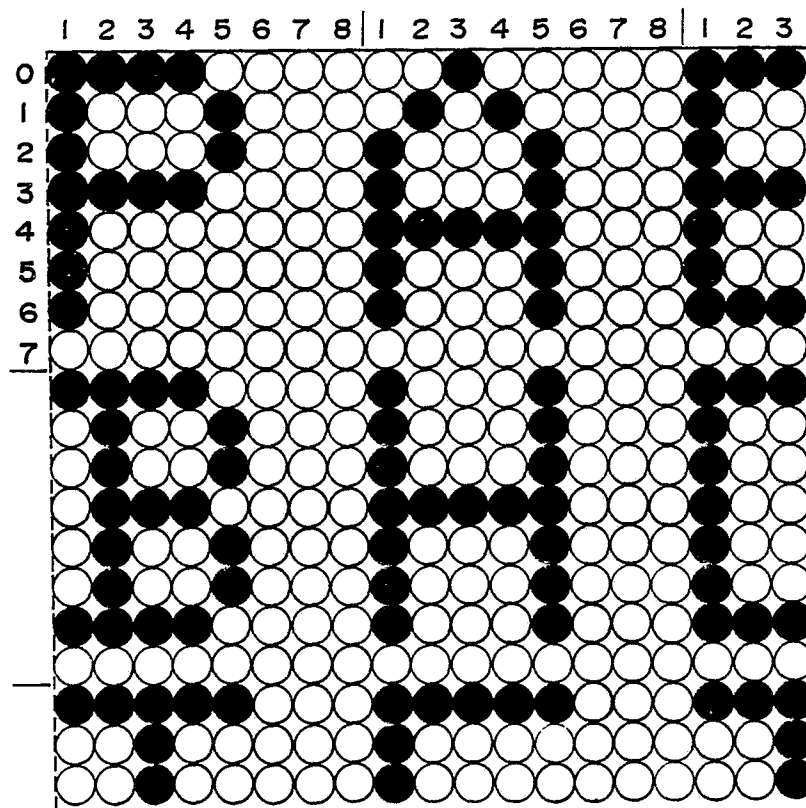
FIG.10

FIG.11

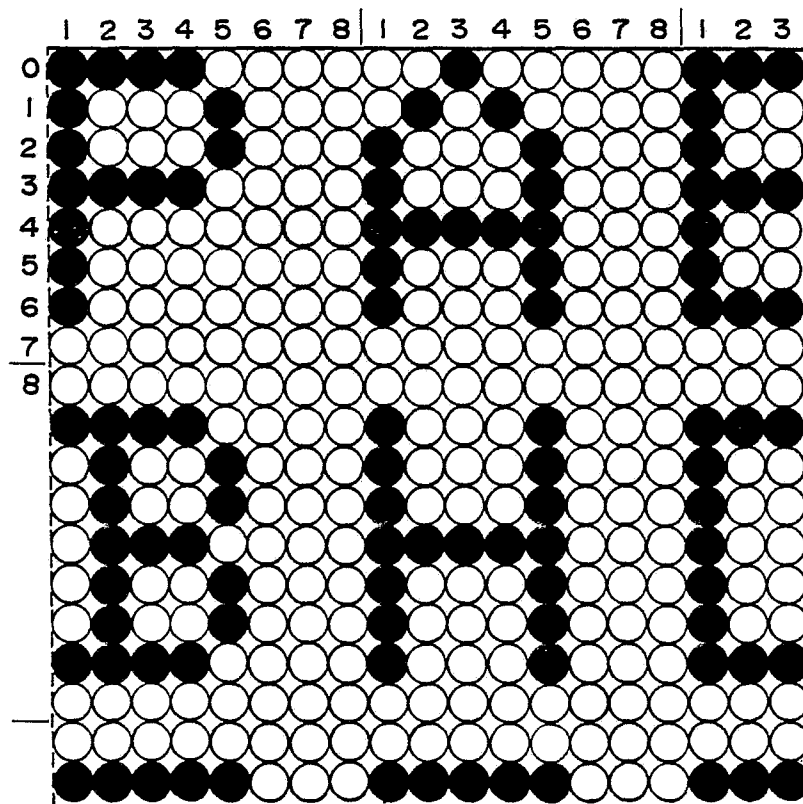


FIG. 12

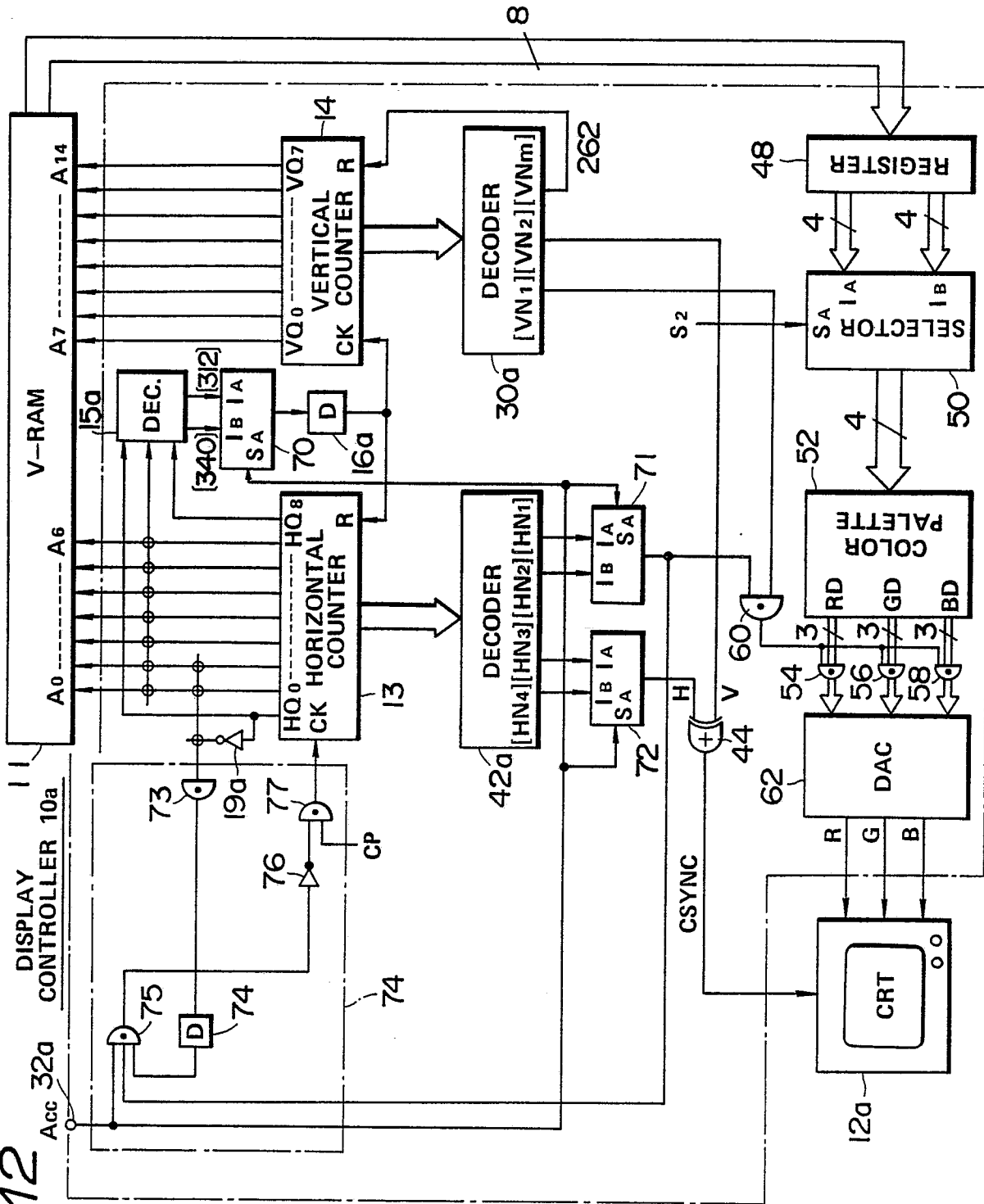


FIG.13

