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(54) Method for displaying picture image data.

(57) A method for displaying a picture image in which pixel data are divide into groups every 2m of the data which are aligned sequentially, the pixel data of each of the divided groups are written into the same numbered addresses of memory elements of 2^m, and read out the 2^m pixel data in parallel, then the data are converted into parallel to series (vice versa) so that order of the data may be restored to the original order thereof. When the pixel data are written in the memory elements, every at least two consecutive addresses sequence of the consecutive 2m pixel data are changed according to accessed addresses and at least every two groups the identical specific numbered pixel data in the groups are controlled so that they may be written in different numbered memory elements with each other. In the case of reading out pixel data from the memory elements, data of 2^m read out of the memory elements of 2m by any consecutive addresses are rearranged according to the writing control in the case of normal display, and in 1/2" reduction display both vertical and horizontal addresses are multiplied by 2ⁿ according to 1/2ⁿ reduction, and the 2^m memory elements are read out basing on different 2" addresses obtained according to writing control.

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METHOD FOR DISPLAYING PICTURE IMAGE DATA

BACKGROUND OF THE INVENTION

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The present invention relates to a picture processing system, particularly to a method for displaying picture image data stored in a picture image memory in the case of displaying the data on monitoring means of display means such as CRT (cathod ray tube), crystal liquid, plasma etc.

In the case of using a picture image processing means, there are many cases in which quantities of information to be processed are larger than the number of pixels, and accordingly, so as to match with such conditions frequently there occur cases in which memory means for displaying the picture images must have sufficient capacities capable of storing the number of pixels of the monitoring means.

For example, in a general case the picture image processing means is adapted that a memory means for displaying having four times of capacity larger than the number of pixels of a monitoring means is provided, and in usual only one fourth of capacity area of the memory means is displayed to perform various processing. Among many kinds of processing there are

some cases in which quantity of information to be processed may be completed only one picture plane of the monitoring means, and in other cases quantities of information to be processed are ranged over the whole picture images.

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In the latter cases, generally, even if addresses are changed, parts of the picture image are sequentially displayed, however, the whole picture image can not be grasped, so that there are some cases in which appropriate processing can not be carried out. In order to avoid the above described inconvenience, it is desired that the picture image in the displaying memory is displayed on a monitoring means in a reduced form so that the picture processing may be promptly and exactly performed and so that the whole picture image may be grasped at a glance.

A simple method for displaying a reproduced picture on a reduced picture image display monitoring means from picture image data stored in a memory means so that, in general, the picture image may be displayed and/or reproduced is to thin out reading addresses from the memory means.

However, in the memory means used for a display of the monitoring means, an access time T of the memory means is longer than a timing t for displaying one pixel (picture element) data on the monitoring means, so that by obtaining an integer N which satisfies t x N \geq T, writing each of data of N pixels being arranged in

time series into the memory means in parallel, reading the data of N pixels in parallel out of the memory means, and assembling them in series according to the original time series within time duration of t x N, the data are supplied to the monitoring means as a usual picture image display.

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In order to obtain a reduced picture image of a half size of that of the original picture as the picture image for the display of the monitoring means, as shown in Fig. 2 by oblique lines, data must be thinned out every other one pixel in the horizontal direction. To carry out the above described thinning out processing two methods have been proposed.

The first one among the methods is a method in which a display memory means which has a short access time is accessed by a half period of usual reading out period, data for 2N pixels are read out in a period, when parallel/serial conversion (hereinafter, refer to P/S conversion) is carried out, unnecessary data are thinned out so that for one period every other data may be those of the pixels of N.

The second method, i.e., the remaining method, is a method in which two display memories which store picture image data into the identical addresses are provided. In the method from one of the memories, for example, a certain address is read out as the LSB (the lowest significant bit) [0] and simultaneously as the next address (for example, an address of the LSB being

"1") the address is read out of the other memory, and unnecessary data are thinned out so that those read out data of 2N pixels may be data of N pixels at P/S conversion time.

However, in the above described the first method, it is required to have a memory element(s) having short access time which results in rising price.

In the second method, it is also necessary to be provided with a plurality of display memory means.

Thus, this second method is very uneconomical. In addition, to obtain a reduced picture image of one fourth of the original picture or that of one eighth of the original picture is less economical than obtaining a reduced picture image to a half size of the original picture.

SUMMARY OF THE INVENTION

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It is main object of the present invention to obtain a picture image of reduced size faithful to the original picture on the display of the monitoring means without requiring may memory element(s) having short access time and any extra memory means for displaying, in other words the object of the present invention is to obtain a picture image of reduced size which is faithful to the original picture by using a conventional display memory means.

In order to solve the conventional problems, it is fundamental of the method according to the present invention to display data of pixels according to their sequence or carry out reduction display. According to the present invention, to achieve the above described object memory elements of 2^m which compose the pixel memory means are numbered sequentially from 0 to $2^{m}-1$, then pixel data are written into the pixel memory with a group of the pixel data of 2^m arranged in time series which compose a picture image to the identical address of each of the memory elements, and when monitoring display is required, the written pixel data are read out of the pixel memory in parallel, and in the case of rearranging the pixel data in time series, when the pixel data are written after having been subjected to series/parallel conversion, by controlling addresses which are given to the pixel data at parallel/series conversion time after the pixel data having been read out, in addition, also controlling the series/parallel conversion and the parallel/series conversion, displaying the sequence of the pixel data or reduction display is fundamentally performed.

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When the data are written in the memory means, conventionally pixel data in time series (2^m) were written in the identically numbered addresses of the memory elements (2^m) according to the order of the number of the pixel. However, in the present invention according to the difference of the address to be

accessed by the memory element, the data are written by modifying the correspondence between the number of the memory and the pixel data in time series into the memory. The reason of the above described is that when reduced pixel data are read out, since the pixel data of 2^m thinned out according to the reduction ratio are read out as one group, if they have been simply written into the memory means according to the order of the memory number in time series, there occurs a condition in which necessary data of the 2^m can not be obtained, when one parallel reading out of the memory elements of 2^m.

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In order to read out the data written as described the above in the memory elements so that usual display or reduction display may be carried out, each of the memory elements addressed independently is accessed so that necessary data of 2^m may be obtained by one parallel reading from the memory elements of 2^m, and in the case of reduction display, each of the addresses in which necessary data are accommodated when data are thinned out is respectively read out in parallel simultaneously, and then these read out data of 2^m are displayed by rearranging these read data in time series.

By citing an example of one second (1/2) ratio display, more concrete description will be given as follows. To address K = 0, 1, 2, 3, ... of the memory elements the pixel elements the pixel data of 2^{m} of the

(2Kth) pixel data group are written into the (2Kth) address of the memory elements (numbered by even number address) by coinciding with the order of the pixel data with that of the memory elements, the pixel data of 2^m of the (2K+1.th) pixel data group are written with the number of the memory elements in the same sequence of the pixel data, that is, with the order of 1, 0, 3, $2, \ldots, 2^m-1, 2^m-2$.

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Next, when the pixel data are read with the usual display the pixel data read out of the (2K.th) address are output to the side of the monitoring means according to the number of the memory elements, and the pixel data read out of the (2K+1.th) address are output to the side of the monitoring means with the number of the memory elements 1, 0, 3, 2,... $2^{m}-1$, $2^{m}-2$ sequentially.

When the pixel data are read out with a half (1/2) reduction display, a vertical and a horizontal addresses which are given to the memory elements are doubled that of the usual display, and at the same time pixel data are read from the even numbered memory elements, and simultaneously through independent address lines of another system pixel data are read out of the odd numbered memory elements with a horizontal address which is made by adding 1 to the even numbered horizontal address.

Thus, by controlling address data of m bits which select the memory elements the read out pixel data of

 2^{m} are assembled to the data in time series and output to the monitoring side.

In general the smallest reduction ratio of a picture image obtained only by thinning out the picture image data without generating distortion in the picture image by using memory elements of 2^m is $1/2^m$. In this case it is adapted that usual display, $1/2^m$ reduction display, 1/4 reduction display, ... 1/2 reduction display can be freely selected.

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The order of the picture image data being stored in the memory elements of 2^m is as follows, that is, with respect to the least significant bit (LSB) address 2^m of the memory elements (for from address 0 to address 2^m), to the address 0 the pixel data are stored according merely to their order in sequence of the number of the memory elements, to address 1 pixel data which are shifted by 1 in their order are stored according to the order of the number of the memory elements. Picture image data being forced out are entered to addresses of emptied number of the memory elements generated by having been shifted 1. As described the above, the picture image data are stored by shifting by 1 up to addresses 2^m-1 of the memory means.

By storing the picture image data as described the above, the thinned out picture image data can be read out.

The order of the data to be read out in the usual case is that the read out pixel data of 2^m are modified so that they may be arranged in the same order as the picture image data according to the least significant bit (LSB) addresses 2^m of the memory elements. In the case of 1/2 reduction display, the vertical address and the horizontal address are doubled of that of the usual display, those even numbered memory elements give the least significant bit (LSB) addresses 2^{k} (k = 0, 1, 2,... m/2) to the memory means through independent address lines and read out the pixel data therefrom, and the odd numbered memory elements give the least significant bit (LSB) addresses 2^k-1 to the memory means and the pixel data are read out of the memory means. Thus, the addresses of total 2^m are arranged according to the order of the pixel data.

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Generally, in the case of $1/2^n$ reduction display $(n=1, 2, \ldots, m)$, the vertical addresses and the horizontal addresses are multiplied by 2^n , and those multiplied by 2^n vertical and horizontal addresses are divided into groups of the memory elements at every memory element numbers 2^n through independent address lines, and at every the least significant addresses of 2^n , regarding 0th address of the memory elements in the memory elements groups, the pixel data read out of basing 0th address (which means that the data are read out of by accessing to the 0th address) are read, regarding the first of the memory elements, pixel date

read out of basing the first address are read, and regarding kth memory elements, pixel data read out of basing on the kth address are read. Thus, the sum of 2^m are read out, and those pixel data are aligned according to their order.

In the present invention, according to a value of the lower ranked address, a method for modifying order of the pixel data being stored, a method for reading out the pixel data by changing addresses to be accessed at every pixel memory according to an object to be displayed (usual display, reduction display) and the lower ranked address 2^m, and basing on a method of rearranging the order of pixel data basing on the object, thus, order of the pixel data are appropriately selected to achieve usual display or reduction display.

BRIEF DESCRIPTION OF THE DRAWINGS

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- Fig. 1 is a schematic block view of one of embodiments of the present invention;
- Fig. 2 is a view illustrating a method for thinning out pixel data in this embodiment;
 - Fig. 3 is a view showing correspondent size of a memory with that of a picture plane in the embodiment;
 - Fig. 4 is a view illustrating composition of picture image data;
- 25 Fig. 5 is a diagramatical view of a memory block;

Fig. 6 is a detailed view of a writing circuit of a picture image memory;

Figs. 7(A),7(B) and 7(C) are views which explain status of writing data;

Fig. 8 is an illustration view of a reading circuit;

Figs. 9(A), 9(B) and 9(C) are explanation views of reading out and P/S conversion in the case of reduction display;

Figs. 10(A) and 10(B) are views explaining the normal display;

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Fig. 11 is a detailed view of a writing circuit of the other embodiment;

Fig. 12 is a detailed view of the reading circuit of the embodiment shown in Fig. 11; and

Figs. 13 and 14 are detailed views explaining the block circuit shown in Fig. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the present invention will be

concretely explained in the cases of 1/2 reduction

display and usual display (magnification is 1) basing

on the following embodiments.

As shown in Fig. 3, the embodiment is provided with a display memory 1 having size of horizontal length x vertical length being 2048 x 2048, and there are some cases in which the display memory 1 is

displayed on a CRT monitor 2 having a picture plane size of 1024×1024 . In usual, a memory area (ln) is equal to the size of the picture plane of 1024×1024 .

picture image data stored in the display memory 1 comprises, for example, as shown in Fig. 4, picture data of the number of 4M which are numbered from 0 to 22²² - 1 according to time sequence thereof. In the case of a color picture image display used in a color plate making system, the amount of the whole information is 4M x 1 byte x the number of colors, however, here, information of the 1 byte which expresses gradation and the number of colors are not displayed, so that we do not give further explanation thereto.

In Fig. 4, the pixel data of 4M are represented with the number of groups of time sequentially determined to which they belong and number of locations of the pixels in the group.

For example, pixel data of 16 (2^m ...2⁴ = 16)

located at the upper corner of the left hand represent
16 data, that is, data at location numbers of the
pixels in the 0th group, 0, 1, 2, ...9, A, B, C, D, E
and F. In the data groups at the upper corner of the
right hand, there are shown 16 pixel data of time

sequentially determined 127th group. The last data
located at the lower corner of the right hand represent
pixel data of the number of 0 to F in the (2¹⁸ - 1)th
group.

Hereinafter, when pixel data are to be shown, they are indicated as a combination of the group numbers 0th to $(2^{18} - 1)$ th and the pixel location numbers 0 to F. Pixel data in the groups from the 0th group to the $(2^{18} - 1)$ group are divided into 128 groups (128 x 16 = 2048) in the horizontal direction and into 2048 groups in the vertical direction, so that they may correspond to the size of the display memory 1 (shown in Fig. 3).

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The display memory 1 comprises, as shown in Fig.

5, 16 pieces of memory elements (M),...(M) which are disposed in parallel and each having 256K x 1 bit memory capacity. The display memory 1 composes a memory block (MB) and this memory block (MB) is used as 1 bit x 4M in the display memory 1.

15 Each of the memory elements (M) is previously numbered 0, 1, 2, ..., E and F, respectively.

Hereinafter, each of the memory elements is indicated discriminatingly by each of the number.

The memory elements (M) have numbers from 0 to (12¹⁸ - 1), and assuming that picture image data of time sequential order are accommodated in the memory elements according to the address order, and they are made to correspond to the composition of the picture image data shown in Fig.4, the 16 pixel data in the nth group are accommodated in the same address in each of the memory elements (M), that is, are accommodated in the nth address.

Fig. 1 shows a schematic block showing a display system which can reduce 4M picture to 1M (1024x1024) picture.

Circuit blocks 3, 4, 5, 6, 7 and 8 are controlled by a signal from a microprocessor 9.

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A vertical address generating circuit 3 generates addresses from $0 + \alpha$ to $1023 + \alpha$ (here, α is a constant set up by the CPU 9, and indicates integers from 0 to 1024 which represent shift values in the vertical direction, and in the case of 1/2 reduction display, value 0 is set up.), in synchronization with a horizontal synchronizing signal from the CRT 2.

A horizontal address generator 4 generates addresses from $0 + \beta$ to $1023 + \beta$ (here, β is a constant set up by the CPU 9, and indicates integers from 0 to 1024 which represent shift values in the horizontal direction. In the case of 1/2 reduction, 0 is set up.) within one horizontal synchronizing signal period.

A display memory writing circuit 5 feeds an address signal of 4 bits for selecting memory element to the display memory 1, when data are written.

Picture image data accommodated in a disc 10 are written into the display memory 1 through the display memory writing circuit 5. The circuits 6 and 7 enable only when a control signal which indicates reduction display is given from the microprocessor 9.

The circuit 6 doubles vertical address generated in the vertical address generating circuit 3. The circuit 7 doubles highly ranked 7 bits of the horizontal address generated in the horizontal address generating circuit 4.

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A P/S conversion control circuit 8 controls a P/S conversion circuit 11 at the rear stage of the display memory 1, basing on an address signal of lower ranked 4 bits fed from the horizontal address generating circuit 4. The P/S conversion control circuit 8 operates with two manners for normal display and reduction display which are different from each other, in response to the control signal from the microprocessor 9. Picture image data written in the display memory 1 are accessed by 18 bits which comprises 11 bits of vertical address from the vertical address generating circuit 3 and the horizontal address composed of the highly ranked 7 bits from the horizontal address generating circuit 4.

This address composed of 18 bits is fed to each of the memory elements (M) shown in Fig.5, and from all the memory elements (M) data for one pixel are read out. Reading is carried out every 320ns period (access time of the memory element is equal or shorter than its access time).

The data of 16 pixels read out in parallel to one another from the display memory 1 are converted to series data by a clock of 20ns in the P/S conversion circuit 11. The series pixel data are converted into

an analog signal(s) in the D/A conversion circuit 12, and displayed on the CRT 2 one pixel for every 20ns.

A method for controlling address will be explained by referring to Figs. 6 and 7, as follows.

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Each of the memory elements (M) is accessed by a memory element address Madd of 18 bits comprising 11 bits vertical addresses 0 to 10 and highly ranked 7 bits Hadd 4 to 10 among the horizontal addresses Hadd 0 to 10. The lower rank 4 bits Hadd 0 to 3 are used to access (chip select) to the address in the memory element (M).

When this address Madd is an even number (Hadd 4 = 0), data of 16 pixels in one group arranged in sequence order are written by every one pixel data according to the memory element number, that is, 0, 1, 2, 3,...E and F, sequentially. For example, if they are pixel data in the 0th group, the first pixel data (0,0) (pixel location number in the 0th group) thereof are written in 0 address of a memory element (M - 0), and those of the second (0,1) are written in 0 address in a memory element (M - 1).

When the address Madd to be given to the memory element is an odd number (Hadd4 = 1), 16 pixel data of one group are written in time sequence order according to the memory element number, 1, 0, 3, 2, 5, 4,...F and E.

For example, if the data are the pixel data in the first group, the pixel data (1,0) are not written to

the address 1 of the memory element (M - 0), but written to the address 1 of the memory element (M - 1), and the pixel data (1,1) are written in the address 1.

To control this writing, as shown in Fig. 6, instead of using conventional horizontal address LSB, an output Haddo' of an exclusive OR circuit 13 of which inputs are LSB (= Haddo) of the horizontal address and LSB (= Hadd4) of the Madd of the memory address element is applied.

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A decoder 14 providing 4 inputs and 16 outputs generates each of chip select signals CSO, CS1, CS2,..CSF of the respective memory elements (M - 0), (M - 1),..(M - F) from HaddO', Haddl, Hadd2 and Hadd3, but if Hadd4 = 0, HaddO is equal to HaddO' (HaddO! = HaddO), CSO, CS1,...,CSF are enabled according to this order. On the contrary if Hadd4 = 1, then, HaddO = HaddO', and the CS1, CSO, CS3,..,CSF, CSE are enabled according to the afore described order.

As described the above, appearance of the pixel data written in each of the memory elements is illustrated in Fig. 7(B). In the case of generating timing of the pixel data being early (for example, 20ns), the picture data are latched by a latch circuit being provided additionally according to the select signals (CSO, CS1, CS2,...,CSF), and the latched 16 pixel data are written into the memory element in parallel at every writing period (320ns).

Thus, in order to write in and read the latched picture data from the display memory for 4M pixels (normally, 1M pixels among 4M pixels are displayed), the order of picture data is remained what it is, when the read out address Hadd4 is an even number, and in the case of it is an odd number, the order of the picture data are alternated.

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In order to read out the picture data and display in 1/2 reduction, the following steps are required. That is, setting α and β in the case of the normal display to 0, doubling the address of Hadd of highly ranked 7 bits and the address Vadd of 11 bits, reading out merely addresses of even numbers in correspondence with the even numbered memory elements (M - 0), (M - 2), (M - 4),..., (M - E), and simultaneously reading out each of the above odd numbered by adding 1, respectively, for the odd numbered memory elements (M - 1), (M - 3),..., (M - F). In Fig. 7(B), pixel data to be read out are surrounded by circles, which indicate a relation between the pixel data and the memory addresses.

Here, the address produced by doubling the address in normal display means that, as shown in Fig. 1, the highly ranked 7 bits of the horizontal address which is an address of the memory element in the case of α and β are set to 0 and the 11 bits of the vertical address are doubled, respectively.

In the case of a necessary picture image being displayed by the normal (0,0) pixel data, display size is 1024×1024 , accordingly, address of 10×10 bits is sufficient, and in both the horizontal and the vertical addresses are, when α and β are 0, the most significant bit is always 0. Therefore, even if displaying address from this (0, 0) data is doubled, there occurs no overflow, and, of course, by an address of 18 bits each of the memory elements is accessed.

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An example of a circuit performing the above described control is shown in Fig. 8.

As shown in the figure, an exclusive OR circuit 17 providing with two line systems comprising an address line (15) connected with those even numbered memory elements (M-0), (M-2), (M-4),...,(M-E), and an address line 16 connected with the odd numbered memory elements (M-1), (M-3),...,(M-F). The exclusive OR circuit 17 also works to add 1 to all the even numbered addresses.

That is, when a normal/reduction display switching signal EX is switched to "l" (corresponds to high level signal [H]), the doubled address wherein \(\precede \) and \(\precede \) are 0 is fed to the even numbered memory elements by an address line 15 through a gate circuit 18, and simultaneously an odd numbered address signal to which l is added, (the least significant bit of the address signal is \(\overline{Hadd4} \) generated by inverting the Hadd4), is

fed to the odd numbered memory elements through the address line 16.

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From each of the memory elements data D0 to DF are simultaneously read out at every period (320ns), and fed through a latch means 26 to a selector 25.

For example, if the doubled address Hadd4 is set to be 0 address, data of (0, 0), (0, 2), (0, 4)....are read from the even numbered memory elements to D0, D2, D4,.., and from the odd numbered memory elements data of (1, 0), (1, 2), (1, 4)....are read to D1, D3, D5, ...(shown in Fig. 9(A)).

These read out data D are not aligned according to the time sequence. Accordingly, it is adapted that when P/S conversion is performed, display data in good order shown in Fig. 9(B) can be obtained by controlling the low rank 4 bits signal of the horizontal address.

That is, as shown in Fig. 8, one data are selected from the 16 output data D0 to DF by applying the selector 25 which selects one data, and instead of setting 4 bits select signal to be Hadd0, Hadd1, Hadd2, Hadd3, they are switched to the order of Hadd3, Hadd0, Hadd1 and Hadd2 by the selectors 21 to 24, and thus, output data are to be arranged to the order of the time sequence.

The select signal is sent from the P/S conversion control circuit 8.

The normal/reduction switching signal EX is set to [H], a control input signal B turns to [H], and either

input 2 or 3 of each of selectors 21, 22, 23 and 24 which has 4 inputs and selects one of them is selected. Then, Hadd3 is set as the LSB, and from the selectors 21, 22, 23 and 24 Hadd0, Haddl and Hadd2 are sequentially output.

In the case of normal display in which any given

lM of memory area of 4M, the normal/reduction switching

signal EX is turned to a low level signal [L].

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By the signal EX, the gate 18 closes and a gate circuit 19 is opened. The normal memory element address in which the vertical and the horizontal addresses advance by 1 is input as an identified signal to all the memory elements simultaneously, through the gate circuit 19 and passing through the address lines 15 and 16.

Heretofore, descriptions are made by assuming the case of reduction display, so that different writing manners according to the case of odd numbered address and that of even numbered address have been explained, when the pixel data are written.

Accordingly, the select signal to be fed to the selector 25 is to be controlled by the LSB Hadd4 of the horizontal address of the memory element.

That is, since the control input B of the selectors 21, 22, 23 and 24 is [L], input 0 or 1 is selected, while according to the control input A to which Hadd4 is input, either of input 0 or 1 is selected. In the case of the even numbered address, an

input 0 is selected at Hadd4 = 0, then Hadd0 becomes the LSB. In the case of the odd numbered address, an input 1 is selected at Hadd4 = 1, and then the LSB becomes to $\overline{\text{Hadd0}}$.

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Basing on the above described fact, in the selector 25, when the memory element is an even numbered address, the order becomes as D0, D1,..DF, and when it is an odd numbered address, the order is D1, D0, D3, D2,...,DF and DE. The exclusive OR circuit 17 and the selector 25 play the same role as that of the P/S conversion circuit 11 shown in Fig. 1. In Fig. 10 there are shown this reading operation and manner of P/S conversion.

The above described embodiment relates to the case of 1/2 reduction display, and by applying the same method $1/2^n$ reduction display is also possible.

That when there are memory elements of the number of 2^m, the normal display, 1/2 reduction display,..1/2^m reduction display can be achieved has been already mentioned. Therefore, explanation will be given regarding a case in which the number of the memory elements is 16 as another embodiment.

With reference to Fig. 7(c), sequence for writing pixel data will be described hereinafter.

In 1/16 reduction display, to read out every 16 pixel data from the memory elements of 16, it is required that from a memory element numbered 0, pixel data numbered 0 in the 0th group are read to the

address 0 of the LSB addresses (Hadd4 to 7) of the memory elements, and from a memory element numbered n, pixel data numbered 0 in the nth group are read to the address n of the LSB of the memory elements. With reason above described, as shown in Fig. 7 (c), in an area diagonal with angles of 45 degree downward in the range of coordinates from (0, 0) to (F, F), pixel data of 0 address of each of the groups are written.

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Next, regarding 1/8 reduction display, to read out every 8 pixel data from 16 memory elements, since in the memory elements numbered 0 to 7 pixel data of 0th address in each of the groups being written at the 1/16 reduction display, pixel data of 8th address in each of the groups are written in the memory elements numbered from 8 to F. With respect to the LSB address 0 of the memory element, when pixel data are written into memory elements according to the order of the element number, same explanation as the above described 1/16 reduction display can be applied.

Quite same explanations can be also applied to cases of 1/4 reduction display and 1/2 reduction display, so that Fig. 7(c) can be drawn.

In Fig. 11 there is shown an example of a writing circuit, in Fig. 12, Fig. 13 and Fig. 14, there are shown examples of writing circuits.

With respect to the example of the writing circuit explanation will be given as follows.

Difference between the circuit shown in Fig. 6 and that of this lies in providing an adder 31 to this circuit instead of the exclusive OR circuit 13.

The memory element number is selected in the horizontal direction address (Hadd0 - 3), and at the LSB address (Hadd4 - 7) of the memory element, the time sequence of the pixel data being written and the order of the memory element number are shifted.

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In the adder 31 addresses (Hadd0 - 3) and

addresses (Hadd4 - 7) are added. Overflow resulting
from the addition is neglected, and as shown in Fig.

7(c), according to the LSB address of the memory
element, writing is performed in the predetermined
order. In the case of timing of occurrence of pixel

data being early, a latch circuit (not shown) is
provided, and latched picture image data are latched by
the select signals (CSO, CS1,...,CSF), and then the
parallel 16 pixel data are written in the memory
element at every period.

Next, an example shown in Fig. 12 (an example of writing manner shown in Fig. 11) will be explained.

Difference between the example and that of shown in Fig. 8 lies in substituting the P/S conversion circuit 8 and the exclusive OR circuit 17 for a new P/S conversion circuit 8' and an address forming circuit of each element 32.

Needless to say that the address doubling circuits 6 and 7 must be vary their setting to 2 times, 4 times,

8 times, 16 times etc. according to desired reduction display, and shift values α and β are set to appropriate shift values such as 0; $\alpha/4$, $\beta/4$, $\alpha/8$, $\beta/8$; $\alpha/16$, $\beta/16$ etc.

Details of the P/S conversion circuit 8' are shown in Fig. 14 and those of the address forming circuit of each element 32 are shown in Fig. 13. Rearrangement of the pixel data is completed by functions of the P/S conversion circuit 8' and the address forming circuit of each element 32.

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In these circuits addresses may be previously formed in a ROM which addresses the addresses Hadd0 - 7 and reduction ratio so that necessary pixel data . necessary for each of reduction display cases shown in Fig. 7(c) may come out in the order of the data.

Fig. 13 shows an embodiment of the address forming circuit of each element 32. It is composed of gate providing selectors (51-0)-(51-F) and adders (52-0)-(52-F), and to an address of each of the memory elements (M-0)-(M-F) a shift amount according to the reduction ratio is added in an adder 52, and the shift amount is selected in selectors (51-0)-(51-F).

In an address Add MO of the 0th memory element (M - 0), the shift amount is always 0 irrespective of the reduction display. In the normal display a G input of the selector 51 level [H] is input, and all outputs of the selector become 0. The shift amount is 0.

Values of A and B are, when reduction ratio is 1/2, 0 and 0, when reduction ratio is 1/4, 1 and 0, in the case of reduction ratio being 1/8, 0 and 1, and when 1/16, 1 and 1. The selector 51 selects 0 input at 1/2 reduction display, 1 input at 1/4 reduction display, 2 inputs at 1/8, and 3 inputs at 1/16 reduction display.

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An address AddM ℓ of the ℓ th memory element (M - ℓ) is divided into 2 groups, that is, they are the following 2 groups; the first group which includes even numbered addresses at which the shift amount is 0 in the case of 1/2 reduction display, the second group which includes odd numbered addresses at which the shift amount is 1 in the same case, and quite the same at the 1/4 reduction display, in this case the address is divided into 4 groups. To the 0th group a shift amount 0 is added , to the first group a shift amount 1 is added, to the second group a shift amount 2 is added, and a shift amount 3 is added to the third group. In the case of 1/8 reduction display, the address is divided into 2 groups of 8 addresses, and at the 0th address of the group shift amount is 0,....and thus, at the 8th address of the group shift amount is In the case of 1/16 reduction display, the number of the memory element is the shift amount thereof.

In Fig. 14, there is shown an embodiment of the P/S conversion control circuit 8' which is composed of a selectors 71 - 74, an adder 77 and gates 75 and 76.

In the case of normal display, a signal of level [H] is input to the gates 75 and 76, and both A and B turn to [H], then, according to the order of addresses Hadd0 - 3 of 3 inputs of the selectors 71 to 73, they are output. At the adder 76 addresses Hadd4 to 7 are added thereto and are output to the selector 25. As shown in Fig. 7(c), the addresses Hadd4 to 7 are added to the addresses Hadd0 to 3 as shift amounts.

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In the case of 1/2 reduction display, the addresses HaddO to 3 exist at every two addresses, accordingly, by slipping off the HaddO - 3 by 1 (that is, as the order of Haddl, Hadd2, Hadd3, HaddO), at every 2 addresses the number of the memory elements are selected and added the Hadd4 to 7 thereto, they come to be equal to the shift amount in the address direction of the memory element shown in Fig. 7(c).

In the case of 1/4 reduction display, the Hadd0 - 3 exist at every 4 addresses, so that by slipping off by 1 from each of the conditions in the case of 1/2 reduction display, that is, each of the Hadd0 to 3 is slipped off by 1 (i.e., in the order of Hadd2, 3, 0, 1), at every 4 addresses memory elements are selected and the Hadd4 to 7 are added thereto, so that it comes to be equal to the shift amount in the address direction of the memory element shown in Fig. 7(C). Then, overflow is neglected.

Since in the case of 1/8 reduction display, the HaddO to 3 are at every 8 addresses, by slipping off

the Hadd0 - 3 by 1 from the case of 1/4 reduction display (in the order of Hadd3, 0, 1, 2), at every 8 addresses memory elements are selected, and by being added the Hadd4 to 7 they come to be equal to the shift amount in the address direction of the memory elements shown in Fig. 7(c). In 1/16 reduction display, the Hadd0 - 3 exist at every 16 addresses, so that the addresses makes a round which results in returning to the original order.

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The data outputs from the memory elements (M - 0) - (M - F) are fed to the selector 25 through the latch circuit 26 at every reading period.

In this embodiment, for example, as shown in Fig. 7(C), writing and reading pixel data are adapted to be sequentially slipped off, however, it is needless to say that if ROM is used, within periodical range pixel data can be read out with any desired order irrespective of the order.

As described the above, the present invention is to control writing and reading pixel data to the memory element, and further control arrangement of the read out data, and therefore the present invention can realize not only 1/2, 1/4 reduction displays but also, in general, up to 1/2ⁿ reduction display.

25 In the above described embodiment it is premised on cases in which size of the memory is larger than that of the picture plane, however, even in the cases

of the size of the memory is equal to or smaller than that of the picture plane, this method can be applied.

If switching from normal display to reduction display or vice versa is performed for blanking duration of a monitor, no disturbance is generated on the displayed picture image.

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Further, in the above described embodiment, explanation is given regarding the cases in which the picture image is displayed on a CRT monitor, of course, it is also possible to apply the present method to a case of printing the picture image (reduction picture image) with a printer.

As described the above, according to the present invention, it is adapted that addresses to be given to picture memory means are controlled so that time sequential picture data may be thinned out by pixel data corresponding to the reduction ratio, accordingly, a reduced picture image of high fidelity to the original picture can be obtained, in addition, without using any high speed memory element, and without applying a plurality of picture memory means, but merely using conventional picture memory means, reduction picture images of high fidelity to the original picture can be obtained.

25 Further, since only addresses are changed, for an instant (for example, 1/30 or 1/60 second) switching to a normal picture display or a reduction picture display can be performed.

WHAT IS CLAIMED IS:

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1. A method for displaying a picture image in which pixel data being aligned in order are divided into every 2^m groups, said pixel data of each of the groups are written in the same numbered addresses of the 2^m memory elements and read out the 2^m pixel data in parallel from said 2^m memory elements, and performs parallel-series conversion to display the picture image on a picture plane of a monitor, characterized in that:

when the pixel data are written in said memory elements, at least every two consecutive addresses in

said memory elements of 2^m said memory elements are accessed, and an order of said consecutive 2^m pixel

data are varied according to said accessed addresses,

identical specific numbered pixel data at least in two consecutive groups are controlled at least every two

groups of so that they may be written in different

numbered memory elements with each other, in the case

of reading out pixel data from memory elements, data of

 2^{m} read out of said memory elements of 2^{m} by

consecutive addresses are rearranged according to said

writing control in the case of normal display, in the $\,\cdot\,$

case of $1/2^{\mathrm{n}}$ reduction display both vertical and

horizontal addresses are multiplied by 2ⁿ according to

 $1/2^n$ reduction, and said 2^m memory elements are read out basing on different 2^n addresses obtained according

to the writing control, basing on said writing and

reading control, either of normal picture images or reduction picture images can be displayed freely.

2. A method for displaying a picture image according to claim 1, wherein when the pixel data are written in the memory elements, even the numbered groups of every 2^m consecutive sequential pixel data are written in 2^m memory elements according to the order of the pixel data, and the odd numbered groups of the 2^m pixel data are written in the 2^m memory elements by substituting the even numbered pixel data for the odd ones, respectively.

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A method for displaying a picture image 3. according to claim 2, wherein when the normal display is performed by reading out the pixel data from the memory elements, data are read out from the 2^m memory 15 elements, if the LSB address which accesses the memory element is an even number, a normal picture display is produced by controlling the monitor according to the order of the sequence of the memory elements, and in the case of the LSB address which accesses the the 20 memory element is an odd number, the normal picture display is produced by controlling the monitor according to an order of having been replaced the even numbered memory element with the odd numbered ones.

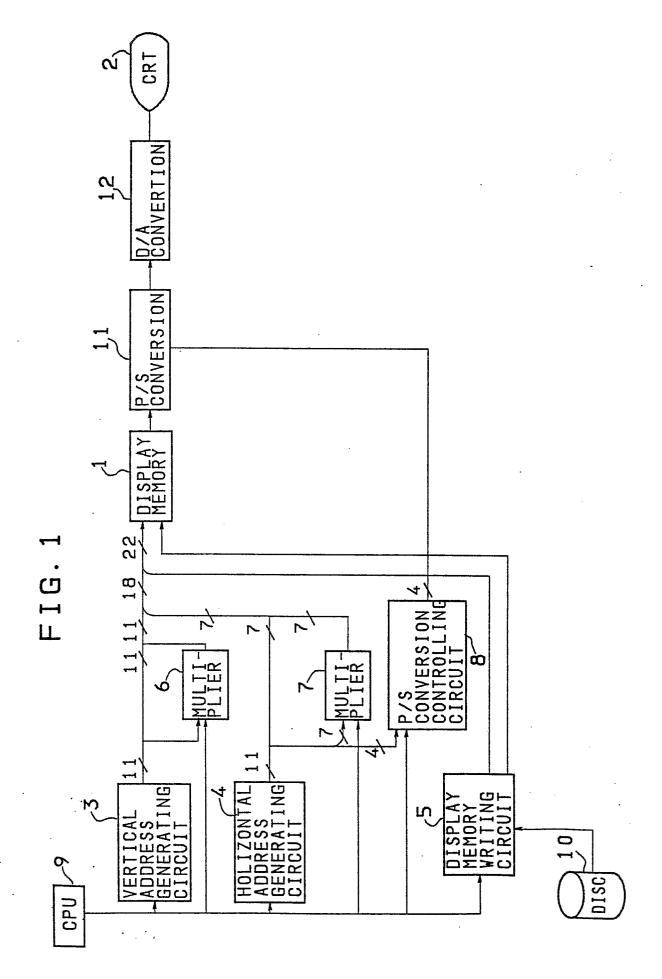
- A method for displaying a picture image 4. according to claim 2, wherein in the case of 1/2 reduction display by reading the pixel data from the memory elements, both the vertical and horizontal addresses are doubled, an even numbered address is 5 added to each of even numbered memory elements independently and to each of odd numbered memory elements an odd address is added independently, by reading out 2^m data every pair of consecutive even and odd numbered addresses, the read out data from the even 10 numbered memory in order with the number of the memory elements and the read out data from the odd numbered memory elements in order with the memory elements are sequentially displayed on the monitor.
- 15 5. A method for displaying a picture image according to claim 1, wherein when the pixel data are written in the memory elements, an order of the consecutive pixel data of every 2^m are circulatingly shifted according to a value corresponding to a memory element access address to store the shifted pixel data according to the sequence of memory element in the memory element.
 - 6. A method for displaying a picture image according to claim 5, wherein when the pixel data are read out of the memory means for the normal display, by rearranging the read picture image data of 2^m in

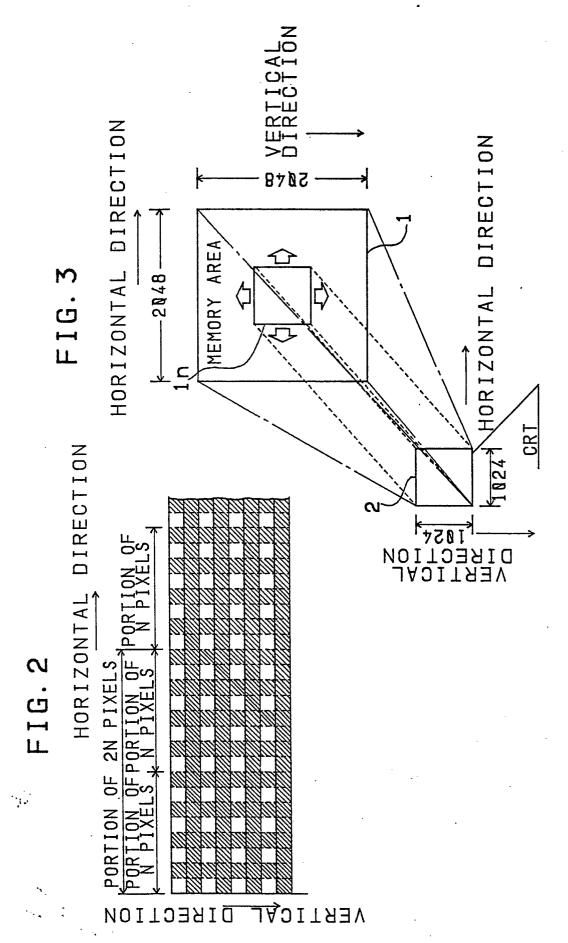
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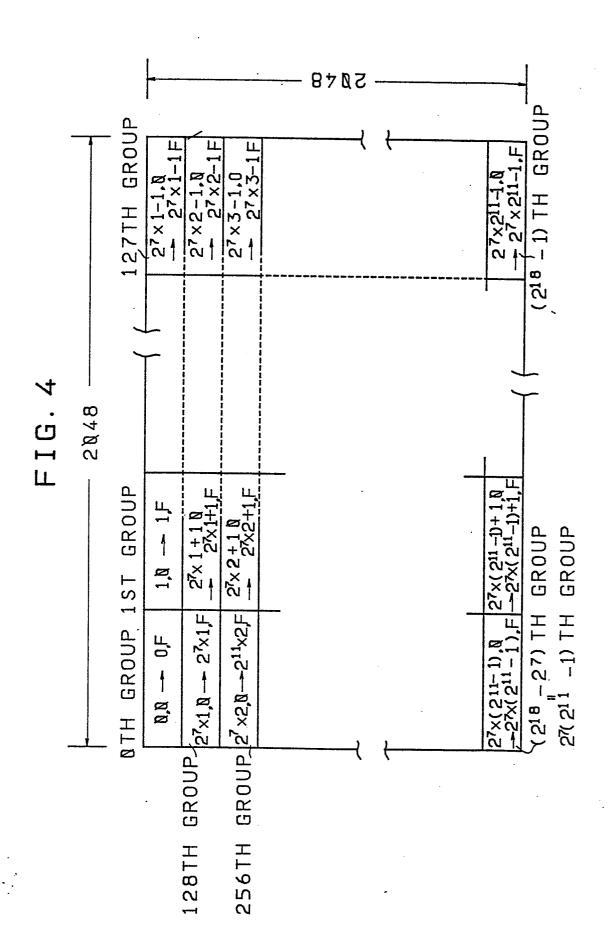
response to a value of the LSB of access address, the normal picture display is carried out by the monitor.

7. A method for displaying a picture image according to claim 5, wherein when 1/2ⁿ reduction

5 picture is displayed by reading out the pixel data from the memory element, the vertical and the horizontal addresses are multiplied by 2ⁿ, divided into 2ⁿ groups basing on order of the address number, the LSB addresses are given to the memory elements and further 0, 1,...2ⁿ⁻¹ are independently given to the memory elements, according to a value of each of the LSB 2^m of the respective access address the data are rearranged to display 1/2ⁿ reduction display by the monitor.

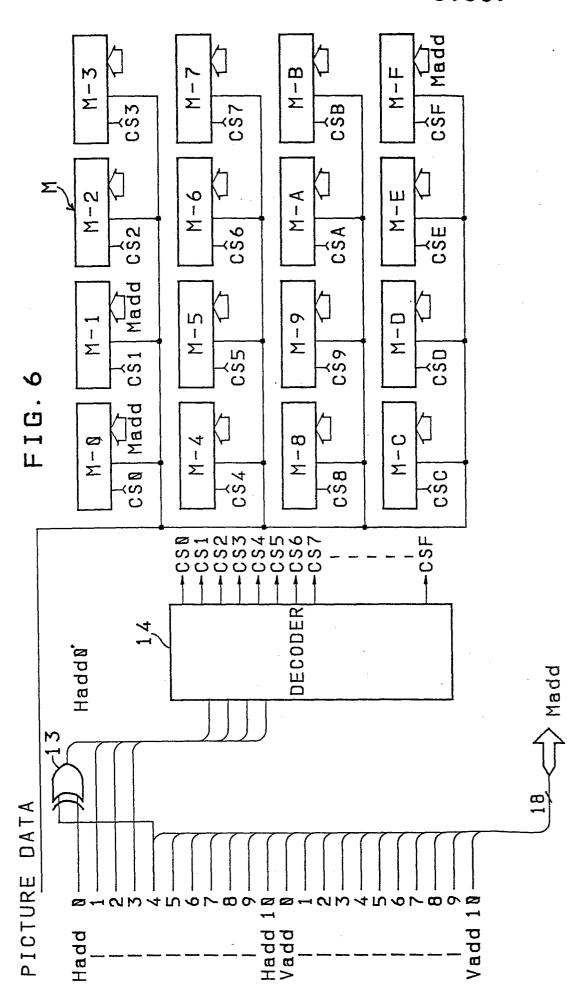






	₩ W			0196733
	N.3 1,2 2,3 3,2 · 127,2 M-3	8,7 1,6 ···· 127,6 M-7	0,8 1,A ···· 127,A M-8	8.F 1,E · · · · 127.E M – F
FIG. 5	N.2 1,3 2,2 3,3 · 127,3 M-2	0,6 1,7 ···· 127,7	8,A 1,B ···· 127,B M-A	0,E 1,F ···· 127,E M − E
FI(8,1 1,8 2,1 38 · 127,8 M-1	8,5 1,4 ···· 127,4 M-5	N.9 1,8 ···· 127,8 M-9	8,0 1,0 ···· 127,0 M-D
Σ	0.0 1.112.0 3.1 ·· 127.1 M-0	0,4 1,5 ···· 127,5 M-4	8,8 1,9 ···· 127,9 M-8	&C 1,0 127,0

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Ъ	Ц	
GROU	<u> </u>	
3RD	Q 1 2	
GROUP	<u> </u>	
2ND	M 1 2	
GROUP	<u>Ц</u>	
1ST G	1 2	
•	Ø L	
GROUP	<u>田</u>	
MH	Ø 1 2	

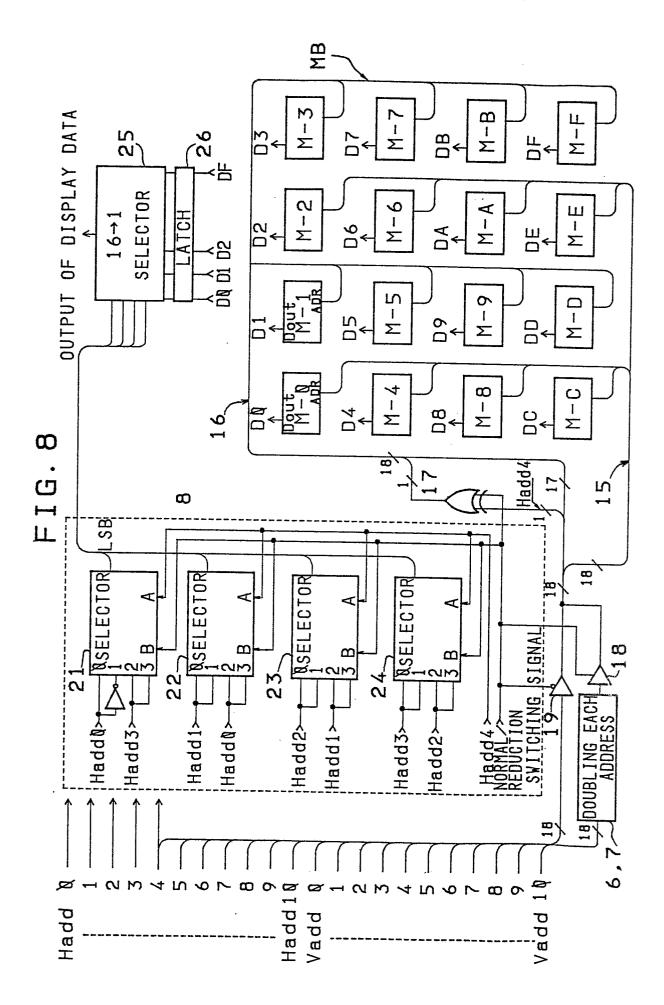
---→TIME SERIES ORDER

FIG. 7(B)

		NTH GROUP	1ST GROUP	2ND GROUP	3RD GROUP	4TH GROUP	STH GROUP	
			\	\	\	-		
	Σμ	Щ	Ш	ш	ш	щ	ш	
	ΣШ	ш	Щ	Ш	Ш	Ш	· LL	
	ΣΩ		ပ		ပ		C	
	Συ	ပ	0	ပ		ပ	О	**************************************
	Σm	В	A	В	A	В	A	angalahanga da gab gan hiri dar dap gapingalikirininyakkunang
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<u></u>	Σω	8	6	æ	6	8	6	
EMENI	ΣΝ	7	9	2	9	7	9	
Ш	Σ 9	9	~	6	7	9	~	
Ш	ΣΩ	N	4	5	. 4	ΩÍ	4	
MEMORY	Σ 4	4	ហ	4	5	7	IJ	
1EM	ΣM	3	2	3	2	3	S	
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FIG. 7(C)

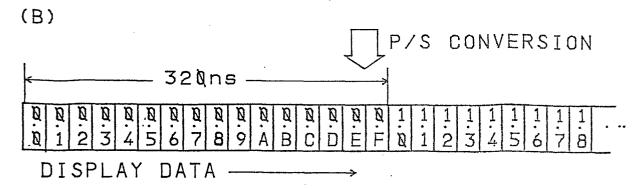
NUMBER OF MEMORY ELEMENT																	
				NU	NB	EK	U	F	ME	MU	K I	EI	_ =	1 E [N I		
		Ø	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
1	Ø	Ø	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
H Z	1	F	Ø	1	2	3	4	5	6	7	8	9	Α	В	ပ	D	E
EME	2	Е	F	Ø	1	2	3	4	5	6	7	8	9	Α	മ	С	D
EL	3		Ш	F	Ø	1	2	3	4	5	6	7	8	9	Α	В	С
⊞ ≻	4	С	D	Ε	П	Ø	1	2	3	4	5	6	7	8	9	Α	В
0R,	5	В	С	D	Е	F	Ø	1	2	3	4	5	6	7	8	9	Α
EM 56.	6	Α	В	С	ם	Е	F	Ø	1	2	3	4	5	6	7	8	9
Σ4	7	9	Α	В	С	D	E	F	Ø	1	2	3	4	5	6	7	8
A D	8	8	9	Α	В	С	D	Ε	F	Ø	1	2	3	4	5	6	7
SHA	9	7	8	9	Α	В	С	D	E	F	Ø	1	2	3	4	5	6
ES	Α	6	7	8	9	Α	В	С	ם	Ε	F	Ø	1	2	3	4	5
DR	В	5	6	7	8	9	Α	В	С	D	E	F	Ø	1	2	3	4
AD	C	4	5	6	7	8	9	Α	В	С	D	Ε	F	Ø	1	2	3
В	D	3	4	5	6	7	8	9	Α	В	C	D	Ε	F	Ø	1	2
LS	Ε	2	3	4	5	6	7	8	9	Α	В	С	D	E	F	Ø	1
	F	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F	Ø

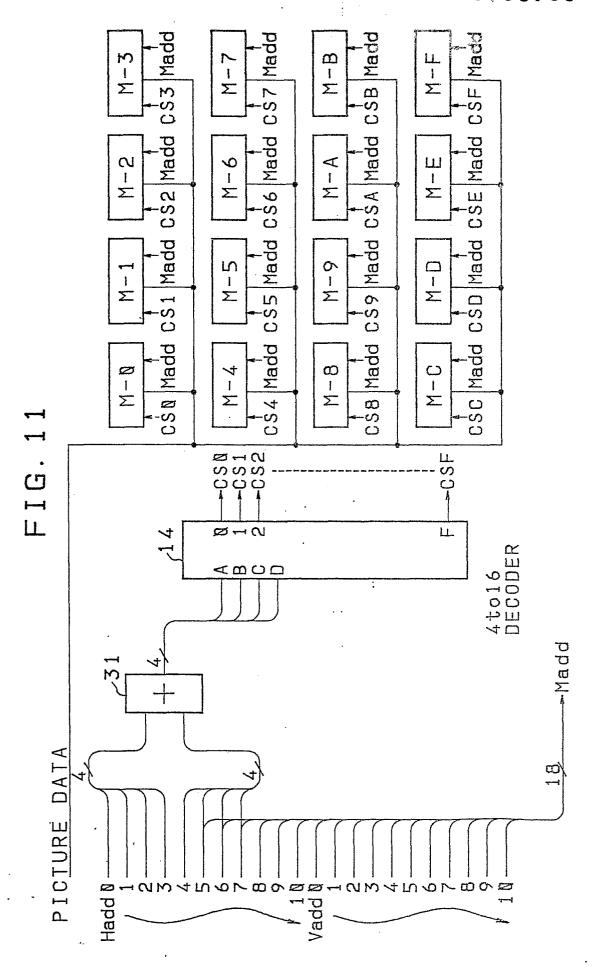


(A) F	IG. 9	320ns	320ns	320ns	
M-8		0.0	2.0	4.0	
M-1		1.0	3.0	5,0	•
M-2		0.2	2.2	4.2	•
M-3		1.2	3, 2	5.2	•
M-4		Q .4	2.4	4.4	•
M-5]→	1.4	3.4	5.4	•
M-6		0.6	2.6	4.6	•
M-7]	1.6	3.6	5.6	•
M-8]	Q. 8	2.8	4.8	
M-9		1.8	3.8	5.8	•
M-A		0.A	2. A	4. A	•
M-B		1. A	3. A	5.A	•
M-C	│	Ø.C	2.C	4.C	•
M-D]	1.C	3.C	5.C	•
M-E]	0.E	2.E	4.E	•
M-F] ——	1.E	3.E	5, E	
МВ		р	Б	5	

1	(B)												Į	J	F	/	S	C	0	N۷	ľΕ	R	s I	0	N		
	k						32	Ø S	ns	3 -					_	 >												•
	0.0	2	04	8	8	Á	Ċ	Ē	1.0	1 2	1 4	16	1 8	1 Å	1 Ċ	1 Ė	2	2.2	2 4	2.6	2.8	2 Å	2 Ċ	2 È	3	3 2	3 4	
	D	I S	SP	L	Αì	,	D	ΑT	Α						>													

(/	A) FIC	G. 10	.320ns	320ns	320ns	
	g - M		0.0	1.1	2.0	**************************************
	M-1		N. 1	1.0	2.1	*
	M-2		N. 2	1.3	2.2	
	M-3		Q.3	1.2	2.3	
	M-4		10.4	1.5	2.4	
	M-5		0. 5	1.4	2.5	*
	M-6	>	0.6	1.7	2,6	*
	M-7		Q. 7	1.6	2.7	*
	M-8		0.8	1.9	2.8	
	M-9		0.9.	1.8	2.9	
	M-A		Ŋ. A	1.B	2. A	·
	M-B	· 	N .B	1.A	2.B	
	M-C		N.C	1.D	2, Ç	
	M∹D		1 0.0	1. C	2. D	•
	M-E	>	Ŋ.E	1.F	2. E	
	M-F	<u></u>	Ŋ.F	1.E	2. F	
-	МВ		D .		Ó	vender vin till för för hap fra dan sen gg





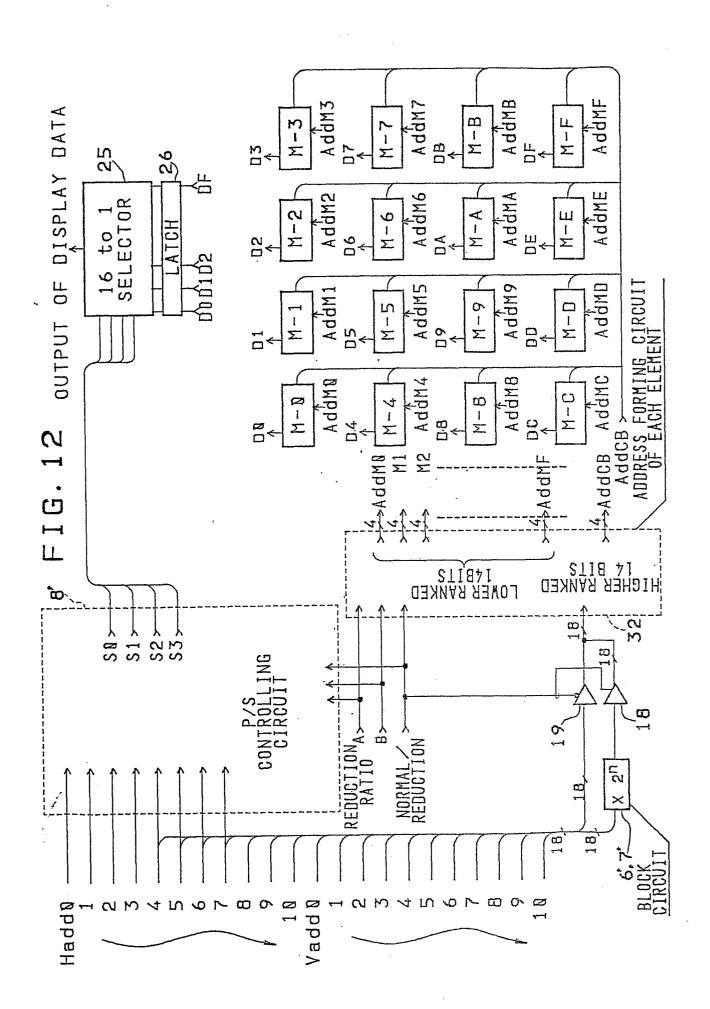


FIG. 13

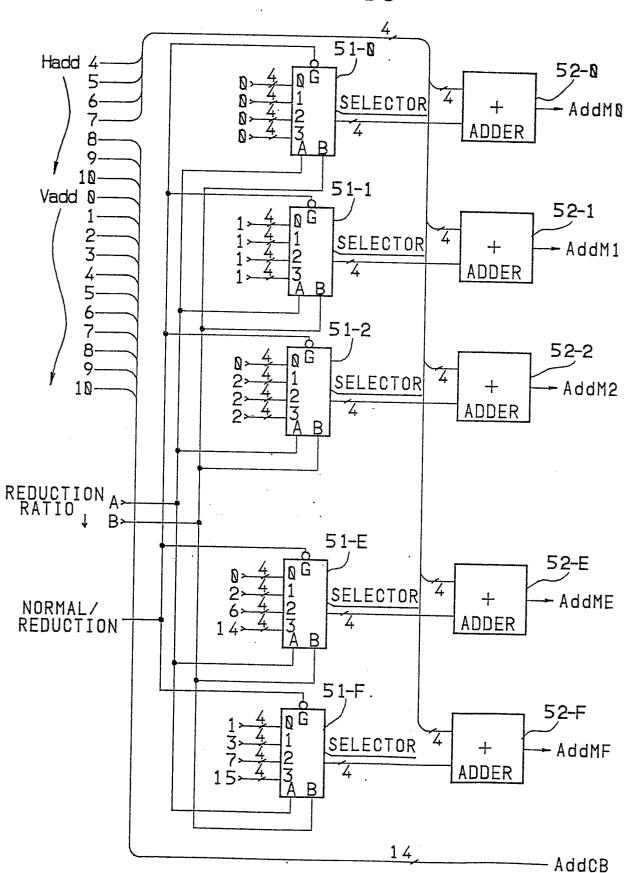


FIG. 14

