

⑫

EUROPEAN PATENT APPLICATION

⑲ Application number: 86300299.4

⑤① Int. Cl.⁴: **G 05 F 3/30**

⑳ Date of filing: 17.01.86

③① Priority: 22.04.85 US 725404

④③ Date of publication of application:
29.10.86 Bulletin 86/44

⑧④ Designated Contracting States:
DE FR GB

⑦① Applicant: **PRECISION MONOLITHICS INC.**
1500 Space Park Drive
Santa Clara California 95050(US)

⑦② Inventor: **Bowers, Derek F.**
1502 Harrison Court
Sunnyvale California 94087(US)

⑦④ Representative: **Crawford, Andrew Birkby et al,**
A.A. THORNTON & CO. Northumberland House 303-306
High Holborn
London WC1V 7LE(GB)

⑤④ Precision bandgap voltage reference.

⑤⑦ A bandgap voltage reference circuit is described in which two sets of bipolar transistors (Q7-Q12, Q13-Q17) are connected so as to accumulate their base-emitter voltages, and currents are caused to flow through the collector-emitter circuits of each transistor (Q7-Q17). The number of transistors in each set, the geometry of each transistor and the currents transmitted through their collector-emitter circuits are selected so that the accumulated base-emitter voltages of the two sets differ by an amount corresponding to a predetermined bandgap voltage, preferably 1.23 volts. The circuitry can be implemented using either CMOS or bipolar fabrication processes, and has a lower error component than prior bandgap references. In the preferred embodiment the first set (Q7-Q12) includes one more transistor than the second set (Q13-Q17), and supports a higher current density than the second set. The bandgap voltage differential between the two transistor sets (Q7-Q12, Q13-Q17) may be reflected back across the inputs to the two sets by means of an operational amplifier circuit (A3,A4) to obtain a ground referenced output voltage which is proportional to the accumulated base-emitter voltage differential between the two transistor sets (Q7-Q12, Q13-Q17).

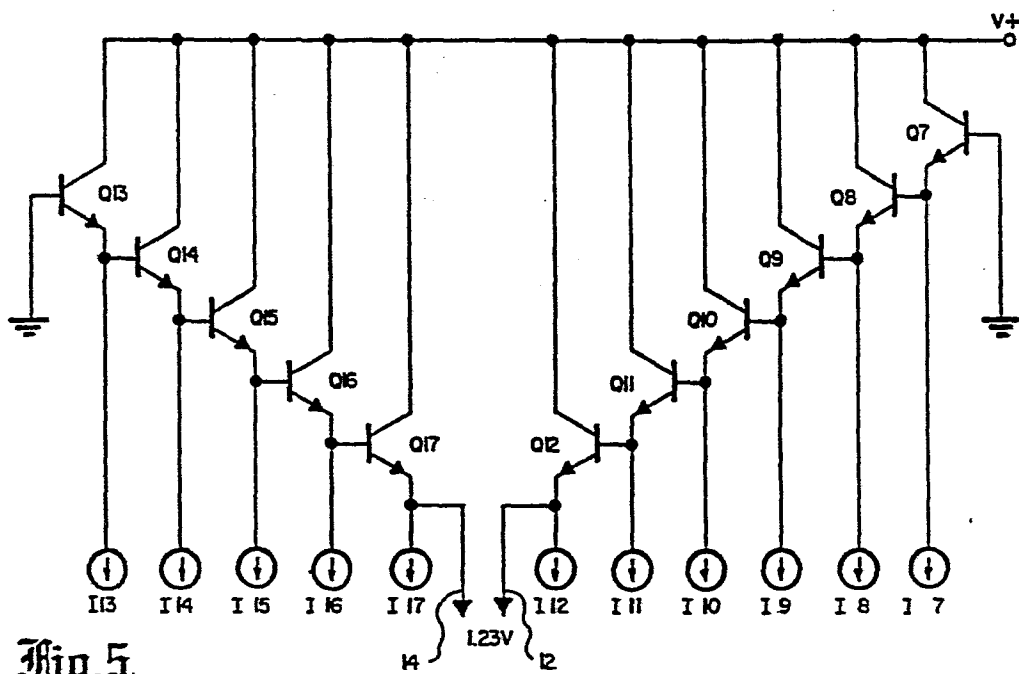


Fig. 5.

PRECISION BANDGAP VOLTAGE REFERENCE

5 This invention relates to integrated circuit bandgap voltage references, and more particularly to bandgap voltage references capable of being implemented with CMOS (complementary metal oxide semiconductor) processing techniques.

10

 Voltage references are required to provide a substantially constant output voltage irrespective of changes in input voltage, output current or temperature. Such references are used in many design applications, such as digital-to-analog
15 converters, power supplies, cold junction thermistor compensation circuits, analog-to-digital converters, panel meters, calibration standards, precision current sources and control set-point circuits.

 Modern voltage references are generally based on either
20 zener diodes or bandgap generated voltages. Zener devices characteristically exhibit high-power dissipation and poor noise specifications. Bandgap voltage references, on the other hand, are designed to yield stable output voltages over temperature by summing a pair of voltages with negative and
25 positive temperature coefficients. A voltage with a negative temperature coefficient is obtained from the base-emitter junction of a transistor, while a voltage with a positive temperature coefficient is obtained from the difference between the base-emitter voltages of two transistors operating
30 with unequal current densities. When the differential voltage is amplified and added to the base-emitter voltage of the first transistor, a voltage level with a low temperature coefficient results if the sum is equal to 1.23 volts, which is close to the bandgap voltage of silicon. The 1.23 volt
35 level is then amplified to provide stable output voltages of typically 5.0 and 10.0 volts.

 A typical bipolar transistor or diode has a base-emitter voltage when the device is on of about 600mV, and a negative temperature coefficient of about -2mV/°C. The positive tem-
40 perature coefficient voltage obtained from the difference

between the base-emitter voltages of two transistors is typically about 60mV at 25°C if the current densities of the two transistors are in a 10:1 ratio, and has to be amplified before being added to the base-emitter of the first transistor in order to achieve a 1.23 voltage level. The 60mV differential might be increased up to about 200 mV for larger but less practical devices, but amplification would still be required.

An early bandgap voltage reference is described in an article by R. Widlar in IEEE J. Solid State Circuits, Vol. SC-6, pages 2-7, February, 1971. Currently, a more common circuit is one developed by Paul Brokaw and described in an article entitled "A Simple Three-Terminal IC Bandgap Reference", IEEE J. Solid State Circuits, Vol. SC-9, pages 383-93, December, 1974. The basic approach taken in this circuit is illustrated in FIG. 1, in which a pair of bipolar transistors Q1 and Q2 have their collectors connected through resistors R1 and R2, respectively, to a positive voltage bus V+ and their bases connected in common to provide a 1.23 volt reference. The collectors of Q1 and Q2 are also connected to respective inputs to an operational amplifier A1, the output of which is connected to the voltage reference output. The emitters of Q1 and Q2 are connected to opposite sides of resistor R3, while the emitter of Q2 is also connected through resistor R4 to ground. Q1 and Q2 are forced to run at different current densities by scaling the geometry of Q1 larger than that of Q2, by making R1 larger than R2, or both (a larger transistor geometry or a smaller through-current will each lead to a smaller current density). A voltage differential thus appears across R3, producing a temperature proportional current which also flows through R4. By a suitable choice of R3 and R4 an arbitrary voltage can be created across R4 which is temperature proportional. The R4 voltage is added to the base-emitter voltage of Q2, producing a relatively stable reference output.

While the FIG. 1 circuit can be implemented with standard bipolar processing, it unfortunately is not readily adaptable to CMOS processing techniques which are presently becoming very widespread. In CMOS processing the transistor collectors are formed from the substrate, which is held at V+; R1 and R2 would thus be shorted out if FIG. 1 was implemented using CMOS

processing. Extra process steps could be added to get around this problem, but this would be a costly alternative,

The standard P-well CMOS process has available parasitic NPN bipolar transistors, but the collectors are not individually accessible and are all connected to V+. Such a transistor is illustrated in FIG. 2. It is fabricated using an N+ (heavily doped) source/drain diffusion 2 as the emitter, the P well 4 accessed through a P+ diffusion 6 as the base, and the N- (lightly doped) substrate 8 accessed through an N+ diffusion 10 as the collector. The polarities of the various components would be reversed for an N-well CMOS process.

Several alternative arrangement of the FIG. 1 circuit have been proposed or used to form a CMOS voltage reference using parasitic bipolar transistors such as that illustrated in FIG. 2. One such arrangement is shown in FIG. 3. In this circuit the collectors of transistors Q3 and Q4 are connected directly to V+, and their bases are connected to the 1.23 volt reference output. The emitter of Q3 is connected to a resistive voltage divider circuit consisting of series connected resistors R5 and R6, while the emitter of Q4 is connected to a resistor R7; the opposite sides of R6 and R7 are both grounded. An operational amplifier A2 has its inputs connected respectively to the emitter of Q4 and to the junction of R5 and R6, and its output connected to the voltage reference output. Amplifier A2 directly amplifies the differential base-emitter voltage term appearing across R5, and forces the output reference voltage in a manner similar to the FIG. 1 circuit. Different current densities are provided for Q3 and Q4 by making Q3 larger than Q4, R6 larger than R7, or both.

One problem with the FIG. 3 circuit is in the required precision for amplifier A2. Even if the current densities in Q3 and Q4 differ by a factor of 100, which is probably about the limit of practicality, only about 120mV appears across R5. Since A2 is fabricated with MOS devices, it could have an input offset as high as 20mV even with a careful design. This would produce about a 16% error in the base-emitter voltage differential term (20mV/120mV) and about an 8% error in the output reference voltage. Additionally, the temperature coefficient of the offset voltage is not predictable and can cause the output voltage to drift with temperature.

One method of improving on the circuit of FIG. 3 involves stacking NPN transistors to increase the base-emitter voltage differential term. This approach is illustrated in FIG. 4, in which the bases of transistors Q3 and Q4 are shown connected to the emitters of transistors Q5 and Q6, respectively, and the collectors of all four transistors are connected to V+. Resistors R5, R6 and R7 together with operational amplifier A2 are connected to the emitters of Q3 and Q4 as in FIG. 3, but the voltage reference output is connected to the bases of Q5 and Q6, rather than to Q3 and Q4. The bases of the two latter transistors are held above ground by resistors R8 and R9, respectively. Again, the geometric scaling of Q3 and Q4 and the resistance ratio of R6 and R7 are selected to produce different current densities in Q3 and Q4. In addition, Q5, Q6 and R8, R9 are scaled in a similar manner to Q3, Q4 and R6, R7 to produce different current densities in Q5 and Q6. The result is a doubling of the differential base-emitter voltage term across R5, which halves the overall error. Unfortunately, the voltage differential between the inputs to A2 now involves the base-emitter voltages of four transistors rather than two, causing the base-emitter voltage term to double along with the doubling of the base-emitter differential voltage term. This produces an output reference of 2.46 volts, which may be too high for many applications. Furthermore, the halving of the error which this circuit produces is not a sufficient improvement for many purposes.

In view of the foregoing problems associated with the prior art, is an object of this invention to provide a novel and improved bandgap reference voltage circuit which has a very low error term in its output reference voltage.

Another object is the provision of such a bandgap voltage reference circuit which is compatible with both bipolar and CMOS processing techniques.

In the accomplishment of these and other objects of the invention, a bandgap voltage reference circuit is provided which includes first and second sets of bipolar transistors connected to accumulate the base-emitter voltages of each set, and means for transmitting respective current flows through

the collector-emitter circuits of each of the transistors. The number of transistors in each set, the geometry of each transistor and the currents transmitted through the various transistors are selected such that the accumulated base-emitter voltages of the first and second sets differ by an amount corresponding to a predetermined bandgap voltage. Output means are connected to present the accumulated base-emitter voltage differential between the two transistor sets as a high precision reference voltage.

In a preferred embodiment the first transistor set includes one more transistor than the second set. Individual current sources are provided for each transistor in each set, with the currents through the transistors of the first set being larger than the currents for the second set. The second set transistors are scaled larger than the first set transistors. Therefore, the current densities through the transistors of the first set exceed the current densities of the second set. The result is a greater base-emitter voltage for each transistor in the first set, and an accumulated base-emitter voltage differential between the two sets of 1.23 volts. If the circuit elements used are formed from a typical CMOS process, a difference in current densities of about 100:1 will normally be required. This is readily achieved by making the currents in the first set of transistors ten times larger than those in the second set, and making the emitters of the second set ten times larger in area than those in the first set. If the circuit elements are formed from a typical bipolar process the imbalance in current densities is likely to be closer to 50:1. This is because the V_{be} of a bipolar process transistor is some 90mV greater than a CMOS parasitic bipolar transistor, due to a higher general level of doping. The 50:1 ratio can be achieved in a similar fashion, with a 7:1 scaling in currents and a 7:1 scaling in emitter areas.

With the bases of the first transistor in each set grounded, the bandgap reference may be taken directly from the voltage differential between the emitters of the last transistors in each set. Alternately, if a ground reference is desired, the emitters of the last transistors in each set may be connected to respective inputs of an operational amplifier. This forces the accumulated base-emitter voltage differentials

between the two sets to appear across the bases of the first transistors in each set. The bases of those transistors are then connected in circuit with another operational amplifier and a ground referenced voltage divider circuit to produce a ground referenced bandgap output.

Another alternate embodiment when the circuit is produced by a bipolar process involves connecting the transistors of both sets as diodes and providing single current sources for each set, thus eliminating all but two of the current sources.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description of preferred embodiments, taken together with the accompanying drawings, in which:

FIG. 1 is a schematic diagram of a prior art bandgap reference circuit;

FIG. 2 is an enlarged cross-section diagram showing the presence of a parasitic bipolar transistor in a CMOS fabricated device;

FIGS. 3 and 4 are schematic diagrams of prior art bandgap voltage reference circuits that are compatible with CMOS processing techniques;

FIG. 5 is a schematic diagram of one embodiment of the present invention; and

FIGS. 6 and 7 are schematic diagrams of alternate embodiments of the invention.

A schematic diagram of a bandgap voltage reference circuit which has a considerably lower offset voltage error than in the prior art and is compatible with both bipolar and CMOS processing techniques is shown in FIG. 5. Six transistors, Q7, Q8, Q9, Q10, Q11 and Q12, are connected in succession with the emitter of each transistor except for the last transistor Q12 connected to the base of the next transistor. The collectors of each of the transistors are connected to a positive voltage bus V+, while their emitters are connected to respective current sources I7, I8, I9, I10, I11

and I12. The base of the first transistor Q7 is grounded, and the emitter of Q12 is connected to an output terminal 12.

A second set of transistors consisting of Q13, Q14, Q15, Q16 and Q17 is connected in succession on the left hand side of the circuit, with the emitter of each transistor in the second set except for the last transistor Q17 connected to the base of the next transistor. The collectors of each of the transistors are connected to positive voltage bus V+, and their emitters are connected to respective current sources I13, I14, I15, I16 and I17. The base of the first transistor Q13 in the second set is grounded, while the emitter of the last transistor Q17 is connected to an output terminal 14.

The first set of transistors Q7-Q12 includes one more transistor than the second set Q13-Q17, and thus the voltage at output terminal 12 will reflect one more base-emitter voltage drop than will the voltage at output terminal 14. In addition, the geometries of transistors Q7-Q12 are scaled smaller than the corresponding geometries of transistors Q13-Q17, and I7-I12 draw greater currents through the collector-emitter circuits of their respective transistors than do I13-I17. The result of both the size and current scalings is to produce current densities through Q7-Q12 which are larger than the current densities through Q13-Q17. This in turn makes the base-emitter voltage drop for each of Q7-Q12 greater than for Q13-Q17, which further increases the voltage differential between output terminals 12 and 14. The sizes of the current sources and the geometric transistor scalings are selected such that, taken together with the additional base-emitter voltage drop at output terminal 12, the voltage differential between output terminals 12 and 14 is the desired bandgap reference level of 1.23 volts. In this manner a bandgap reference voltage is achieved directly as a differential between two sets of transistors. The prior art requirement of amplifying a differential voltage, which also resulted in amplifying the error component associated with that voltage, is avoided.

The number of transistors employed in each set is somewhat arbitrary. The use of a larger number of transistors will reduce the geometric scaling ratio required, but will take up more area. Fewer transistors would reduce the

required area, but would increase the geometric scaling ratio. Regardless of the absolute number of transistors in each set, however, it is preferable that the first set have one more transistor than the second set. A base-emitter voltage term
5 is then added to a differential base-emitter voltage term to produce the desired temperature stable bandgap reference.

With bipolar fabrication techniques, in which base-emitter voltage drops are typically in the range of 0.65-0.75 volts, scaling transistors Q13-Q17 larger than transistors
10 Q7-Q12 by a factor of approximately 7 and making current sources I7-I12 larger than current sources I13-I17 by a similar factor of approximately 7 will result in the desired 1.23 volt bandgap reference across output terminals 12, 14. In this case I7-I12 would each be about 14.3uA, and I13-I17 would
15 each be about 100uA. For CMOS processing techniques, in which the base-emitter voltages are typically in the range of 0.55-0.65 volts, a somewhat more extreme area and current scaling is necessary to achieve a 1.23 volt differential output. For the circuit of FIG. 5, a scaling of approximately
20 10:1 for both transistor area and current will achieve the desired output for CMOS devices.

While the FIG. 5 circuit has a lower error component than prior art CMOS circuits, one disadvantage is that the reference voltage across output terminals 12, 14 is floating and
25 not referenced to ground. A variation of the circuit which provides an adjustable ground referenced output voltage is shown in FIG. 6. In this circuit Q7-Q17 and I7-I17 are implemented essentially as in the circuit of FIG. 5. However, instead of being taken directly as an output, the emitters of
30 Q12 and Q17 are connected to the inputs of an operational amplifier A3. Since operational amplifiers act to equalize the voltages applied to their inputs, the effect of this connection is to substantially equalize the emitter voltages of Q12 and Q17, and force the former output of 1.23 volts to
35 be reflected back through the two transistor sets as a voltage differential between the bases of the first transistors Q7 and Q13 of each set. Instead of being grounded as in the FIG. 5 circuit, the bases of Q7 and Q13 are connected respectively to an output terminal 16, and to the inverting input of another
40 operational amplifier A4, with the output of A3 connected in

common with the base of Q13 to the inverting input of A4. In addition to its connection to output terminal 16, the base of Q7 is connected to the output of A4 and to one end of a voltage divider circuit consisting of series connected resistors R10 and R11. The non-inverting input to A4 is taken from an intermediate point 18 in the voltage divider circuit at the junction of R10 and R11.

The action of A4 is to raise the voltage at output terminal 16 until the base voltage of Q13 is equal to the voltage at junction 18, thus causing the two inputs to A4 to equalize in voltage. Accordingly, the 1.23 volts established between the bases of Q7 and Q13 also appears across R10. Under these conditions the output voltage at terminal 16 is ground referenced and equal to $1.23V \times (R10+R11)/R11$. This circuit has the added advantage that a more precise output voltage can be obtained than in the prior art even if amplifiers A3 and A4 are not as accurate as the amplifiers employed in prior circuits, since A3 and A4 amplify 1.23 volts rather than a much smaller voltage as in the prior art.

Another embodiment of the invention which is particularly adapted for a bipolar fabrication process is shown in FIG. 7. In this embodiment two sets of transistors are provided in a manner similar to the FIG. 5 circuit. The first set consists of nominally six transistors Q18, Q19, Q20, Q21, Q22 and Q23, while the second set consists of nominally five transistors Q24, Q25, Q26, Q27 and Q28. The emitter of each transistor except for the last one in each set is connected to the base of the following transistor, as in FIG. 5. However, each of the transistors in FIG. 7 functions as a diode by having its collector shorted to its base. The bases of the first transistor in each set Q18 and Q24 are no longer grounded, but rather are connected along with their collectors to V+. The transistors of each set are connected in series, with only the first transistor of each set connected to V+.

With this embodiment all but two of the current sources can be eliminated, thus considerably simplifying the circuitry. One current source I18 is connected to the emitter of Q23 and draws current through each of the transistors Q18-Q23, while another current source I19 is connected to the emitter of Q28 and draws current through each of the transistors

Q24-Q28. The geometric scalings of the transistors and the two current sources are selected as in the circuit of FIG. 5 to establish a bandgap reference voltage of 1.23 volts across output terminals 20 and 22 at the emitters of Q23 and Q28, respectively.

Various embodiments of a novel and improved bandgap voltage reference circuit which is highly accurate and can be implemented with both bipolar and CMOS processes have thus been shown and described. Numerous modifications and alternate embodiments will occur to those skilled in the art. For example, the circuitry can be fabricated with an N-well CMOS process merely by reversing the polarities of the various circuit elements, and such an implementation should be considered as being equivalent to the specific circuits shown. Accordingly, it is intended that the invention be limited only in terms of the appended claims.

CLAIMS:

1. A bandgap voltage reference, comprising:
a first set of bipolar transistors (Q7-Q12) mutually connected to accumulate their base-emitter voltages,
a second set of bipolar transistors (Q13-Q17) mutually connected to accumulate their base-emitter voltages,
means (I7-I17) for transmitting respective current flows through the collector-emitter circuits of each of the transistors (Q7-Q17),
the number of transistors in each set, the geometry of each transistor and the currents transmitted through the collector-emitter circuits of the various transistors being selected so that the accumulated base-emitter voltages of the first (Q7-Q12) and second (Q13-Q17) sets differ by an amount corresponding to a predetermined bandgap voltage, and
output means (I2,I4) connected to present the accumulated base-emitter voltage differential between the first (Q7-Q12) and second (Q13-Q17) transistor sets as a reference voltage.

2. The bandgap voltage reference of claim 1, wherein the first set of transistors (Q7-Q12) includes one more transistor than the second set of transistors (Q13-Q17), and the transistor geometries and current transmitting means (I7-I17) are selected to produce higher current densities and correspondingly higher base-emitter voltages for the transistors in the first set (Q7-Q12) than for the second set (Q13-Q17).

3. The bandgap voltage reference of claim 1, wherein the accumulated base-emitter voltage differential between the first (Q7-Q12) and second (Q13-Q17) transistor sets is substantially equal to 1.23 volts.

4. The bandgap voltage reference of claim 1, wherein the various circuit elements are bipolar process fabricated, the transistors (Q7-Q17) of both sets are diode connected, and the current transmitting means comprises first and second current sources (I18,I19) connected to transmit respective currents through the first (Q7-Q12) and second (Q13-Q17) transistor sets, respectively.

5. The bandgap voltage reference of claim 1, wherein the transistors of each set are connected with their base-emitter circuits in series from first (Q7,Q13) to last (Q12,Q17) transistors within each set, the bases of the first transistors (Q7,Q13) in each set are grounded, and the output means (12,14) is connected to the emitters of the last transistors (Q12,Q17) in each set to present the voltage differential therebetween as a reference voltage.

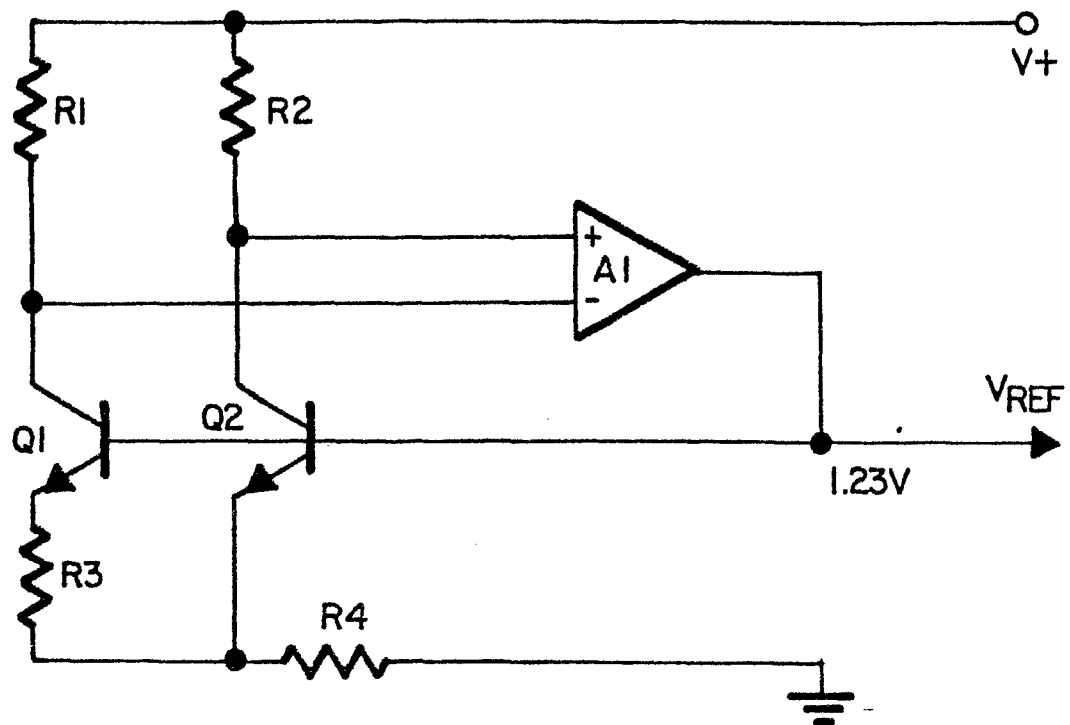
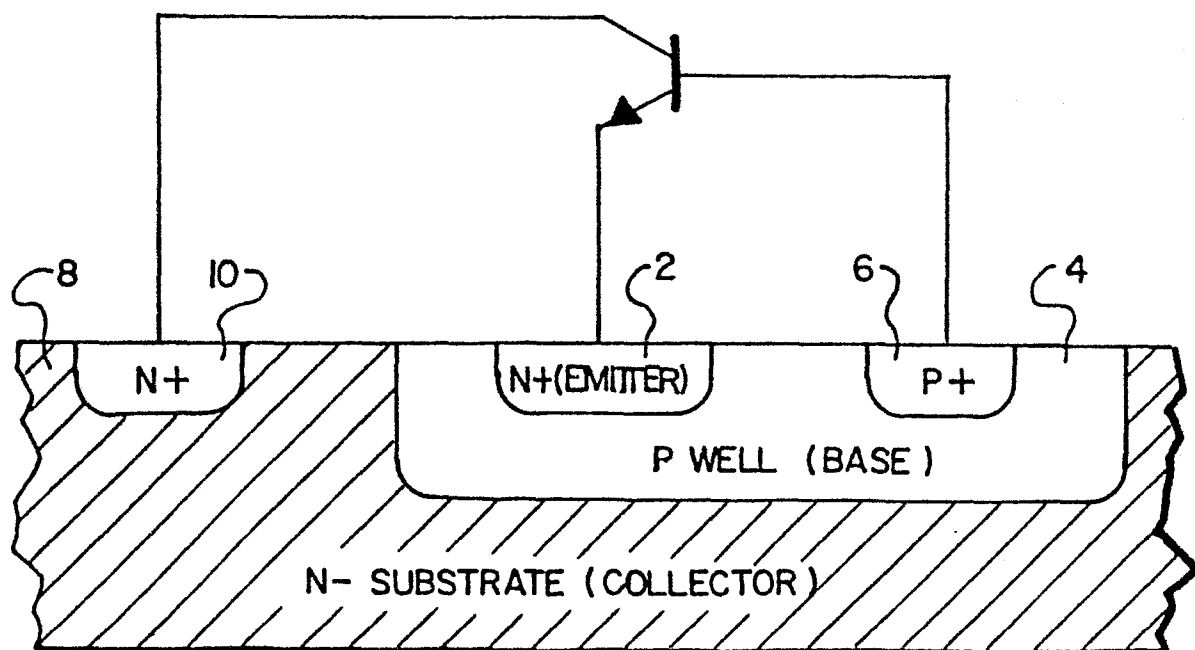
6. The bandgap voltage reference of claim 1, wherein the transistors of each set (Q7-Q12, Q13-Q17) are connected with their base-emitter circuits in series from first (Q7,Q13) to last (Q12,Q17) transistors within each set, further comprising:

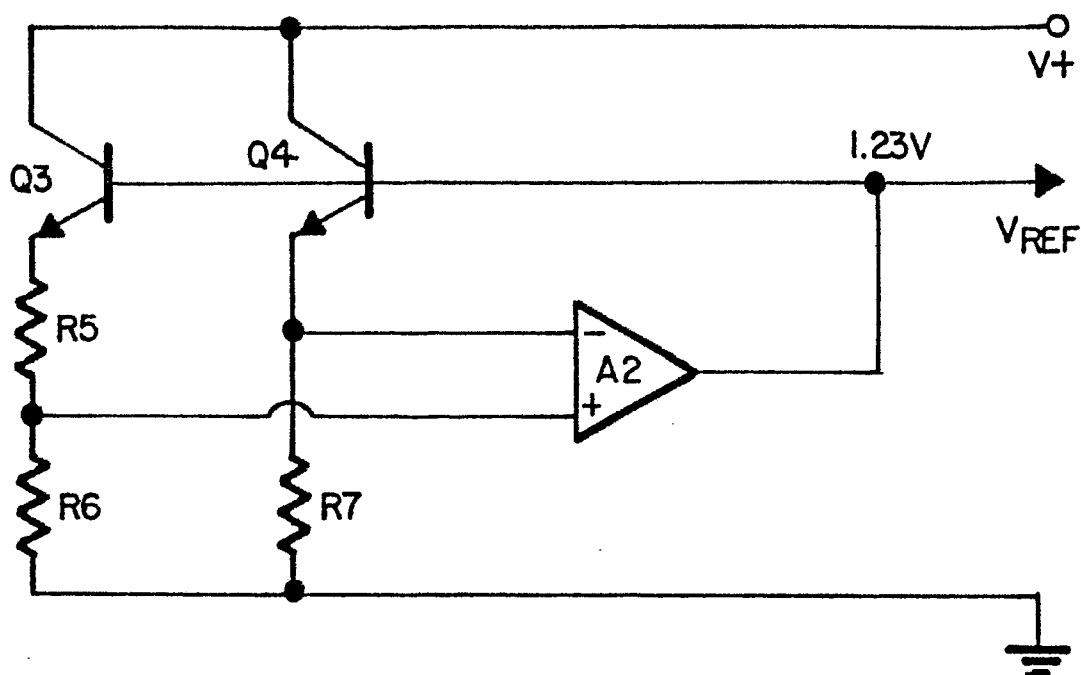
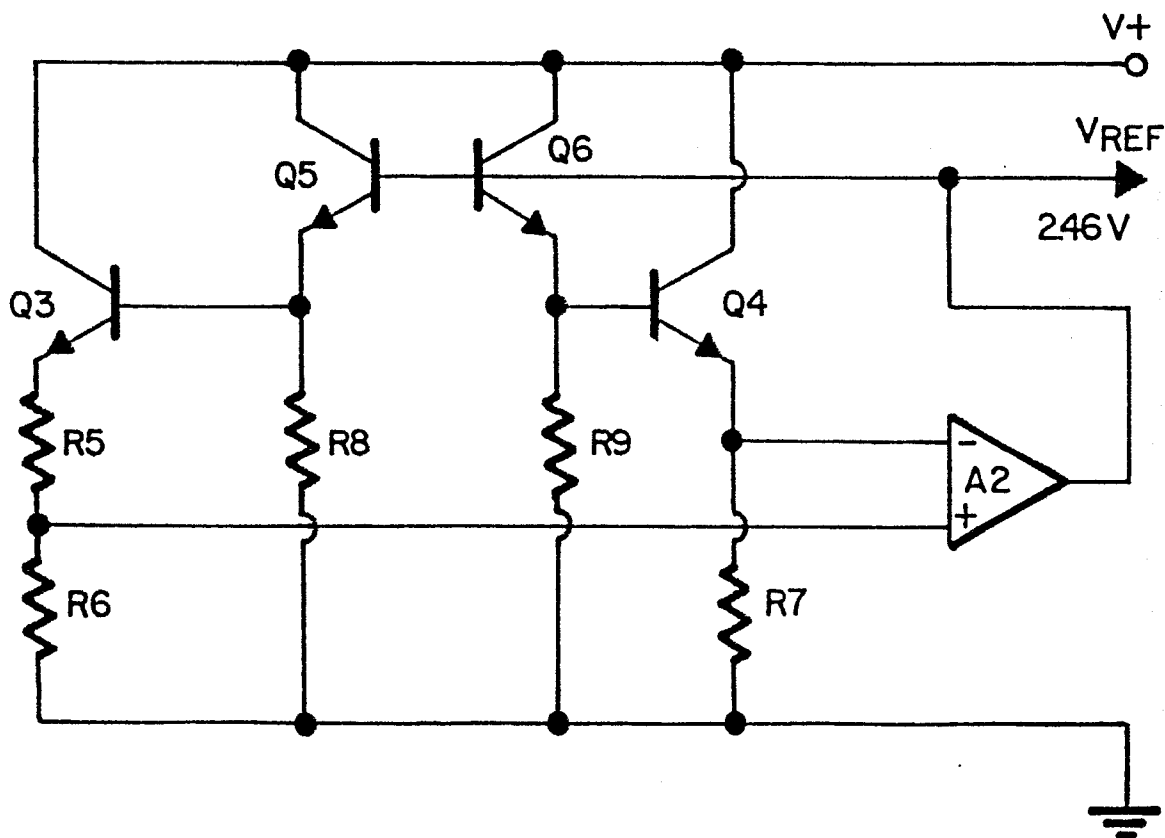
a) a first operational amplifier (A3) having its inputs connected to the emitters of the last transistors (Q12, Q17) in each set, thereby forcing the emitter voltages of those transistors (Q12,Q17) to substantially equalize and reflect the accumulated base-emitter voltage differential between the two sets (Q7-Q12, Q13-Q17) as a voltage differential between the bases of the first transistors (Q7,Q13) in each set,

b) a ground referenced voltage divider circuit (R10, R11) connected to the base of the first transistor (Q7) in the first set, and

c) a second operational amplifier (A4) having one input connected to the base of the first transistor (Q13) in the second set, its other input connected to the voltage divider circuit (R10,R11), and its output connected to the base of the first transistor (Q7) in the first set and to an output terminal (16), whereby a ground referenced voltage is established at the output terminal (16) which is proportional to the accumulated base-emitter voltage differential between the two transistor sets (Q7-Q12, Q13-Q17).

1/5

**Fig.1. (PRIOR ART)****Fig.2. (PRIOR ART)**

**Fig. 3. (PRIOR ART)****Fig. 4. (PRIOR ART)**

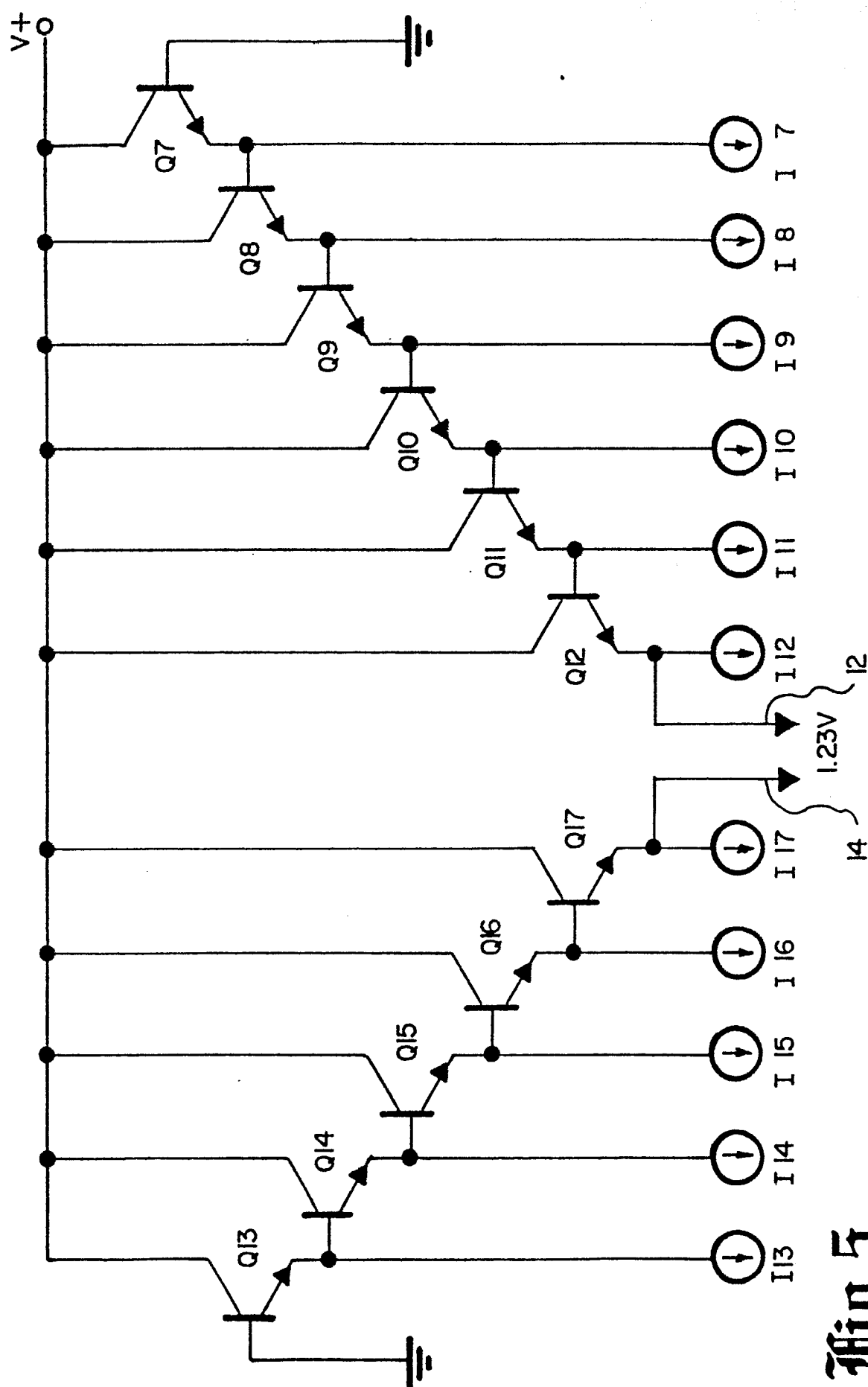


Fig. 5.

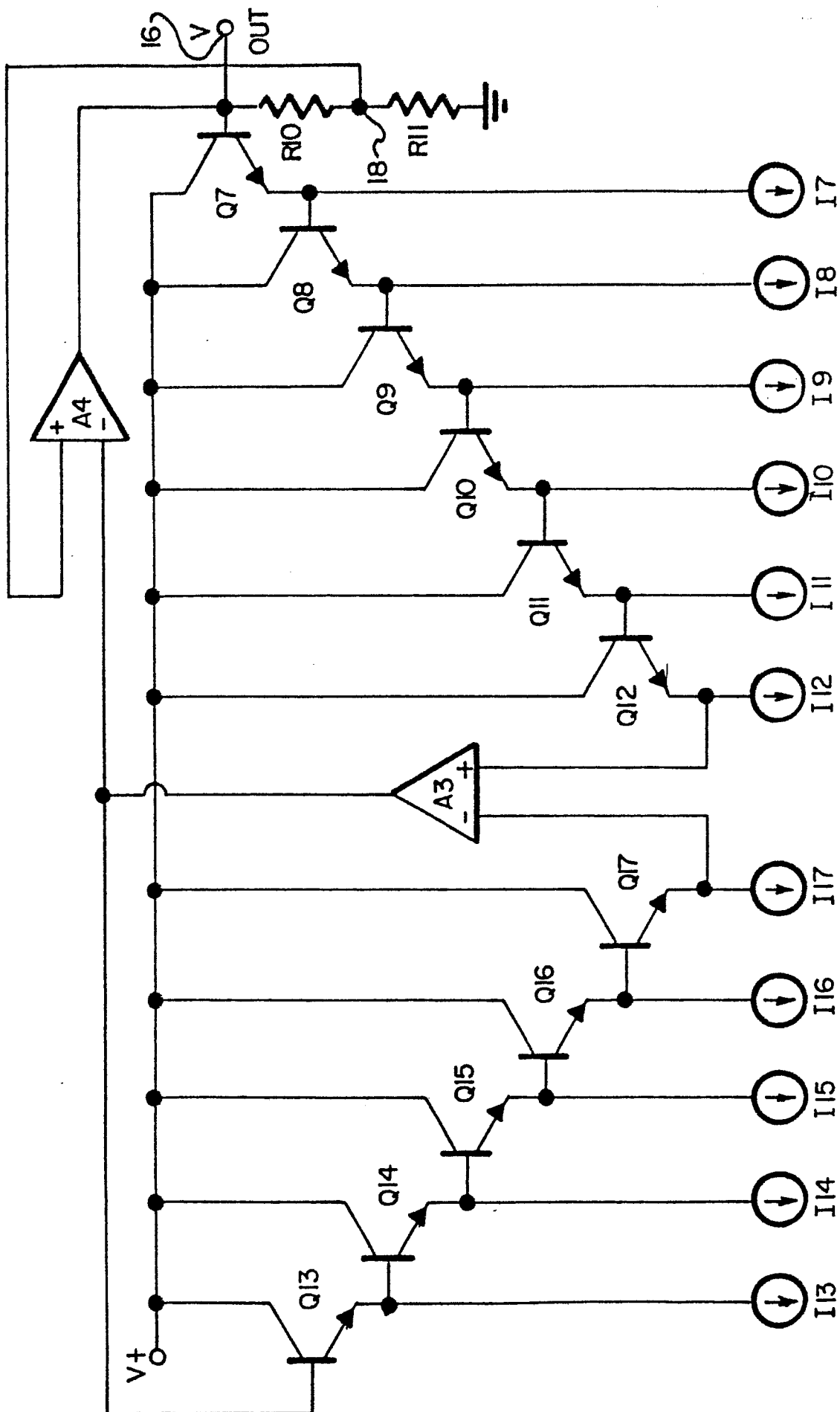


Fig. 6.

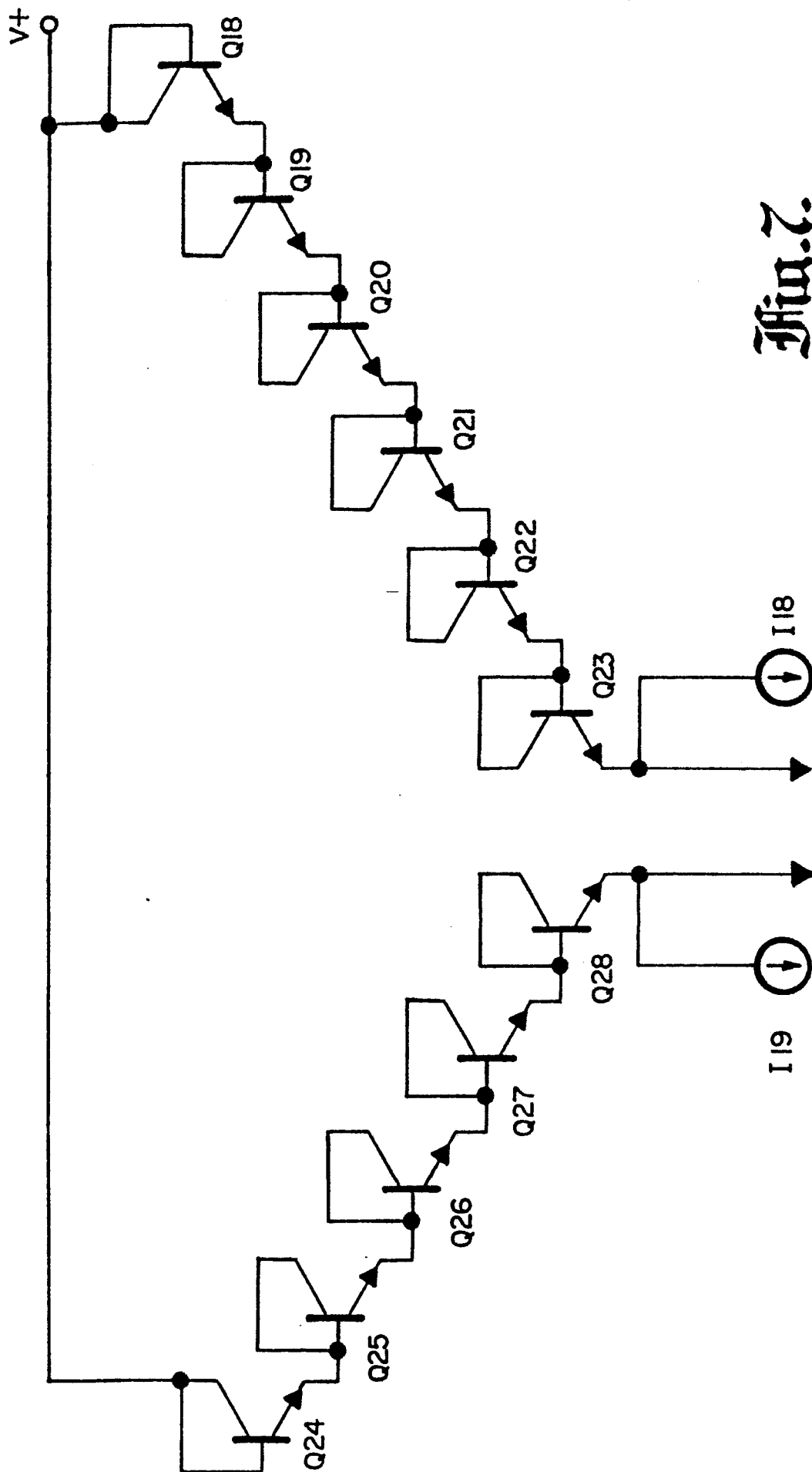


Fig. 7.



European Patent
Office

EUROPEAN SEARCH REPORT

0199427

Application number

EP 86 30 0299

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
X	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.SC-17, no. 6, December 1982, pages 1139-1143, IEEE, New York, US; G.C.M. MEIJER et al.: "A new curvature-corrected bandgap reference" * Figure 16 *	1-4	G 05 F 3/30
A	US-A-4 224 537 (MOTOROLA) * Figure 1; abstract *	1	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.SC-8, no. 3, June 1973, pages 222-226, IEEE, New York, US; K.E. KUIJK: "A precision reference voltage source" * Figures 2,6 *	1	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.SC-19, no. 6, December 1984, pages 892-899, IEEE, New York, US; B.K. AHUJA et al.: "A programmable CMOS dual channel interface processor for telecommunications applications" * Figure 6 *	1	G 05 F 3/00
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 06-06-1986	Examiner ZAEGEL B.C.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			



European Patent
Office

EUROPEAN SEARCH REPORT

0199427

Application number

EP 86 30 0299

Page 2

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
A	PATENTS ABSTRACTS OF JAPAN, vol. 8, no. 137 (P-282) [1574], 26th June 1984; & JP - A - 59 36 826 (NIPPON DENKI K.K.) 29-02-1984 * Whole abstract * -----	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 06-06-1986	Examiner ZAEGEL B.C.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			