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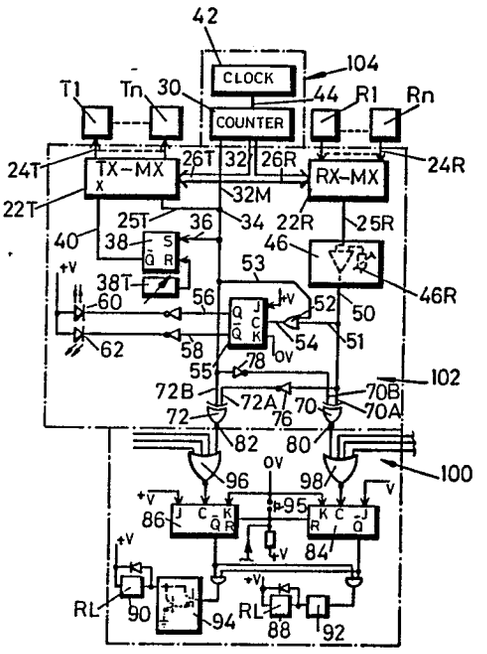
(71) Applicant: **Hughes, John Peter, 9 Ash Tree Drive, Little Neston Wirral (GB)**
Applicant: **Fletcher, Brian Dows, 89 West Vale, Neston Wirral (GB)**

(72) Inventor: **Hughes, John Peter, 9 Ash Tree Drive, Little Neston Wirral (GB)**
Inventor: **Fletcher, Brian Dows, 89 West Vale, Neston Wirral (GB)**

(74) Representative: **Dodd, David Michael, ROYSTONS 531 Tower Building Water Street, Liverpool L3 1BA (GB)**

(54) Guard system.

(57) Guard system for protecting some space against undetected intrusion uses a plurality of wave beam paths (from transmitter T1-Tn to receivers R1-Rn) selectively energised in cycles (multiplexer Tx-Mx) so that each beam (transmitters T1-Tn) is energised for part only of each cycle. Pressure or absence of beam energy indicative of intrusion is monitored (receivers R1-Rn and multiplexer Rx-Mx). Signal level discrimination (46) of received signals operates both logic circuitry (flipflop 55) to give effectively continuous output (56, 58) except for beam interruption (52) even through a quiescent state of each cycle, and fault indication logic circuitry (100 via 70, 72) that is shown duplicated.



Title: Guard System

DESCRIPTION

This invention relates to guard systems in which some space requires protection against undetected intrusion as applies, for example, at work stations of machines where danger can arise from intrusion of parts of operators' bodies and/or clothing, and at displays of valuable goods such as jewellery.

At least in relation to machine guards, it is known to set up so-called curtains or screens of beamed wave energy, usually electromagnetic, making a plurality of crossings of an entry position to the protected space. Those crossings can be associated with a single beam that is subject to multiple reflection to and fro between sides of that position and between a transmitter and receiver, or with a plurality of beams each having an associated transmitter and receiver. This invention arises from particular consideration of systems of the latter type, i.e. to plural beam systems, and aims to provide a novel and advantageous manner of operation capable of competing with systems employing pulse code modulation

techniques in order to get self-checking of operation.

According to one aspect of this invention, plural wave beam paths are selectively energised in cycles at the end of each of which all such paths have been energised each for part only of that cycle during which receiving means is monitored for presence and/or absence of interruption to the path concerned. The cycle parts are preferably discrete and non-overlapping.

In one embodiment, the beam paths extend from an array of transmitters, one for each beam, and can then conveniently be associated, one-to-one, with a corresponding array of receivers. Suitable energising or enabling means for such transmitters and sampling for such receivers includes sequential enabling and/or routing means, and could be implemented as shift-register-type enables at least for digital circuitry, or multiplexer type routing at least for analogue circuitry. We actually prefer to use counter-driven circuitry including binary-to- "one-out-of-n" converter means.

One reason for that latter preference is the provision of means establishing phases of operation, preferably one per the above-mentioned cycle, in which transmission and/or reception are

quiescent, i.e. not enabled. Then, a complete cycle, i.e. including a quiescent phase, is readily controlled using a counter, specifically in response to achievement of a particular state of a cyclically operating counter. A particularly simple provision is for the number of required transmission/reception operating/sampling signals to be a binary power definable by least significant outputs of the counter, which then has a further, more significant, output for disabling or blocking response to the aforesaid transmitters/receivers, with the result that each complete cycle is divided into transmission/reception and quiescent parts, which would actually be of equal length. Such provision permits checking of the transmission/reception both as to its sequential operation and as to there being a correct quiescent state, and suitable logic circuitry is preferably incorporated to that end, say as a two-state circuit or flip-flop that times out if not refreshed by more-significant output-dependent signals at expected intervals. A corresponding output can then disable transmission, say by disabling binary-to-"one-out-of-n" converter means. In an analogue system a transmission multiplexer can serve to feed its outputs off said more-significant counter output.

Moreover, in further controlling sampling or routing for receiver inputs, again using binary-to-"one-out-of-n" converter means, it is a simple matter for the aforesaid least significant counter outputs to coordinate operation of transmitters and receivers so that that latter produce an output signal representing successive sampling or selection of normally operative beams. That output is readily discriminated as to signal level so as to detect interruption of any beam by absence of expected received signal. A suitable signal discriminator such as a comparator can produce output at logic signal levels suitable for Exclusive-ORing with the afore-mentioned more-significant counter output in order to produce a control signal that maintains its level (except for beam interruption), i.e. including through quiescent phases, but always responds to any one of more beam interruptions. We prefer effectively to duplicate that control signal using a pair of Exclusive-OR gates and true and inverted pairs of inputs thereto from the comparator and the more-significant counter output line.

In itself, and in conjunction with cyclic on-off transmitter operation and receiver sampling, Exclusive-

ORing of comparator and the counter's more-significant stage operates as a check on the operation of the transmitter/receiver control and comparator circuitry, plus, of course, the transmitters and receivers as such.

It is, however, found advantageous further to utilise the comparator output via a relaxation-type two-state device or flip-flop that requires such comparator output to stay in one of its states, otherwise defaulting to its other state. At envisaged repetition rates for cycles of transmitters/receivers, an indicator, such as a light emitting diode (LED) driven by either of complementary outputs of the two-state device will appear to an operator to be continuously energised. It is, however preferred for such complementary outputs each to drive a different indicator for visually checking operation up to the comparator means output.

Comparator-dependent output of the Exclusive-OR means, or each of them as we prefer, is readily used via latch or relay means to record intrusion by breaking of any aforesaid beam; or such latch or relay means is readily further used as desired, for example operating alarms, disables, etc. Moreover,

inclusion of OR-gate means between Exclusive-OR output and such latch or relay means allows more than one guard screen to operate the same latch or relay means, whether such multiple guard screens are associated with the same protected space or with different protected spaces.

Another aspect of this invention concerns the provision of a modular guard system wherein one set of circuitry for providing basic timing control signals, such as the aforementioned counter and associated clock pulse source, can serve a plurality of sets of guard screen control circuitry each operating on a cyclic basis relative to transmitters/receivers, and one set of fault response circuitry, such as the aforesaid OR-gate and latch/relay means, can serve a plurality of such sets of guard screen control circuitry. Significant practical advantage appears from each of those sets being a distinct system unit, for example on its own printed circuit board.

Specific implementation of this invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic indication of one

typical installation;

Figures 2A to 2C are diagrammatic side, bottom and end views of a particular installation; and

Figure 3 is a schematic circuit diagram of a guard system hereof.

In the drawings, referring first to Figure 1, the paper itself represents a plane bounding a space for which intrusion of any foreign body is to be detected. Accordingly, there may be a work station or display space in front or behind Figure 1. Shown spaced relative to opposed edges of the space, are spatially related arrays 12 and 14, at sides, though top and bottom could equally well be used, as could curved linear arrays even non-linear arrays. As illustrated, there is one-to-one correspondence between transmitters T1-Tn and receivers R1-Rn of the arrays 12 and 14, respectively, both as to their numbers and as to their spacings in relation to beam transmissions B1-Bn, respectively.

It is found particularly convenient for the transmitter and receiver arrays to be fabricated as slides or trolleys 16 fixed in tracks 18. Then, the spacings of the transmitter and receivers in each array can be accurately set at manufacturing

tolerances, and the trolleys 16T and 16R simply located and clamped or braked, or otherwise held, in their tracks 18T and 18R on site for best results.

Actual spacings of transmitters, or at least receivers, is dependent both on site requirements (for maximum) and on beam spread/signal discrimination capability (for minimum). We can also offset the order of energisation, see also below.

Figure 2 shows a frame 20 with front and rear uprights 20F and 20R and a horizontal upper 20U, all hollow to take trolleys 16' that can be self-locating interference fits therein via spring leaves 16S and take arrays of transmitters (T) and/or receivers (R) revealed by slots in the faces to which arrows A point. It should be clear that two such frames 20 in spaced relation, with confronting sides as shown in Figure 2A, readily permit of setting up wave beam screens at front, top and both sides of a cuboid space to be protected, the trolleys 16' then having suitable combinations of transmitter and receiver arrays, shown for the front upright 20F as one of each, but not necessarily so.

Turning to Figure 3, multiple input/output blocks 22T and 22R represent control circuitry for

transmitters T1-T$\underline{n}$, and receivers R1-R$\underline{n}$, respectively, with outputs 24T for transmitter drive signals and inputs 26T for transmitter select signals (actually for routing a signal on input 25T), and inputs 24R and 26R form receivers and for receiver selection, respectively, and output 25R for the enabled receiver input. As shown, of course, the blocks 22T and 22R are of analogue multiplexer type operative sequentially relative to their lines 24 one at a time in successive cycles covering all of them. Whilst convenient to view the lines 24 as sequentially energised/sampled left-to-right or right-to-left, it will be appreciated that connections to the actual transmitters T and receivers R can be so as to minimise any effects of beam spread, say in the sequence 1, $\frac{1}{2}\underline{n}$ + 1; 2, $\frac{1}{2}\underline{n}$ + 2; ..... $\frac{1}{2}\underline{n}$, $\underline{n}$ for even $\underline{n}$ as applies for our preferred powers of two as the numbers of transmitters and receivers.

The multiplexers 22 are indicated as being of binary-to- "one-out-of" type, with inputs 26 branched from outputs 32 of all but the most significant stage of a counter 30. Three such lines 32 will control eight-way transmitter/receiver arrays, four will control sixteen-way etc. The most significant bit output line 32M from the counter 30 is used to set aside

one half of a complete operating cycle as quiescent, see its application at branch node 34 to supply input 25T of the transmit multiplexer 22T. Another branch 36 of the line 32M goes to a two-state device 38 as a missing pulse detector that is put to one state by input pulses, see to its set input (S), and goes to its other state automatically after a predetermined time delay, see variable timer box 38T connected to its reset input R. Setting such time delay to be longer than one interval between changes of the state of line 32M, but less than double that interval, enables checking that the counter 30 is cycling properly. Output 40 from the two-state device 38 is shown taken to an inhibit terminal of the transmit multiplexer 22T.

The counter 30 is itself driven by a suitable clock pulse generator 42 over line 44. The frequency of clock pulses is required to be between limits set effectively by response times of the transmitters T1-Tn and by the required repetition rate for multiplexed part-cycles of energisation of the transmitters T1-Tn in order to give the required security. A complete cycle time, i.e. each multiplexed traversal of the transmitter/receivers plus related quiescent period, of 20 milliseconds or less is found to be

satisfactory.

Outputs from the receivers R1-Rn are sampled sequentially over line 25R and applied to a detection circuit 46 shown as a comparator operative relative to signals on 25R at one input and a preset reference at its other input, see variable resistor 46R. Output 50 of the detection circuit 46 should go high for successive receiver samples on line 25R until a beam is broken. It is thus convenient to use signals on the line 50 in a manner similar to signals on line 32M, i.e. to check that they appear at the expected intervals whilst all the beams are uninterrupted. Accordingly, line 50 is shown branched at 51 to Exclusive-OR gate 52 also receiving branch 53 from line 32M and supplying its output 54 to the clocking input of a J-K flip flop 55 which will drop from its "up" state only if not clocked sufficiently frequently. Its "up" and "down" outputs (Q and $\overline{Q}$) are shown at 56 and 58 to indicators, actually light emitting diodes 60 and 62 and shown via inverters for LED's poled as shown. The LED's will, of course appear to an operator to be permanently lit at the above-indicated repetition rate.

Effectively, then, the circuit 38 checks inputs to the multiplexer 22T, and the circuit 55 drives display of the system status. The advantages of

that will become apparent from the modularity provisions described below.

First, however, it is convenient to mention that a digital configuration of circuitry equivalent to that of Figure 3 could work off a single binary-to-"one-of-out-n" converter then with suitable sampling circuitry for the receiver lines 24R enabled by logic level signals.

Also, reference is made to the use of duplex logic circuitry intended to assure reliability of production of signals truly equivalent to output 50 and used for warning etc. purposes. Thus, two Exclusive -OR gates 70 and 72 each have two inputs 70A, 70B and 72A, 72B. Of those inputs, first ones 70A, 72A are fed from the comparator output 50 with one (72A) inverted at 76, and others 70B, 72B are fed from line 32M also with one (70A) inverted at 78. The net result is, of course, that both Exclusive -OR gates should produce the same output and go low in normal operation only if there is an interrupted beam, i.e. at detection of unwanted intrusion. Effectively, the Exclusive -OR gates provide a check on the output of the detector 46.

Outputs 80, 82 of the Exclusive -OR gates 70, 72 go to latches shown including J-K flip-flops 84, 86 further shown dually operating relays 88, 90 via

drive circuits 92, 94 such as including suitable transistor pairs, see dashed. Clearly, suitable latches could equally well be other types of electrónic circuits or relays requiring a reset (see button 95) once operated by detection of a beam interruption. The outputs 80, 82 are shown going via OR-gates 96, 98 with other inputs that can usefully serve for similar Exclusive-OR gate outputs from other similar guard screens, such as those of the top and sides of the frames 20 of Figure 2.

That leads naturally to our advantageous preference for modularity via one unit 100 as an interface board capable of serving several multiplexing control units 102 themselves fed with timing control signals from a common unit 104, such units usually comprising printed circuit boards.

CLAIMS

1. Guard system for protecting a space against undetected intrusion, comprising, across or over access to said space, a plurality of selectively energisable wave beam paths; means for energising those paths in cycles, each such path being energised for part only of each cycle; and means for monitoring reception of energy from said paths according to its presence of absence.

2. Guard system according to claim 1, wherein the means for energising is operative to energise said paths for discrete and non-overlapping parts of said cycle.

3. Guard system according to claim 1 or claim 2, wherein said paths extend from an array of energy transmitters, one for each beam, to a corresponding array of energy receivers associated with the monitoring means.

4. Guard system according to claim 3, comprising sequential enabling means for said transmitter and sequential sampling means for said receivers.

5. Guard system according to claim 4, wherein the sequential enabling means and the sequential sampling

means include multiplexer type routing means.

6. Guard system according to claim 5, wherein said multiplexer means comprises counter driven circuitry including binary-to-one-out-of-n converter means.

7. Guard system according to any preceding claim, wherein each said cycle includes a quiescent phase during which no said paths are energised.

8. Guard system according to claim 7, wherein the monitoring means includes signal level discrimination means and logic gating for maintaining a control signal level in the absence of any detected beam interruption which signal level persists through beam energisation cycling and through said quiescent phase.

9. Guard system according to claim 8, wherein said logic gating produces duplicate said control signals.

10. Guard system according to claim 8 or claim 9, further comprising a relaxation two-state device responsive to said discrimination means to default to an intrusion indication state if not held to its other state by successive signals thereat.

11. Guard system according to claim 10, comprising light means driven from said two-sate device, said cycle parts being at a fast enough repetition rate for the light means to appear continuously energised unless there is intrusion and loss of energy reception from

at least one said beam.

12. Guard system according to claim 10, comprising duplicate light means driven from complementary outputs of said two-state device.

13. Guard system according to claim 8 or claim 10, comprising latch means to record intrusion by breaking of any said beam.

14. Guard system according to claim 13, comprising logic circuitry permitting the same said latching means to be operative relative to different pluralities or sets of said beams.

15. A guard system according to any preceding claim of modular construction, comprising one set of circuitry providing basic timing control signals can serve a plurality of sets of guard screen control circuitry each operating on a cyclic basis relative to transmitters/receivers for its plurality of beams, and one set of fault response circuitry which also can serve said plurality of sets of guard screen control circuitry.

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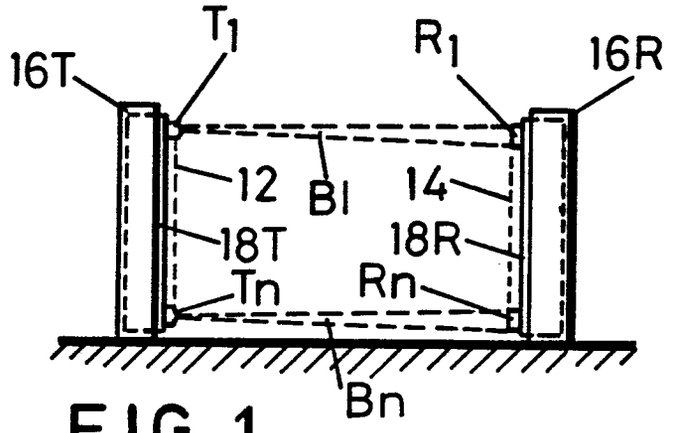

FIG. 1

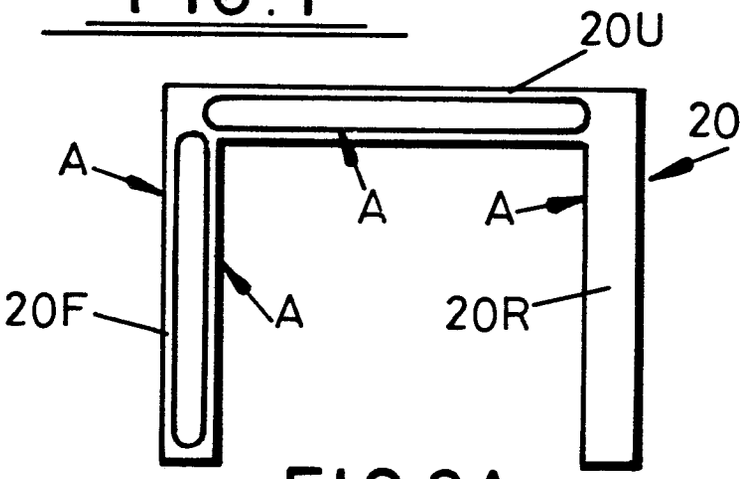

FIG. 2A

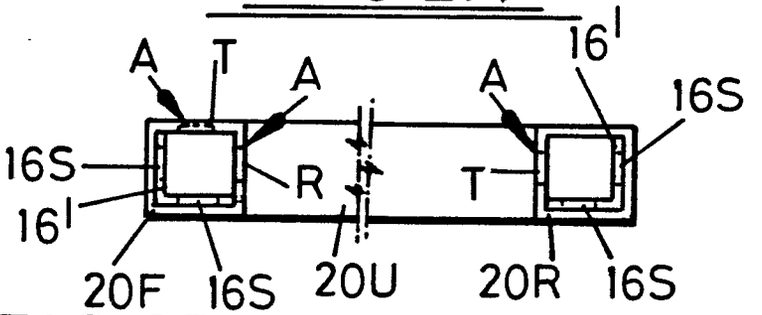

FIG. 2B

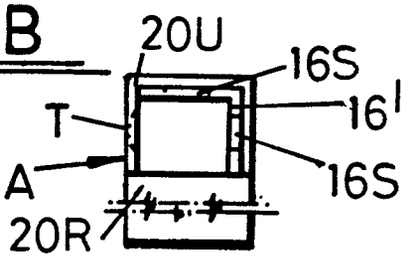

FIG. 2C

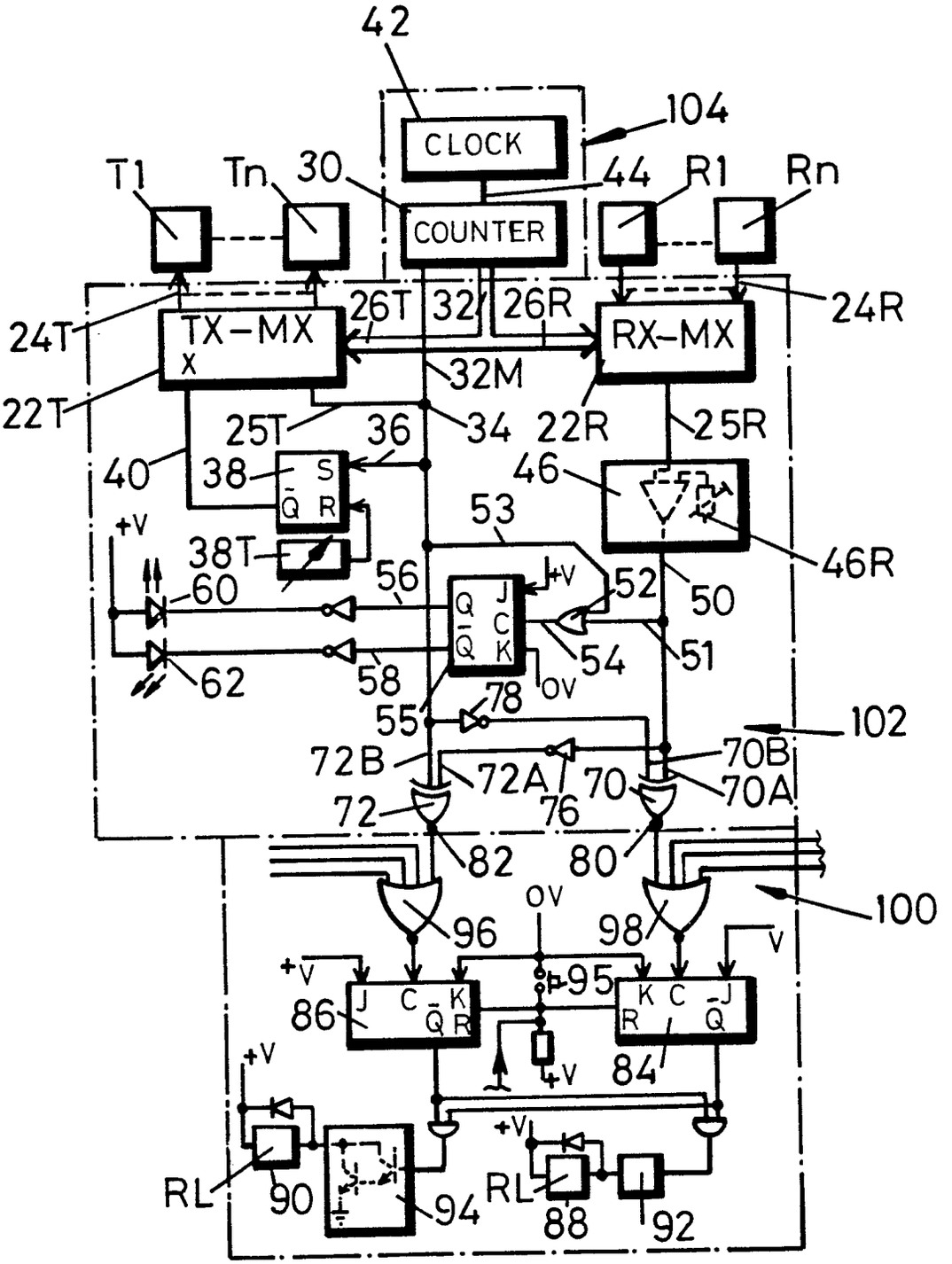
42
CLOCK
104
T1
Tn
30
COUNTER
44
R1
Rn
24T
TX-MX
X
26T
32
26R
RX-MX
24R
32M
22T
25T
36
34
22R
25R
40
38
S
Q
R
46
46R
+V
38T
53
56
60
52
50
62
58
54
51
OV
55
78
102
72B
72A
70
70B
70A
72
76
82
80
OV
100
96
98
V
+V
86
95
84
RL
90
94
88
92

FIG. 3