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EUROPEAN PATENT APPLICATION

21 Application number: 86304877.3

61 Int. Cl.⁴: **H 01 L 21/90**
H 01 L 21/268

22 Date of filing: 24.06.86

30 Priority: 24.06.85 US 748375
23.08.85 US 768590

43 Date of publication of application:
14.01.87 Bulletin 87/3

84 Designated Contracting States:
AT BE CH DE FR GB IT LI LU NL SE

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54 Planarization of metal films for multilevel interconnects.

57 In the fabrication of multilevel integrated circuits, each metal layer (54, 64) is planarized by heating to momentarily melt the layer. The layer is melted by sweeping laser pulses of suitable width, typically about 1 microsecond duration, over the layer in small increments. The planarization of each metal layer eliminates irregular and discontinuous conditions between successive layers. The planarization method is particularly applicable to circuits having ground or power planes (64) and allows for multilevel interconnects. Dielectric layers (50, 60) can also be planarized to produce a fully planar multilevel interconnect structure. The method is useful for the fabrication of VLSI circuits, particularly for wafer-scale integration.

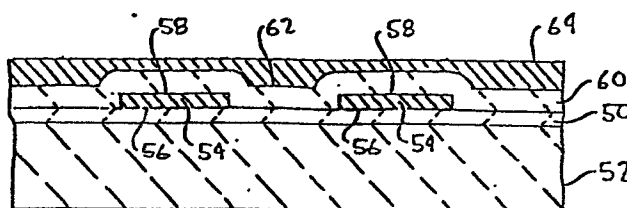


FIG. 3B

PLANARIZATION OF METAL FILMS FOR
MULTILEVEL INTERCONNECTS

BACKGROUND OF THE INVENTION

The invention relates generally to integrated circuit and other electrical interconnection network fabrication and more particularly to the planarization of layers to produce a sufficiently flat topography in fabricating a multilevel structure.

The United States Government has rights in this invention pursuant to Contract No. W-7405-ENG-48 between the U.S. Department of Energy and the University of California, for the operation of Lawrence Livermore National Laboratory.

Multilevel interconnect schemes for integrated circuits generally require one or more planarization steps, in order to maintain an acceptably flat topography for lithography and thin-film step coverage on the higher levels. Traditional approaches have involved planarization of the interlevel insulation (dielectric) layers, either by spin-on application (e.g., polyimide), or by reflow (e.g., phosphosilicate glass).

The fabrication of multilevel VLSI circuits often requires the use of thin-film planarization procedures. The need is particularly acute to achieve wafer-scale integration; an efficient, high-power wafer-scale integrated system might require four levels of interconnect plus two or more ground or power planes. The most severe topographic problems occur around stacked vias, where a connection extends from the bottom interconnect level to the top level.

Planarization techniques have conventionally involved smoothing the dielectric between the metal layers. Spinning on polyimide as the dielectric is often used to achieve planarity. Other dielectric planarization techniques use bias sputter etching, and still others use photoresist to planarize and then plasma back-etch to the underlying SiO_2 . Phosphosilicate glass flow can be achieved by furnace

heating. Yet another planarization technique uses a scanning cw laser to rapidly flow phosphosilicate glass. None of these techniques will planarize a stacked (nested) via, because the dielectric must be removed from the contact area between each level, resulting in a large thickness deficiency at the via.

A high performance VLSI wafer scale multilevel interconnect system is desirable. This system should be compatible with bi-polar logic technology, i.e., provide high current drive capability and high power. It will often be necessary to provide power, ground, clock and reference voltage planes, especially for ECL technology, to provide low ohmic drops and reduced cross talk. Gold metallization is preferred for low electrical resistance; however, silver and aluminum may also be desirable. A SiO_2 dielectric is preferred for the reliability and thermal tolerance; glass or other dielectrics are also useful. The system must provide multiple levels, e.g., five or more, with some vias extending from top to bottom.

Accordingly it is an object of the invention to provide a method for producing an electrical interconnection network.

It is also an object of the invention to planarize the levels in a multilevel VLSI circuit.

It is a further object of the invention to produce planarized multilevel electrical interconnection network structures.

It is another object of the invention to
5 produce multilevel VLSI circuit structures having power, ground and/or reference voltage planes.

It is yet another object of the invention to provide a method of producing multiple levels, as many as five or more, with vias extending between various
10 levels, including from top to bottom.

SUMMARY OF THE INVENTION

The invention is a planarization method for the fabrication of multilevel integrated circuits or other electrical interconnection networks, and the resulting planar structures, in which each metal level is
15 planarized by melting the metal using a pulsed laser prior to patterning. Short pulses, e.g., about 1 microsecond, are used to preclude undesirable metallurgical reactions between the metal film, any adhesion or barrier layer, and dielectric layer. Laser
20 planarization of metals is particularly well suited to multilevel systems which include ground or power planes.

In particular gold films are planarized on SiO_2 dielectric layers (with an adhesion layer) using

a pulsed laser, e.g., a flashlamp-pumped dye laser. For a 1 micron layer, the pulse duration is typically about 1 microsecond which allows the heat pulse to uniformly penetrate the gold while not penetrating substantially through the underlying SiO_2 hence not perturbing the lower levels of metal. Excellent planarization of the gold films is achieved, less than 0.1 micron surface roughness (even starting with extreme topographic variations), as well as improved conductivity.

10 Aluminum metallization is planarized using a thin silicon overcoating to passivate the aluminum and increase its initial optical absorption.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

15 Figure 1A, B, C shows a multilevel structure with nested vias with no planarization (prior art), with dielectric planarization only (prior art), and with both dielectric and metal planarization, respectively.

Figure 2 is a block diagram of apparatus for planarizing metal layers in a multilevel structure.

20 Figure 3A and B shows a multilevel structure in the form of microstrips covered by a ground plane before and after planarization of the metal layer, respectively.

Figure 4A and B shows a surface profile of a 1 micron aluminum layer on a commercial C-MOS gate array before and after planarization, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The invention is a method for achieving
5 planarity in multilevel systems by the planarization of the metal layers, and the resulting planar structures. The metal and dielectric layers are typically of thickness on the order of 1 micron. Planarizing metals by momentarily melting them is feasible because of the
10 very high surface tension (about 50 times that of most nonmetallic liquids) and relatively low viscosity (similar to water) of clean molten metals; the surface tension is the planarizing force while the viscosity is the damping force. Rapid planarization can thus be
15 achieved. Calculating the time-dependent relaxation of low-amplitude, long-wavelength topographic variations in a molten metal surface, neglecting inertial effects (the Reynolds number is low under these conditions), the amplitude of a Fourier component of spatial period L
20 will decay exponentially with a time constant of $\tau = 3\mu L^4 / 16\pi^4 \gamma h^3$ where μ , γ , and h are the dynamic viscosity, surface tension, and thickness of the molten metal. For gold, $\gamma = 1130 \text{ ergs/cm}^2$; experimental data

on its viscosity is unavailable so the value for silver,
i.e. $\mu = 0.03$ poise, is used. Thus in only 1
microsecond, for a 1 micron thick layer, all Fourier
components of the surface topography in molten gold with
5 periods shorter than approximately 21 microns will be
virtually eliminated. Since most VLSI structures of
interest are much smaller, this would be quite
sufficient planarization. A duration of the melt much
longer than 1 microsecond may induce unacceptable
10 metallurgical reactions in the thin films. For example,
molten aluminum will reduce an SiO_2 dielectric to form
silicon in a few seconds. As another example, it is
estimated, based on typical diffusivities in molten
metals, that 1 micron molten gold will completely alloy
15 with a titanium adhesion layer in about 1 ms.

Thus, according to the invention, a very fast
(microsecond) heat pulse is optimal for planarizing
metals. In general, the heat pulse should be less than
1 ms, and more preferably in the 10 ns-1 microsecond
20 range. Initial experimental tests utilized a high-power
scanning electron beam to melt an aluminum line sitting
in a silica trench. Excellent silica wetting and
partial aluminum planarization was clearly observed.
However, rastering a fine electron beam does not produce
25 a perfectly flat surface, because not enough metal area

is molten at one time. Therefore, according to the invention, it is preferred to use a pulsed laser to melt a large area, e.g., 4 mm² of metal with a single pulse.

In contrast with dielectric planarization techniques, the present invention requires that the dielectric be capable of withstanding high temperatures, e.g., SiO₂ or some glasses, whereas the planarized metal has a moderate melting point, e.g., Au or Al. Conventional planarization processes often require just the opposite, i.e., a relatively low-temperature dielectric such as polyimide (for spin planarization) or phosphosilicate glass (for thermal planarization) is used with a moderate- or high-temperature metallurgy, e.g., tungsten. Planarization of the metals is advantageous because refractory dielectrics tend to be of higher quality, having few pinholes, greater dielectric strength and higher reliability. Furthermore, for metal interconnect levels, the compelling need is for electrical continuity of the fine wires, and this is easier to achieve with a non-refractory material, which would generally have a high surface mobility at the deposition temperature. Moreover the problem of filling stacked vias is avoided because the planarized metal would be correspondingly thicker over the via area. The invention includes a

multilevel interconnect process which uses both laser planarization of metal and also a dielectric planarization process to obtain a fully planar interconnect structure.

5 Metal planarization combined with dielectric planarization eliminates problems with nested vias as illustrated in Figure 1A, B, C. A prior art structure with no planarization is shown in Figure 1A. First gold layer 10 is formed on first dielectric layer 12. A
10 second dielectric layer 14 is then formed and patterned so that a second gold layer 16 is formed in electric contact with first gold layer 10. After patterning the second gold layer 16 a third dielectric layer 18 is added and patterned. Finally, a third gold layer 20 is
15 formed in contact with second gold layer 16 and patterned as desired. The process can be continued in this manner for as many levels as are required. However, the topography of the via formed by the stacked gold layers 10, 16 and 20 which form an electrical
20 interconnect and the adjacent dielectric layers 14 and 18 are irregular. The planarization of the dielectric layers as shown in Figure 1B provides some improvement but the topography is still irregular and limits the number of levels which may be interconnected. With both
25 metal and dielectric planarization in accordance with

the invention, as shown in Figure 1C, the problem is eliminated; the topography is uniform and there are no steps in the gold layers 16 and 20 or dielectric layers 14 and 18. Multilevel interconnects between many levels
5 can thus be made.

The use of laser planarization of metal films imposes some constraints on the choice of metals and dielectrics. The molten metal must wet the dielectric; this generally requires that the solid metal has good
10 adhesion to the underlying dielectric. Gold films deposited directly on SiO_2 do not adhere well, and correspondingly molten gold does not wet SiO_2 (contact angle of 140°). In contrast, the customary use of an oxygen-active metal as an adhesion layer, e.g., Cr, Nb,
15 Ti, or $\text{Ti}_{0.1}\text{W}_{0.9}$ alloy gives good adhesion when the gold is solid, and correspondingly excellent wetting in the liquid phase. Aluminum films deposited directly onto SiO_2 adhere in the solid phase and wet well in the liquid phase.

20 In addition to having good adhesion, the metal film should be able to absorb a significant amount of the incident optical power. For this reason, highly reflective metals such as aluminum or silver are more difficult to utilize than gold; gold has greater than
25 50% absorbance in the green or blue. Thus wavelengths

less than about 650 nm are preferred for gold layers. The problem with highly reflective metals is not the energy requirement (simply increase the incident flux), but that when reflectivity is near unity, small changes
5 in surface texture, topography, and composition can radically alter the absorbed power. This can lead to instabilities, in which excess absorbed heat modifies the surface in such a way as to further reduce the reflectance, causing still more optical absorption,
10 until the film is vaporized. However, one solution is to overcoat such metal films with a thin absorbing layer.

Based on the above considerations, gold is the preferred material for laser planarization, although aluminum is also acceptable and silver could be used.
15 Typical layer thicknesses are on the order of 1 micron.

Aluminum is more commonly used for IC metallization than gold and thus the ability to planarize aluminum thin films is very important. For aluminum the surface tension is 520 ergs/cm^2 and the
20 viscosity is about 0.014 poise at 800°C . However, laser planarization of aluminum films is more difficult than gold. The high reflectance of aluminum, about 92 percent, requires higher optical pulse energy. Small variations in the surface texture, topography and
25 composition can significantly increase the absorbed

power, causing damage. The most severe problem is the existence or formation of a refractory native oxide (Al_2O_3) layer on the surface of the aluminum. This solid oxide skin can impede planarization even if the
5 underlying aluminum is molten. If the layer is heated sufficiently to also melt the aluminum oxide then damage to underlying layers can result. One solution is to remove the oxide in a vacuum system, e.g., by ion
- milling, and then perform the laser planarization in the
10 vacuum.

A preferred method for the planarization of an aluminum layer, typically about 1 micron thickness, according to the invention is to form, e.g. sputter deposit, a thin, typically less than about 200 Å, layer
15 of amorphous silicon over the aluminum after removing, e.g. sputter etching, the native Al_2O_3 oxide. The silicon layer has two functions, to passivate the aluminum against oxide formation, and to act as an antireflection coating. Thus, the thickness is chosen
20 for antireflection or low reflection, preferably in the 100-150 Å range, and is much thinner than the aluminum layer, about 1 percent of the aluminum layer thickness. In the formation of the aluminum layer on the structure, the aluminum is deposited without any contact to oxygen,
25 e.g., by sputter deposition in a vacuum, so that no

aluminum oxide is formed. The silicon layer is also deposited on the aluminum layer in vacuum to prevent the formation of the aluminum oxide. Thereafter, the coated aluminum layer can be removed from the oxygen free environment for the processing since the aluminum layer is now protected from oxidation (SiO_2 formation does not interfere with planarization). When the silicon-coated aluminum is heated in the laser planarization step, the silicon alloys with the aluminum so the layer becomes reflective again thereby limiting the temperature and heat absorption. Also the resulting structure has no silicon layer since the silicon has been alloyed into the aluminum.

Having chosen the metal, it is necessary to choose the dielectric. It is essential that the dielectric not be damaged by momentary exposure to the overlying molten metal. This probably eliminates organics such as polyimide. The preferred dielectric is pure SiO_2 , mainly because its physical properties are desirable and well characterized; some glasses can also be used. For the Au/SiO_2 multilevel system, an adhesion layer such as Cr, Ti or W is necessary at every interface between the two materials.

Once the metal/dielectric system is chosen, the heat pulse can then be optimized. The optical

absorption depth in Au or Al is so short, 200 Å at
typical wavelengths, that the heat is generated
essentially at the surface of the metal film. The heat
will diffuse a depth $z = (\alpha t)^{1/2}$ in time t , where α is
5 the thermal diffusivity of the gold ($1.0 \text{ cm}^2/\text{s}$ at
700°C). It therefore takes only 10 ns for most of the
heat to penetrate through a micron of gold. A somewhat
longer pulse width is desirable in order to allow
sufficient metal flow over a sufficiently large area,
10 e.g., a 20 micron spatial period. For a 1 microsecond
heat pulse, the gold may be considered to be nearly in
thermal equilibrium during the pulse (relatively small
vertical temperature gradients). The underlying SiO_2
dielectric has a much lower thermal diffusivity,
15 $\alpha = 0.032 \text{ cm}^2/\text{sec}$. This is useful for two reasons:
the underlying layers are exposed to much lower
temperatures than is the surface, and the pulse energy
required to achieve complete melting is minimized. The
minimum absorbed energy needed to melt 1 micron of Au on
20 top of a 1 micron SiO_2 layer on a silicon wafer ranges
from 0.4 J/cm^2 at 10 ns pulse duration, rising
gradually to 0.8 J/cm^2 for a 1 microsecond pulse, and
thereafter increasing approximately as the square root
of the pulse duration (due to heat penetration into the
25 silicon substrate). A pulse shorter than 10 ns would

not be useful, because large thermal gradients would be generated in the gold layer, vaporizing the surface before the bottom of the film reaches its melting point. A pulse up to 1 ms may be used in some
5 circumstances. For laboratory work these energies must be doubled to account for the approximately 50% reflectance of the gold. These energies are minimums; in practice operation at somewhat higher values is necessary to allow for cold spots in the beam. The
10 laser planarization process for the Au/SiO₂ interconnect system has been calculated and experimentally verified to have a large operating window for a pulse length of 1 microsecond. Energies can typically be increased a factor of two above the minimum
15 values without significant film vaporization or damage.

As described the preferred pulse length is primarily chosen as a function of the heat flow characteristics, i.e., the thickness of the dielectric layer. The laser pulses of predetermined pulse-width
20 are stepped or rastered over the surface of a metal layer. The beam spot size is much greater than the spatial period of any surface features of the layer, e.g., 2 mm compared with 20 microns. The beam spot is rastered generally in an overlapping pattern, e.g., 1 mm
25 steps for 2 mm diameter spot size. Often a single laser

pulse of predetermined width is sufficient at each incremental step on the surface of the metal layer. However, the invention also includes utilizing several pulses at each step; in particular, for long period features it may be necessary to utilize more than a single pulse in order to achieve planarization. Lengthening the pulse is not generally advantageous since it is limited by the heat flow characteristics of the layer, but the use of multiple pulses of the predetermined effective pulse width can be advantageous.

In one particular apparatus for carrying out the invention, shown in Figure 2, a pulsed laser 30, e.g., a linear flashlamp-pumped dye laser containing a coumarin dye, is used to supply optical pulses at 504 nm, of which 48% is reflected by the gold films. The pulses have 1 microsecond duration (full width at half maximum), 150 mJ of energy, and 1 Hz repetition rate. The beam 32 is focused to a 2 mm diameter spot on the wafer 34 by means of lens 36. No effort is made to make the spot uniform in intensity; consequently about half of the pulse energy (around the beam circumference) is below the melt threshold and hence wasted. By adjusting the distance between the wafer 34 and lens 36 the spot size can be varied; the wafer is preferably positioned at a point beyond the focal point of lens 36

rather than before the focal point. X-Y translation stages 38 are configured with stepping motors to translate the wafer 34 mounted thereon between pulses; typically the pulses are spaced 1 mm apart so there is
5 considerable overlap. Laser 30 is powered by power supply 40 which is pulsed by trigger 42 to produce pulses of laser radiation. Trigger 42 also controls X-Y stages 38 so that the laser spot is stepped across the surface of wafer 34. An alternate more efficient and
10 versatile arrangement would be to homogenize the beam, e.g., by means of a kaleidoscope.

Experiments were mostly performed on sputter-deposited gold films on SiO_2 dielectric layers. Initially, the underlying substrates were bare
15 silicon wafers. Later work deposited a gold pattern ("metal level 1") with a pitch of 4, 8 or 16 microns onto thermally grown SiO_2 , then coated the gold with a second SiO_2 layer by chemical vapor deposition, and finally sputter-deposited an upper layer of gold ("metal
20 level 2"). It is important to deposit suitable adhesion layers at the Au/SiO_2 interfaces (e.g., Cr, Nb, or $\text{Ti}_{0.1}\text{W}_{0.9}$) or else the structures will fail when pulsed with heat. The results of the planarization procedure are illustrated in Figures 3A and B which
25 illustrate structures in the form of microstrips

(transmission lines) covered by a ground plane. A first dielectric layer 50 of SiO_2 is formed on a substrate 52 of silicon. A first layer of gold 54 is formed on dielectric layer 50 with a very thin adhesion layer 56 in between. Metal layer 54 is then patterned into a pair of parallel lines, for example, 7 microns wide, 1 micron thick on 16 micron centers. Gold layer 54 is then coated with a second dielectric layer 60, with another thin adhesion layer 58 therebetween. Finally, dielectric layer 60 is coated with a thin adhesion layer 62 and a second gold layer 64 which forms a ground plane. Figure 3A shows ground plane 64 before planarization; Figure 3B shows ground plane 64 after planarization. Laser planarization of metal level 64 had no apparent effect on the underlying metal level 54, due to the thermal barrier presented by the SiO_2 dielectric layer 60. In principle this process could be repeated: coating with SiO_2 , opening contact windows, coating with Au, laser planarizing, patterning the Au, coating with SiO_2 , etc. After each level of Au is deposited, the planarity of the surface is restored by laser planarization.

The wafers were exposed to ambient air during the planarization process; no adverse effects appear to be associated with this procedure. In the case of

aluminum, which oxidizes easily, it is possible to operate in an oxygen-free environment, but satisfactory results were obtained with aluminum without doing so. A few experiments were done using a KrF excimer laser as the pulse source, but the 10 ns pulse gave a substantially reduced operating window between melting and damage, compared with the factor of two window available with the 1 microsecond pulsed dye laser.

As is evident from Figures 3A and B the planarization process was very successful. The CVD and sputtering processes used to deposit the SiO_2 and Au produced extreme step coverage problems, yet the planarized gold is smooth and flat to better than 500 Å. No changes whatsoever were noticeable in the lower SiO_2 or gold layers. This indicates that the process should be readily adaptable to more levels of metal. The geometries shown were particularly challenging cases, for the gold in these examples was barely thick enough to cover the higher regions after the planarization has been accomplished. The difficulty of planarization, i.e., melt time required, varies as h^{-3} , where h is the metal film thickness. Thicker gold films flow much more easily. Good results were obtained with a relatively thick 1.6 micron gold film on

a silicon wafer etched with vertical grooves and coated with 0.4 micron SiO_2 .

The deposited dielectric layers should have low internal stress for the planarization process to be successful. For example, sputter-deposited SiO_2 tended to be much more highly stressed than CVD-deposited SiO_2 . Multilayer structures using the sputtered SiO_2 were found to rupture during laser planarization. For designing a multilevel metal process, it is important to understand what physical changes (besides the obvious topographic ones) occur in the metal films due to the laser planarization process.

One concern is whether the adhesion layer at the Au/ SiO_2 interface diffuses significantly into the gold while the latter is molten. Using Secondary Ion Mass Spectroscopy (SIMS) depth profiling to study planarized gold samples having adhesion layers of Cr, Nb, and $\text{Ti}_{0.1}\text{W}_{0.9}$, no radical movement of any adhesion layer was observed. While it is difficult to draw quantitative conclusions from SIMS data, it appears that each type of adhesion layer exhibited a small amount of diffusion into the gold (i.e., a Gaussian-like impurity tail was observed penetrating up into the gold). The concentration levels appear to be in the parts per million when more than about 0.2 microns from

the adhesion layer. The fastest diffuser was titanium, which produced a weak but measurable signal as far as 0.5 microns from the interface. The slowest diffuser was tungsten, which did not diffuse measurably into the gold. Since the diffusivities of impurities in molten metals are typically between 10^{-4} and 10^{-5} cm^2/s at 1100°C , this confirms that the gold could only have been molten for at most a few microseconds. None of these impurity levels are considered significant for multilevel interconnect purposes. The chemical etching properties of the gold appear unaffected by the planarization process.

No change in average thickness of the films was observed at normal power levels. Thus there is no significant vaporization of the films during planarization, even when the same area is pulsed repetitively.

The average grain size of the gold films increased substantially after laser planarization, from about 0.3 microns as deposited to 1 or 2 microns after planarization. However, this did not interfere with the ability to chemically etch the gold with edge roughnesses much less than a micron. In fact, the planarized gold is easier to pattern accurately because it is smoother than the sputtered films. The greater

the incident optical pulse energy, the larger the grain size, probably because these areas have more thermal energy stored in the substrate, hence the cooling time is longer, which allows more opportunity for grain growth before the temperature drops too low. Compared with sputter-deposited films, the texture is very smooth (100 Å roughness). X-ray diffraction showed that the planarized grains are oriented almost exclusively in the $\langle 100 \rangle$ direction, regardless of initial orientation (which was $\langle 111 \rangle$ for sputter deposition).

Adhesion of the planarized gold films is better than before planarization. In all cases resulting tensile strengths were greater than 5000 psi. In many cases the final failure occurred in the silicon substrate rather than the Au/SiO₂ interface.

The sheet resistance of the planarized films was determined by 4-point probing, and was found to be approximately 12% lower than before planarization. Typical room-temperature resistivities were 2.95 $\mu\Omega\text{-cm}$ before planarization, and 2.6 $\mu\Omega\text{-cm}$ after planarization. This is not far from the bulk value of 2.2 $\mu\Omega\text{-cm}$, which would be the lowest possible value. Presumably this reduction in resistance is due to the larger grain size, which reduces electronic scattering.

All of the above physical properties appear to be independent of the number of pulses; i.e., there is no advantage or disadvantage to using multiple planarization pulses. The only defects which appear to result from laser planarization occurred in areas of poor adhesion, presumably where the SiO_2 substrate was contaminated prior to the Au deposition. In such spots, the poor heat transfer results in overheating and vaporization of the spot, leaving a crater approximately 10 microns in diameter. In addition to these defects, there is a visible artifact which occurs at the border of the melted area, presumably due to a slight difference in level between the planarized and unplanarized area. This is typically very small, about 100 Å.

Silicon coated samples of both pure aluminum and aluminum alloy with 1 percent silicon, which is a standard IC metallization, on an SiO_2 dielectric layer have been planarized. Typical fluences are 1 J/cm^2 which is comparable to that used for planarizing gold. Since the amorphous silicon coating rapidly alloys with the aluminum during the melt, restoring the high reflectance of the surface, the process is self-limiting by limiting the absorbed energy, and thus the process has higher tolerance to non-uniformities in heat

transfer, e.g. due to vias. Any native oxide that forms on the amorphous silicon coating will not interfere with planarization since SiO_2 reacts very rapidly with molten aluminum. No difference in planarization behavior has been observed when performing the planarization of silicon coated aluminum in 0.1 Torr vacuum compared with the usual ambient air environment.

The surface profile 72 of a 1 micron aluminum layer 70 on a commercial C-MOS gate array is shown in Figure 4A. Variations in the surface are produced by the underlying structure which includes (not shown) an SiO_2 dielectric layer on a silicon substrate and polysilicon lines on the SiO_2 with vias extending to the silicon substrate. The surface is treated by first removing aluminum oxide and then coating with 120 Å silicon. The aluminum layer is then planarized by applying laser pulses, producing the surface profile shown in Figure 4B, in which variations are less than 10 percent of the original surface variations.

Thus by utilizing the pre-planarization steps of first preventing the formation of an aluminum oxide layer or removing an already formed aluminum oxide layer and then coating the aluminum layer with a thin silicon passivating antireflection layer, an aluminum layer may be planarized by the same method as planarizing a gold

layer. Laser planarization substantially increases the grain size of sputter deposited aluminum from about 0.3 microns as deposited to 1-2 microns after planarization. The electrical resistance of an aluminum
5 film is reduced typically from 4.14 to 3.76 $\mu\Omega$ -cm.

Laser planarization of the metal layers thus offers an attractive technique for fabricating multilevel interconnect structures, particularly where a number of ground or power planes are included. The
10 Au/SiO₂ combination is well suited to laser planarization, although successful results were also achieved with the Al/SiO₂ combination. Two levels of metal have been demonstrated, but this process can be extended to circuits containing a large number of
15 interconnect levels and ground/power planes by planarizing after each metal level is deposited. The technique can be used by itself, or it can be combined with a compatible dielectric planarization process to make truly planar multilevel interconnect structures.

20 Changes and modifications in the specifically described embodiments can be carried out without departing from the scope of the invention which is intended to be limited only by the scope of the appended claims.

CLAIMS:

1. A method of planarizing a metal layer comprising heating the metal layer to momentarily melt the layer to produce a flat surface prior to patterning the layer.
2. The method of Claim 1 wherein the duration of the melt is sufficient to melt the metal without vaporization, allow metal flow over a preselected area, and prevent damage to any underlying layer.
3. The method of Claim 1 wherein heating the metal layer is performed by applying pulsed laser radiation to the surface of the layer.
4. The method of Claim 3 further including stepping the pulsed laser radiation over the surface of the metal in a series of incremental steps.
5. A method of fabricating an electrical interconnection network, comprising:
 - forming in sequence a plurality of alternating layers of metals and dielectric materials;
 - planarizing each metal layer to produce a flat surface prior to patterning the layer and prior to forming an additional dielectric layer;
 - patterning each metal layer and dielectric layer in a preselected pattern prior to forming an additional layer.
6. The method of Claim 5 wherein the step of planarizing each metal layer is performed by heating the metal layer to momentarily melt the layer to produce a flat surface.
7. The method of Claim 6 wherein the duration of the melt is sufficient to melt the layer without vaporizing

the layer or damaging any underlying layer and to allow metal flow over a preselected area.

8. The method of Claim 6 wherein the step of planarization is performed by irradiating the layer with pulses of laser radiation.

9. The method of Claim 5 further including:
forming the metal layers of a low melting point metal;
forming the dielectric layers of a high temperature refractory dielectric material.

10. The method of Claim 5 further including:
forming the metal layers of gold;
forming the dielectric layers of SiO_2 or glass; and
forming an adhesion layer of an oxygen action metal alloy between the gold and dielectric layers which is much thinner than the gold or dielectric layers.

11. An electrical interconnection structure comprising a plurality of metal layers separated by dielectric layers, each metal layer having been planarized to form a flat surface by heating to momentarily melt the layer prior to the formation of an additional dielectric layer, the metal layers having been patterned after planarization according to a preselected pattern and interconnected through the dielectric layers.

12. The structure of Claim 11 wherein the metal layers are formed of gold, and the dielectric layers are formed of SiO_2 and further including an adhesion layer of an oxygen-active metal between each gold and SiO_2 layer, which is much thinner than the gold or SiO_2 layers.

13. A method of planarizing a layer of a metal which forms a native oxide coating on its surface, comprising:

forming the metal layer without an oxide coating;
forming a passivating and antireflection coating on the metal layer, the coating having a thickness substantially less than the metal layer;
heating the coated metal layer to momentarily melt the layer to produce a flat surface prior to patterning the layer.

14. The method of Claim 13 for planarizing an aluminum layer, comprising forming a coating of silicon on the aluminum.

15. A method of fabricating an electrical interconnection network, comprising:

forming in sequence a plurality of alternating layers of metals which form native oxide surface coatings and dielectric materials;

planarizing each metal layer to produce a flat surface prior to patterning the layer and prior to forming an additional dielectric layer by forming the metal layer without an oxide coating, forming a passivating and antireflection coating on the metal layer, the coating having a thickness substantially less than the metal layer, and heating the coated metal layer to momentarily melt the layer to produce a flat surface;

patterning each metal layer and dielectric layer in a preselected pattern prior to forming an additional layer.

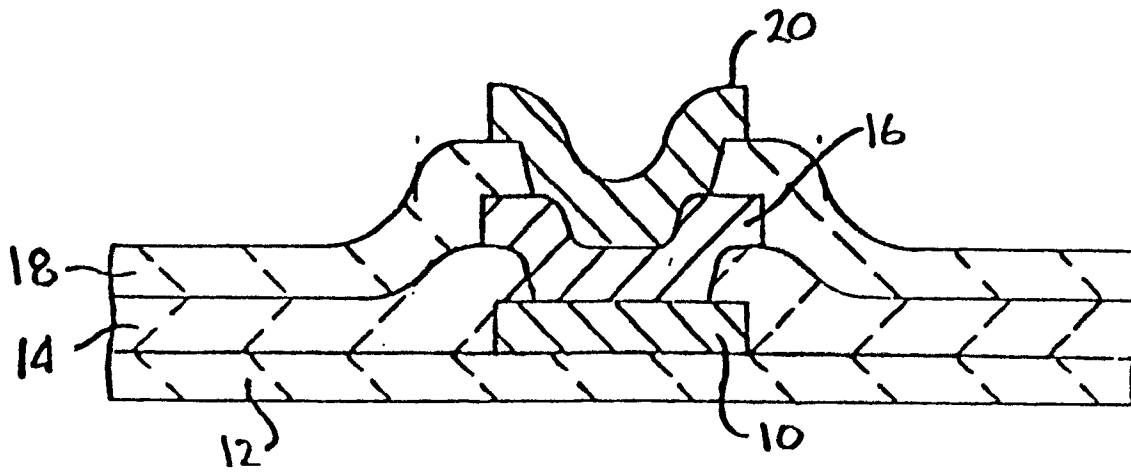
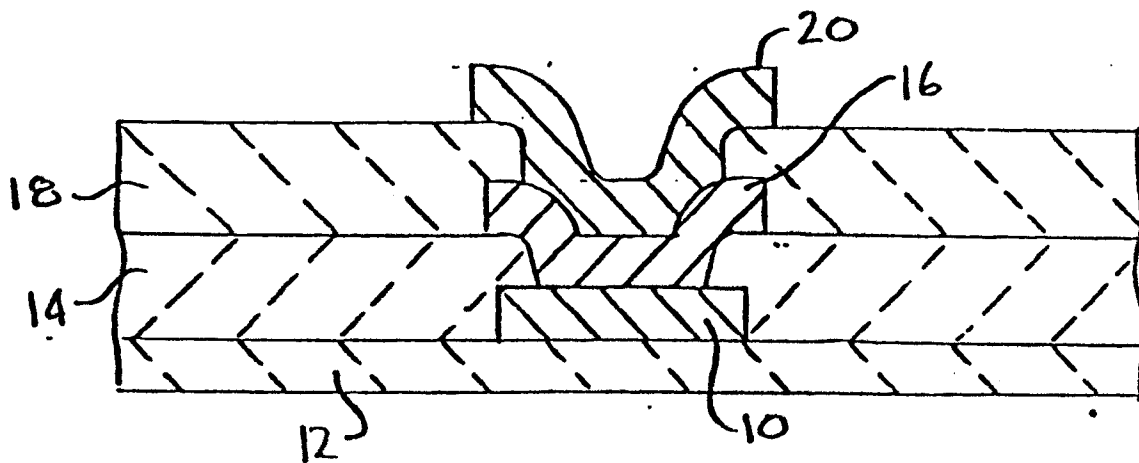
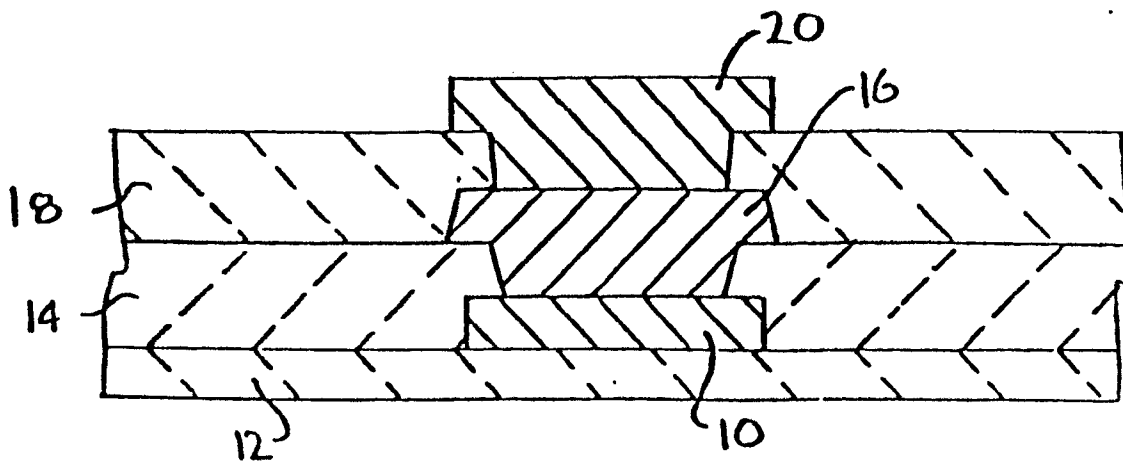
16. The method of Claim 15 further including:

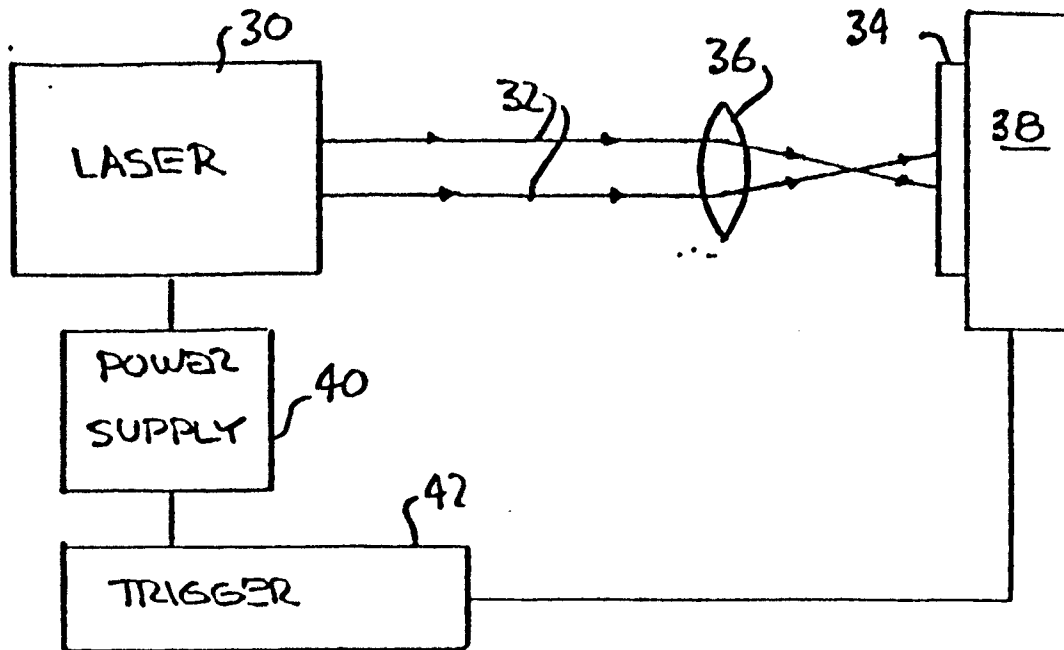
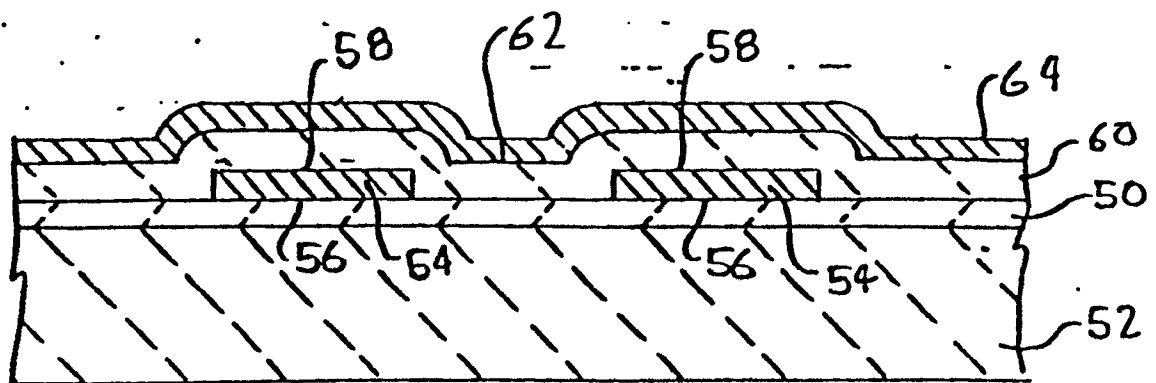
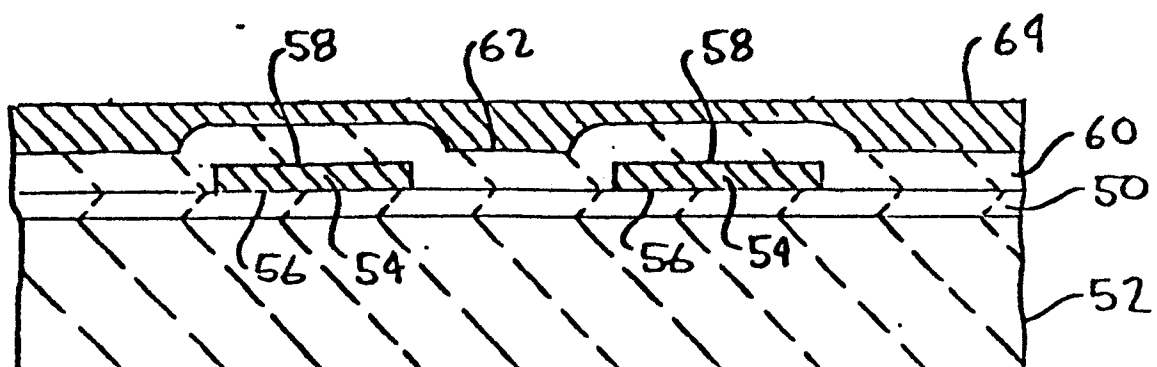
forming the metal layers of aluminum or aluminum-silicon alloy;

forming the passivating and antireflection coating of silicon;

forming the dielectric layers of a high temperature refractory dielectric material.

17. An electrical interconnection structure comprising a plurality of aluminum or aluminum-silicon alloy layers separated by dielectric layers, each aluminum or alloy layer having been planarized by eliminating any oxide coating of the aluminum or alloy, forming a passivating and antireflection coating of silicon on the aluminum or alloy, and heating to momentarily melt the layer prior to the formation of an additional dielectric layer, the metal layers having been patterned according to a preselected pattern and interconnected through the dielectric layers.

**FIG. 1A** (PRIOR ART)**FIG. 1B** (PRIOR ART)**FIG. 1C**

**FIG. 2****FIG. 3A****FIG. 3B**

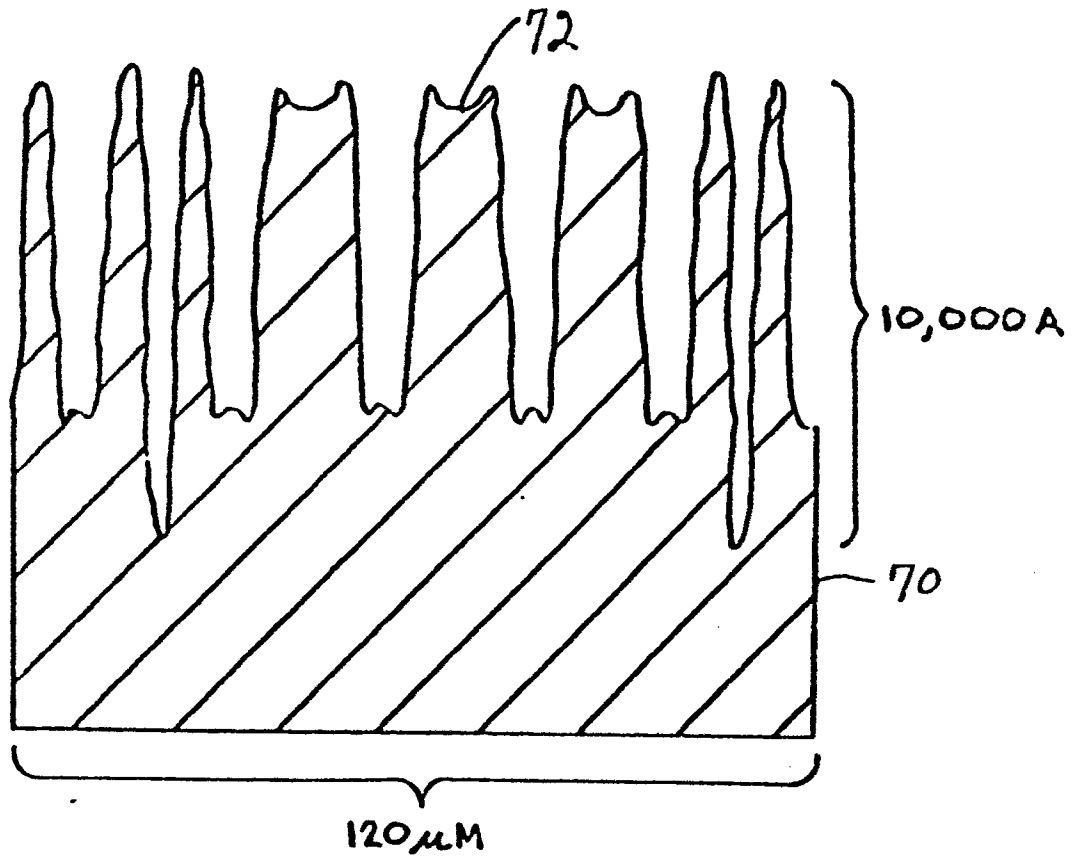


FIG. 4A

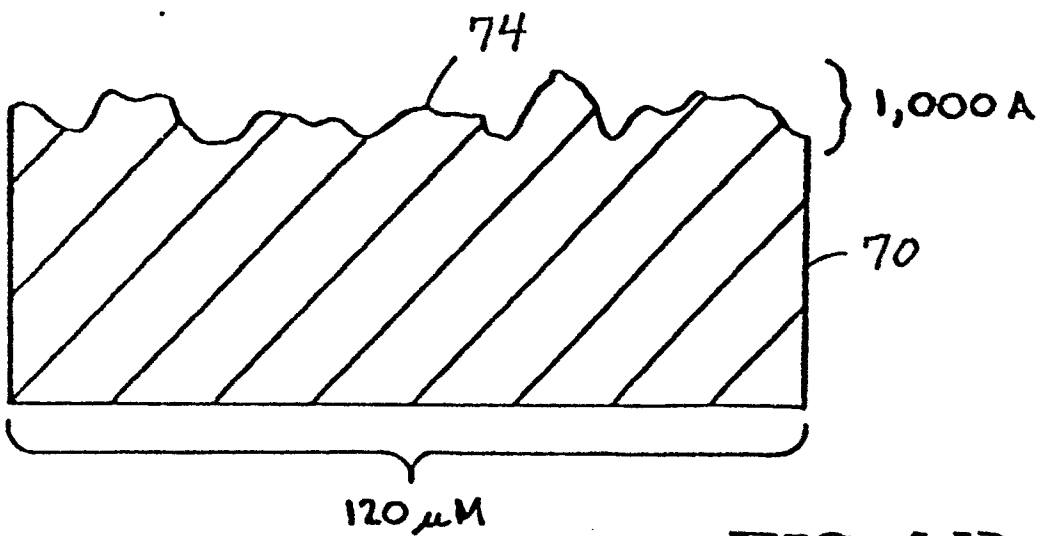


FIG. 4B



EP 86 30 4877

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	EP-A-0 097 848 (TOKYO SHIBAURA DENKI K.K.) * abstract; page 6, lines 32-37; page 7, lines 8-9; page 8, lines 6-22; page 11, line 26 - page 12, line 23; figures 2D, 2E, 4B * ---	1,2,5- 7,9,17	H 01 L 21/90 H 01 L 21/268
A	EP-A-0 041 776 (FUJITSU LTD.) * abstract; figures 3, 4; page 16 * ---	1,5	
A	US-A-4 508 815 (P. ACKMANN) * column 2, line 52 - column 3, line 13 * ---	1,5	
A	RCA REVIEW, vol. 40, no. 3, September 1979, pages 339-344, Princeton, US; C. WU et al.: "Laser annealing to round the edges of silicon structures" * page 339, last paragraph; page 344 * ---	1	TECHNICAL FIELDS SEARCHED (Int. Cl.4) H 01 L 21/268 H 01 L 21/88
A	EP-A-0 090 565 (FUJITSU LTD.) * page 2, lines 19-25 * -----	13,14, 16,17	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 24-09-1986	Examiner PRETZEL B.C.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	