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(54) Abstract operation-signalling from a raster scan video controller to a display memory.

(57) A generalized operation-signalling logic for a raster scan video controller whereby the video controller, in accessing the memory of a computer system, can indicate what type of operation is to be performed at each memory address to be accessed. The signalling scheme provides a rich set of functions, logic to generate this signalling and an external PLA-type device which interprets this signalling for a wide variety of memory types.

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Abstract operation-signalling from a raster scan video controller to a display memory.

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to the following applications: "HARDWARE WINDOWING SUPPORT IN A BIT MAPPED RASTER SCAN VIDEO CONTROLLER" Craig MacKenna and Jan-Kwei Li, inventors, serial No. 793,521, filed October 31, 1985; "DISPLAY ACCUMULATOR FOR HARDWARE WINDOWING RASTER SCAN VIDEO CONTROLLER" Craig MacKenna, Jan-Kwei Li and Cecil H. Kaplinsky, inventors, serial No. 793,526, filed October 31, 1985; "UPDATE CACHE FOR A RASTER SCAN VIDEO CONTROLLER", Craig MacKenna and Jan-Kwei Li, inventors; and "PROGRAMMABLE SHARING OF DISPLAY MEMORY BETWEEN UPDATE AND DISPLAY PROCESSES IN A RASTER SCAN VIDEO CONTROLLER", Craig MacKenna and Jan-Kwei Li, inventors; the last two filed simultaneously herewith. All these applications are assigned to the same assignee, and incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention pertains to the field of bit-mapped alphanumeric and graphic processors, or bit-mapped raster scan video controllers, and in particular to the logic and circuits necessary to output display memory addresses and to signal what type of operation is to be performed at each address in a generalized way. The invention is useful for high performance display systems, black/white or color, especially those capable of accessing display memory as needed to create and update an image on a video display, because it provides a simplified interface with a wide variety of memory types.

Description of the Prior Art

Most presently available video display systems typically include a processor, a video controller, a display memory containing a single current screen image, other system memory, and a raster scan video display. In normal (steady-state) operation, the video controller continually reads out the contents of the display memory and transforms the information read out to the signalling necessary to control the raster scan beam while it is in its active display time. The video controller also provides the horizontal and vertical retrace signalling at appropriate intervals, and blanking of the raster scan beam during retrace.

The principal external function of CRT controllers is to output display memory addresses and to signal what type of operation is to be performed at each address. Existent CRT controllers may have simple and generic signalling of operations (for example read and write), which restricts their functionality and can make dynamic RAM interfacing complex. Or they may have signals quite specific to a particular family or set of DRAMS (for example RAS, CAS, WE), which restricts their applicability to other devices. The invention consists of a signalling scheme which provides a rich set of functions and an external PLA-type device which interprets this signalling for any of a wide variety of memory types.

SUMMARY OF THE INVENTION

The improved raster scan video controller incorporating the present invention is a chip set which has an address module and preferably at least one data module. This chip set, tentatively known as BMAP, is designed to work with an external processor which generates the instructions for the set. The major function of the address module is to generate both video addresses and update addresses, while the data modules are used to collect and integrate video data that had been read out from the display memory. The data output from the data module passes through high speed shift registers and a look-up table to the raster scan video display.

The major parts of the address module are a synchronous signal generator, a window controller, an update controller and an interface controller. The address module also has the ability to update the contents of the display memory according to instructions passed from the host system. Thus, the host system does not have to access display memory when it wants to insert characters or graphic elements into display memory. It only passes the appropriate instructions and/or data to the BMAP. The structure of the display memory is related to the operating frequency of the raster scan video display and the complexity of the system.

The principal external function of raster scan video display controllers is to output display memory addresses and to signal what type of operation is to be performed at each address. In the present invention, there is a plurality of operations which may be executed for a given address in display memory.

Each operation in display memory is defined first and most basically by two sets of outputs called TYPE1 and TYPE 2 from the video display controller which are appropriately encoded. These outputs divide memory operations into four types: 1) sequential display accesses which can be implemented through an external PLA via page mode read operations, or nibble mode or static-column mode, according to the type of display memory used; 2) random display accesses; 3) DRAM refresh cycles, which again can be implemented as appropriate for the memory; and 4) update accesses. The latter category uses the TYPE 2 and LA (local address) outputs, and is disclosed in the parallel application entitled UPDATE CACHE FOR A RASTER SCAN VIDEO CONTROLLER filed simultaneously herewith.

The invention provides the logic to generate the less significant of the two TYPE1 outputs during display accesses, that is, to distinguish between a code for sequential and a code for random accesses. Whenever a memory address is accessed that is not one higher than the previous address, the access is random. A mask register is programmed to reflect the page boundaries of the memories, so that if the address counter crosses such a boundary as it is being incremented, the first access on the new page is also random. The TYPE1, TYPE2 and LA outputs are all inputs to a PLA type device which is coded to generate the specific control and timing signals for the type of memory used. Thus, this logic generates control signals for one of four options, while the PLA generates specific memory controls based on these signals. This logic specifies what to do, the PLA specifies how to do it, based on the specific type of memory used.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a bit-mapped alphanumeric and graphic display controller with which the present invention can be used.

Figure 2 is a block diagram of a sophisticated display system using the controller of Figure 1 and the present invention.

Figure 3 is a block diagram of the structure of a display memory system used with the present invention.

Figure 4 is a block diagram of the interface controller used with the present invention.

Figure 5 is a block diagram of the display address output controller of the present invention.

Figure 6 is a block diagram of the update address output controller used with the present invention.

Figure 7 is a block diagram of an exemplary system utilizing the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

BMAP is the name of a bit-mapped raster scan video (CRT) controller chip set illustrated in Figure 1, having an address module 10 and a data module 12. This chip set provides hardware support for windows in a bit-mapped alphanumeric and graphic raster scan video (CRT) display system used in a computer system having one or more main processors and is particularly advantageous for use with multi-tasking operating systems. The hardware support includes logical circuits whereby a description of overlapping windows can be programmed into the chip set. This feature allows the CPU to maintain a multi-window bit-mapped display almost as easily as it maintains a conventional alphanumeric display.

The cross-referenced applications, which are incorporated herein by reference, disclose the address module and the data module in substantial detail.

In this specification the term "video access" is used to indicate an access that reads out the display memory contents to be displayed on the screen. The term "update access", on the other hand, indicates a memory access that is used to update the contents of the display memory. The term "update operation" refers to the transfer of information between the updating device and the registered transceivers of Figure 3. In the embodiment used to illustrate the present invention, each video access and update access consists of 16 to 256 bits, while an update operation always consists of a 16-bit word.

Figure 1 of the cross-referenced application serial No. 793,521 shows the relations between video accesses and update accesses. After the display memory address is presented, the display memory outputs the whole block of information corresponding to the display memory address. Then, preferably the data read out will go to data accumulator modules or to the shift registers directly, as described therein.

During an update operation that does not access data already present in the registered transceivers, the BMAP outputs a "local address" together with the display memory address to select a 16-bit word from the display memory. The local address is used to select the desired word from the corresponding video access. All 4 bits in the local address are needed when the BMAP is used in a system that has 8 bits per pixel and 32 pixels per video access.

Figure 2 of the cross-referenced application serial No. 793,521 shows the relations between the display address, update address, and the pixel address. The 18 most significant bits in the pixel address represent the 18 bit display memory address.

Since a 16-bit word may consist of 16 pixels for a monochrome display system, and consist of 2 pixels for a system that has 8 bits per pixel, the pixel offset can vary from 1 to 4 bit positions. Table 1 of the cross-referenced application serial No 793,521 shows the number of bits in the local address and the pixel offset for different systems.

Address Module and Date Module

Figure 1 is a block diagram of the improved video controller incorporating the present invention. This is a chip set which has an address module 10 and preferably at least one data module 12. These chips are designed to work with an external processor which generates the instructions for the set. The major parts of the address module are a synchronous signal generator 30, a window controller 40, an update controller 32 and an interface controller 34. This application is directed primarily to the interface controller of the address module. The cross-referenced application serial No. 793,526 is directed to the data module, while the cross-referenced application serial No. 793,521 is directed to the window-controller of the address module.

Figure 2 is a block diagram of a sophisticated system that includes an address module 10 and several data modules 12. The major function of the address module is to generate both display addresses and update addresses, while the data modules are used to collect and integrate the display patterns that have been read out from the display memory 13. The data output by the data module(s) then goes through the high speed shift register(s) 15 and color look-up table 17 to the video display 19.

The address module also has the ability to update the contents of the display memory 13 according to the instructions passed from the host system. Therefore, the host processor 11 does not have to access the display memory 13 when it wants to insert characters or graphic elements into the display memory. Instead, it only needs to pass appropriate instructions and/or data to the address module 10.

After receiving the instructions and/or data passed from the host system, the address module executes them one by one as a special purpose microprocessor. Since the whole procedure is controlled by the internal hardware, instructions can be done within a very short time. Typically the insertion speed is 5 to 50 times faster than a software procedure on the host processor.

The data module 12 has 32 data inputs and 8 data outputs. By setting the appropriate control inputs, one or more data modules can be used in various kinds of applications. All systems that use sequential memory access to increase the data read out speed, have to include the data module (or equivalent hardware) in the back-end.

The structure of the display memory 13 is related to the operating frequency of the raster scan video display and the complexity of the system. Figure 3 shows a typical memory structure that can be used with BMAP chip set.

The principal external function of video controllers is to output display memory addresses and to signal what type of operation is to be performed at each address. Existent CRT controllers may have simple and generic signalling of operations (for example read and write), which restricts their functionality and can make dynamic RAM interfacing complex. Or they may have signals quite specific to a particular family or

set of DRAMS (for example RAS, CAS, WE), which restricts their applicability to other devices. The invention consists of a signalling scheme which provides a rich set of functions, logic to generate this signalling, and an external PLA-type device which interprets this signalling for any of a wide variety of memory types.

The invention generates control signals for conversion by a PLA for access to specific memory types. Each operation in display memory is defined first and most basically by two sets of outputs called TYPE1 and TYPE 2 from the video controller which are encoded as shown in Table 1. These outputs divide memory operations into four types: 1) sequential display accesses which can be implemented through the external PLA via page mode read operations, or nibble mode or static-column mode, according to the type of display memory used; 2) random display accesses; 3) DRAM refresh cycles, which again can be implemented as appropriate for the memory; and 4) update accesses. The latter category uses the TYPE2 and LA outputs, and is covered by a parallel application filed simultaneously herewith.

The circuit in Figure 5 is used to generate the less significant of the two TYPE1 outputs during display accesses, that is to distinguish between the 00 code for sequential access and the 01 code for random access. Whenever a new address is loaded (via LOAD 0), the next access is random. Also, the mask register is programmed to reflect the page boundaries of the memories, so that if the address counter crosses such a boundary as it is being incremented, the first access on the new page is also random. The TYPE1, TYPE2 and LA outputs are all inputs to a PLA type device which is coded to generate the specific external control signals for the type of memory used.

Memory Interfaces

The function of the display address and update address output controller blocks in Figure 4 is to generate the "TYPE" outputs corresponding to the address sent out from the window controller 40 and/or the update controller 32. There are two sets of "TYPE" output, which are related to two of the address ports respectively.

Interface for Video Access

Video accesses are controlled by the 18-bit address and the "TYPE1" outputs. As described in the cross-referenced application serial No. 793,521, the video access is a display memory access that can read out all the information stored in the location pointed by the 18-bit address. The time sharing situation of the address port is described in that application.

The window controller 40 generates 4 types of operations which are described in a parallel application filed simultaneously herewith. All the operations, except the "H Resync", have to access the display memory directly. Figure 5 shows the structure of the display address output controller.

Referring to Figure 5, the 8-bit mask register is used to define the page size of the DRAM, while the 8 2-1 MUXs and the zero detector are used to detect the page boundary. The 19-bit latch is part of the single stage pipeline structure. It is used to store the next display address, such that there is enough time to generate the VAEND signal for the non-intermediate video access.

Table 1 shows 4 types of memory accesses that relate to the 18-bit address port. The 2-bit "TYPE1" output is used to direct the external PLA to generate the corresponding DRAM control signals.

TYPE1 OUTPUT	Type of Access	Address Port*	Description
00	Sequential READ	A,(B)	Sequential Video Access or Vertical Resync Access
01	Random READ	A,(B)	Random Video Access or Vertical Resync Access
10	DRAM Refresh	A	DRAM Refresh Cycle
11	Read-Modify -Write	(A),B	Update Access

*A : 18-bit Address Port
B : 4-bit Local Address Port
() : Depend on Type 2 Output

Table 1 TYPE1 Control Output

The display memory access is started by the rising edge of the AS* (address strobe) signal and terminated.

Interface for Update Access

The update access is controlled by an 18-bit address, supplied by the window controller (disclosed in a parallel application field simultaneously herewith) of the address module, the local address and the "TYPE2" outputs. The need for the 18-bit address depends on the type of update access. The update controller 32 generates three kinds of operations. Two of them have to access either the display memory or the system memory. The hardware that is used to generate the local address and the "TYPE2" outputs is shown in Figure 6.

As shown in Figure 6, the 4-bit address port is used to output one of the local addresses stored in the PC (program counter), DC (destination counter) and Sc (source counter). The 4-bit mask register 60 is used to define the address boundary for the external transceivers/registers 14. If the update operation access refers to the "first" word of an update access, the BMAP has to read the destination pattern from the display memory, latch the data in the transceivers/registers 14, and read the required 16 bits of the latched data.

If the update operation refers to the "last" word of an update access, the BMAP has to combine the write operation with the access that writes the whole data block from the transceivers/registers 14 back to the display memory 13.

If the update operation is the first and the last operate of a certain update access, the BMAP performs a read-modify-write operation to the display memory 13 directly. Table 2 shows 8 kinds of access that relate to the output controller.

TYPE2 OUTPUT	Type of Access	Address Port	Description
000	R-M-W to T/R	B	Intermediate Destination Access
001	R-M-W to Memory	A, B	First Destination Access
010	R-M-W to Memory	A, B	Last Destination Access
011	R-M-W to Memory	A, B	First and Last Destination Access
100	Read from Memory	A, B	Read Instruction
101	R-M-W to Memory	A, B	Write Instruction
110	Read from Memory	A, B	Source Pattern Access
111	Read from Memory	A, B	Vertical Resync Access

Table 2 TYPE2 Control Output

The three TYPE2 outputs are also connected with the external PLA 54, such that the corresponding DRAM 13 (display memory) and transceiver/register 14 control signals can be generated to do the update access. Both the "TYPE2" and "local address" outputs are qualified by the LAS* (local address strobe) signal and negated by the LDTACK* (local address acknowledge) signal, as in the display memory access cycle.

Claims

1. Generalized operation-signalling logic for use in accessing the memory of a computer system for indicating what type of operation is to be performed at each memory address to be accessed, comprising:
a memory having a plurality of signals on which data can be read or written;
one or more devices which can generate specific memory addresses and signals indicating the operation to be performed at each of said memory addresses;
means to define the type of operation to be performed at each memory address and to signal said type of operation together with said memory address;
programmable means to convert the type of operation signals into specific control signals required by a specific memory device.

2. Generalized operation-signalling logic for use in accessing the display memory of a computer system for indicating the type of operation to be performed at display memory address, comprising:
a display memory having one or more signals on which data can be read or written;
a display controller which generates and outputs display memory addresses and signals indicating the type of operation to be performed at each display memory address;
means to define the type of operation to be performed at each of said display memory addresses;
means for said display controller to signal said type of operation along with said display memory address;
programmable means to convert the type of operation to be signalled to display memory into specific control signals required by a specific memory device.

3. The operation-signalling logic of Claim 1 wherein said memory is a display memory.

4. The operation-signalling logic of Claim 1 wherein said device which can generate specific memory addresses is a display controller and wherein said memory is a display memory.

5. The operation-signalling logic of Claims 1 or 2 wherein the means to define types of operation includes a mask register in the display address output controller of said display interface of said display controller.

6. The operation-signalling logic of Claims 1 or 2 wherein said types of operations include random accesses and sequential accesses.

7. The operation-signalling logic of Claim 2 wherein said types of operations include:
sequential display accesses;
random display accesses;
dram refresh cycles; and
update cycles.

8. The operation-signalling logic of Claims 1, 2 or 3 wherein the means to convert the type of operation signalled into the specific control signals required by a specific memory device is a programmed logic array.

9. The operation-signalling logic of Claims 2 and 7 wherein the means to convert the type of operation signalled into the specific control signals required by a specific display memory device further includes a mask register to identify memory address boundaries for sequential accesses.

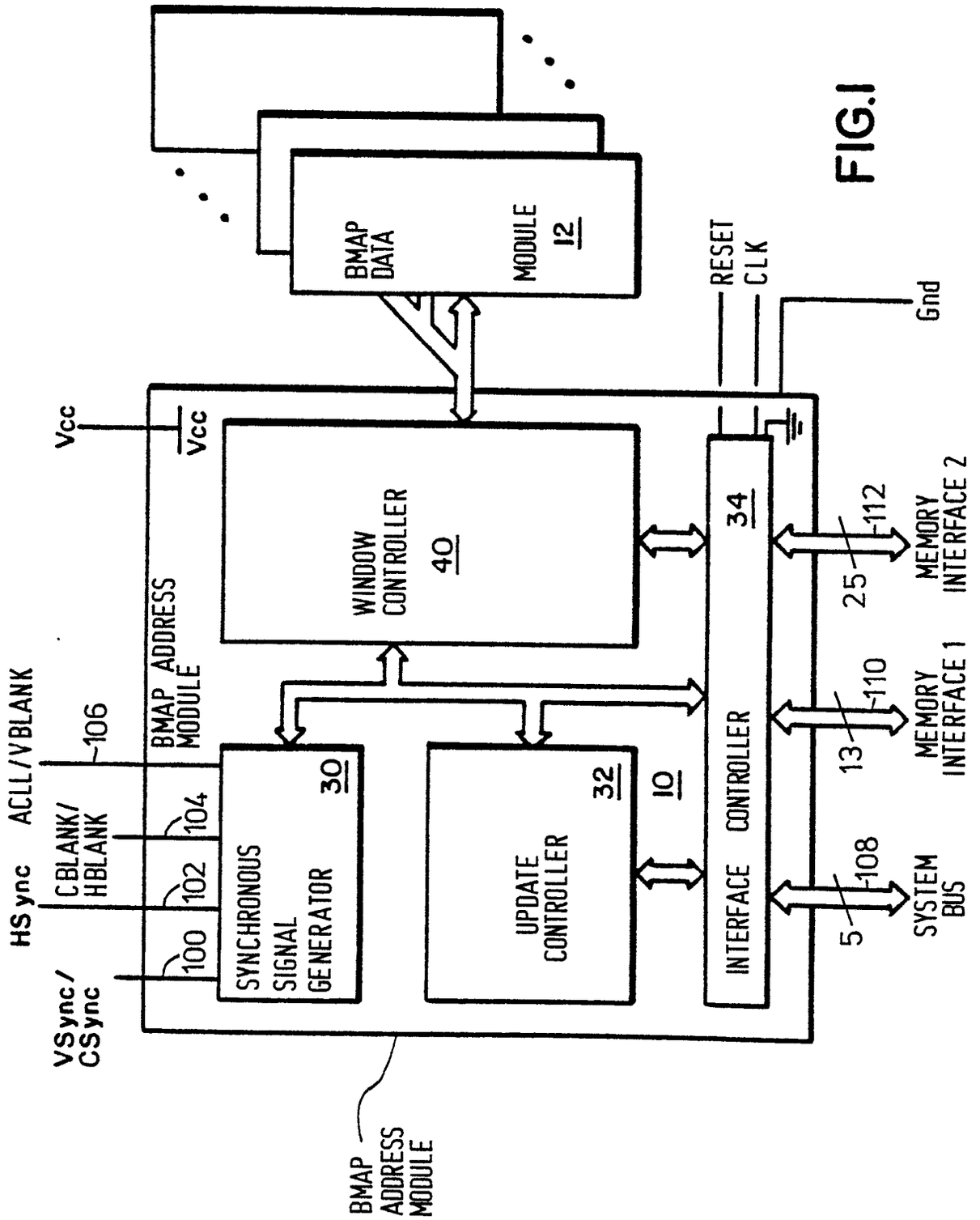

BMAP DATA
MODULE 12
RESET
CLK
Gnd
Vcc
Vcc
WINDOW CONTROLLER 40
34
112
25
MEMORY INTERFACE 2
BMAP ADDRESS MODULE
106
ACLL/VBLANK
HSync
CBLANK/ HBLANK
VSync/ CSync
104
102
100
SYNCHRONOUS SIGNAL GENERATOR 30
UPDATE CONTROLLER 32
10
INTERFACE CONTROLLER
110
13
MEMORY INTERFACE 1
108
5
SYSTEM BUS
BMAP ADDRESS MODULE

FIG.1

FIG.2

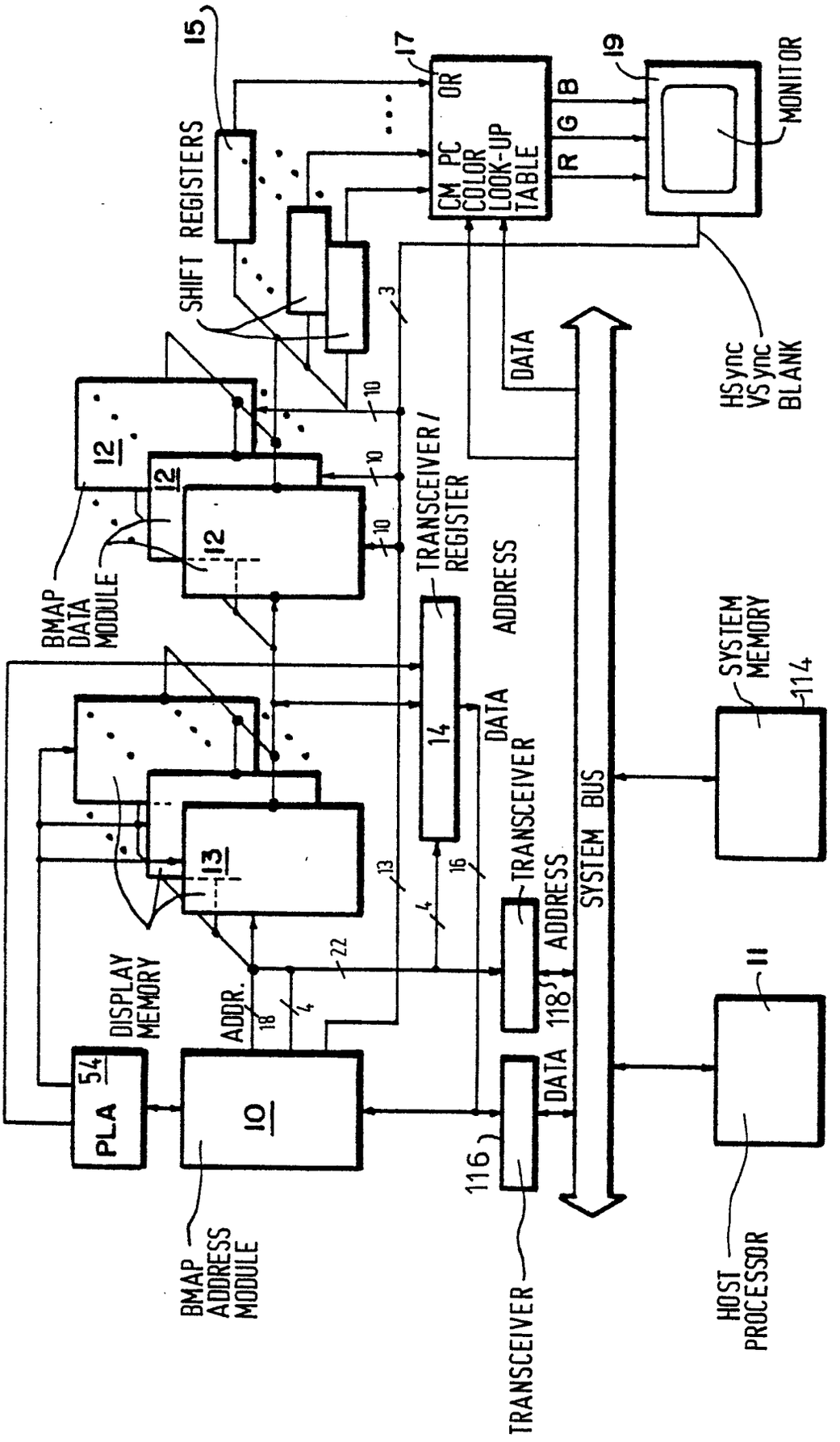
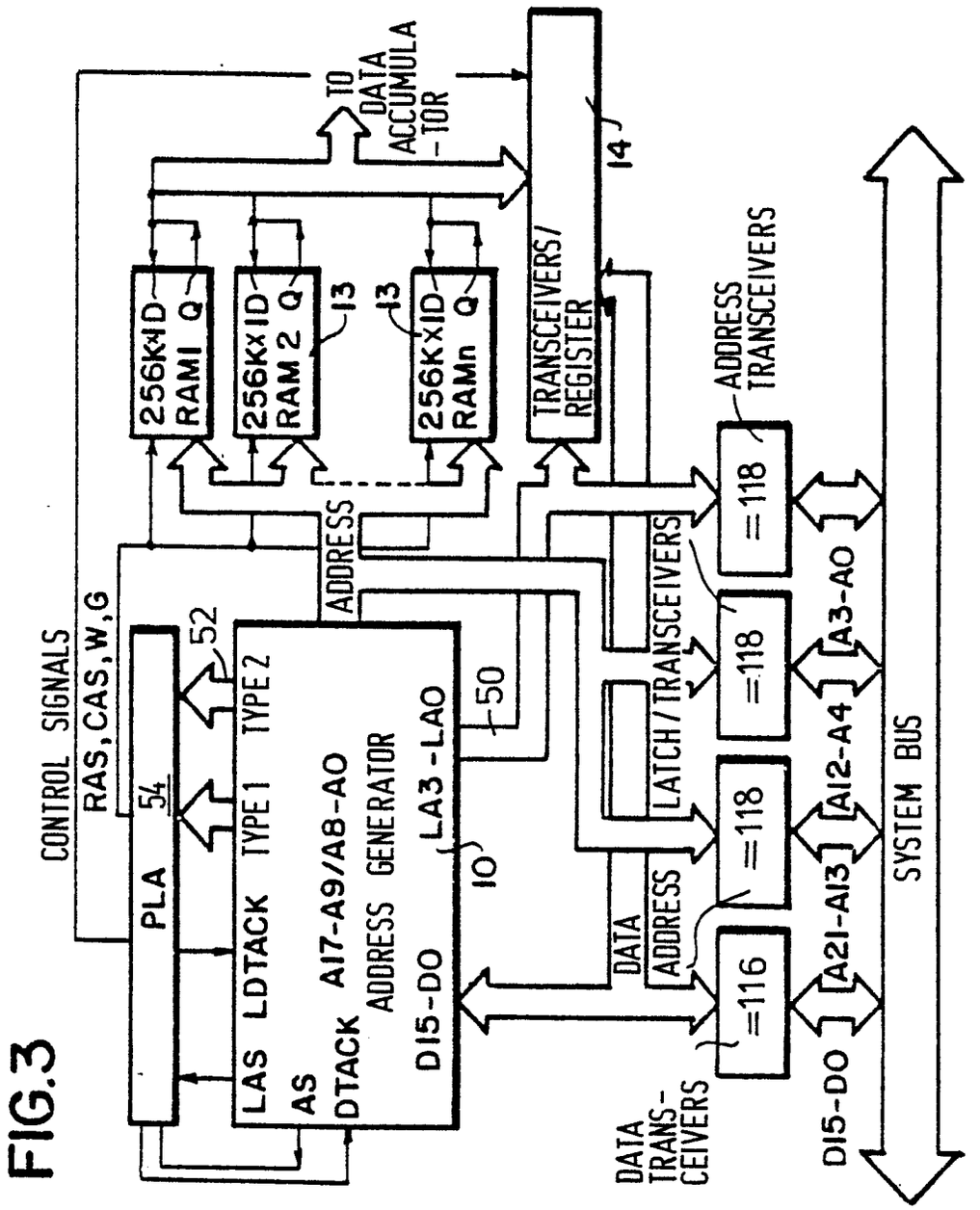

15
SHIFT REGISTERS
17
CM PC COLOR LOOK-UP TABLE
OR
G
B
R
19
MONITOR
HSync
VSync
BLANK
DATA
3
10
12
BMAP DATA MODULE
TRANSCEIVER / REGISTER
ADDRESS
14
DATA
TRANSCEIVER
16
4
13
SYSTEM BUS
SYSTEM MEMORY
114
TRANSCEIVER
116
DATA
118
ADDRESS
11
HOST PROCESSOR
22
ADDR.
18
4
DISPLAY MEMORY
PLA
54
10
BMAP ADDRESS MODULE

FIG.3


CONTROL SIGNALS
RAS, CAS, W, G
PLA
54
52
TYPE 1
TYPE 2
LAS LDTACK
AS
DTACK
A17-A9/A8-A0
ADDRESS GENERATOR
D15-D0
LA3-LA0
50
10
ADDRESS
256K×1D RAM1 Q
256K×1D RAM2 Q
13
13
256K×1D RAMn Q
TO DATA ACCUMULA-TOR
TRANSCEIVERS/ REGISTER
14
ADDRESS TRANSCEIVERS
=118
=118
=118
=116
LATCH/TRANSCEIVERS
DATA
ADDRESS
DATA TRANS-CEIVERS
A3-A0
A12-A4
A21-A13
D15-D0
SYSTEM BUS

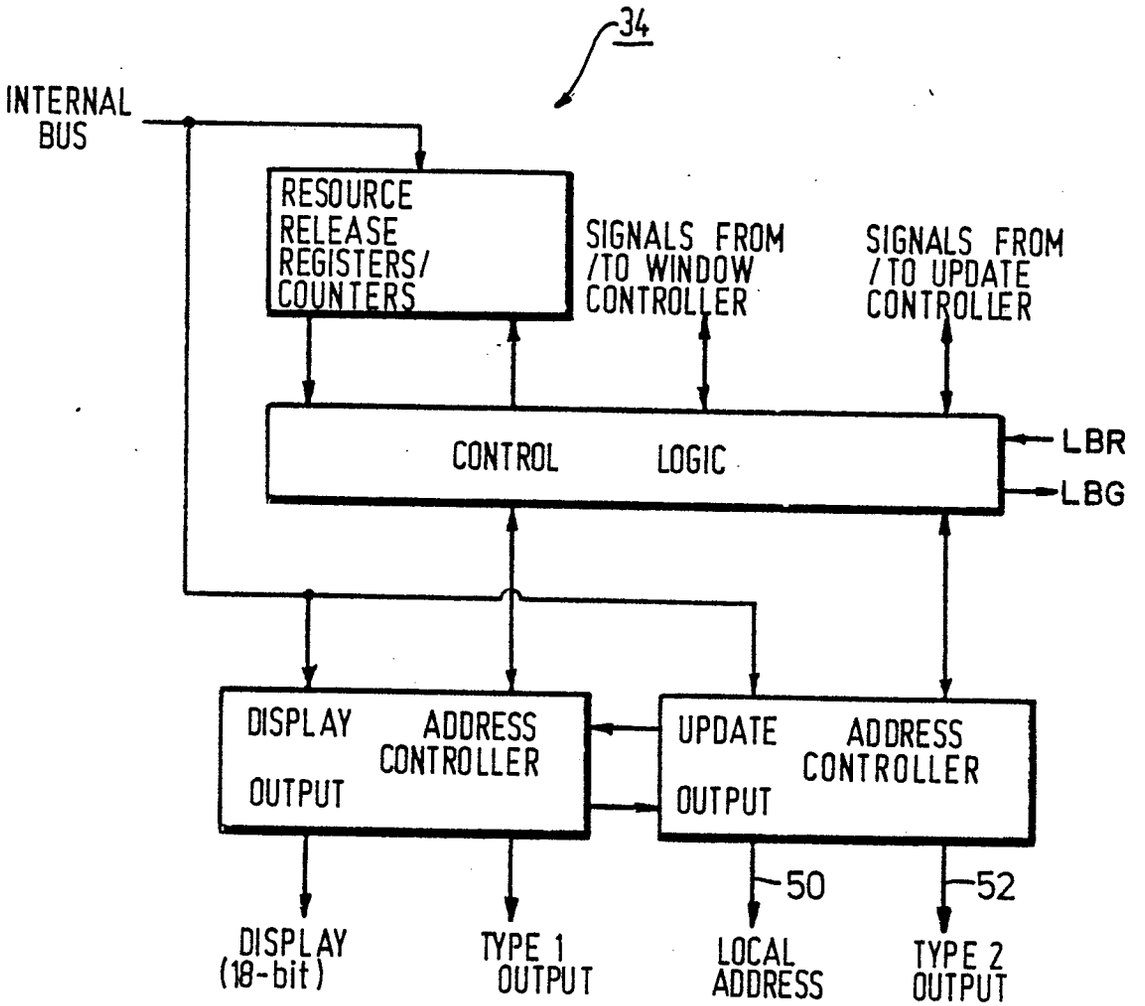

34
INTERNAL BUS
RESOURCE RELEASE REGISTERS/ COUNTERS
SIGNALS FROM /TO WINDOW CONTROLLER
SIGNALS FROM /TO UPDATE CONTROLLER
CONTROL LOGIC
LBR
LBG
DISPLAY OUTPUT
ADDRESS CONTROLLER
UPDATE OUTPUT
ADDRESS CONTROLLER
50
52
DISPLAY (18-bit)
TYPE 1 OUTPUT
LOCAL ADDRESS
TYPE 2 OUTPUT

FIG.4

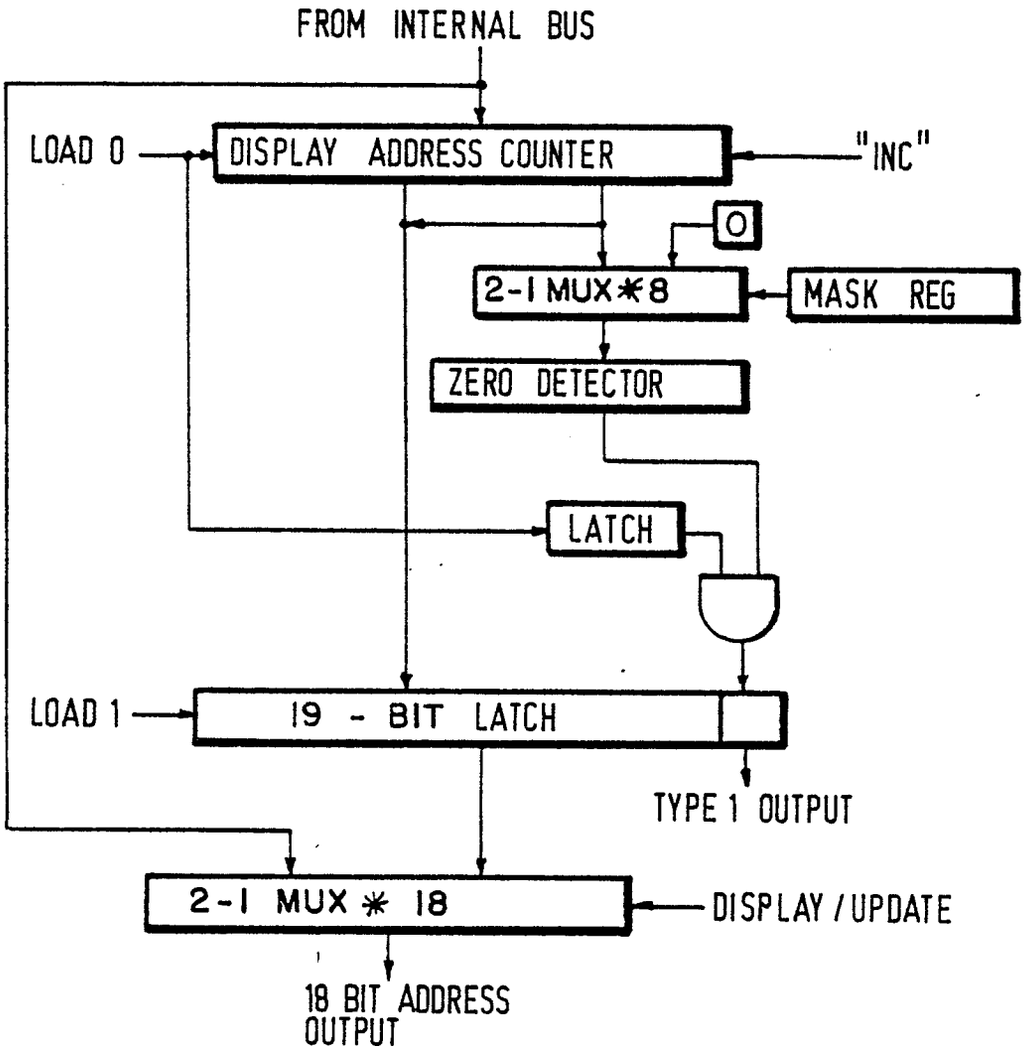
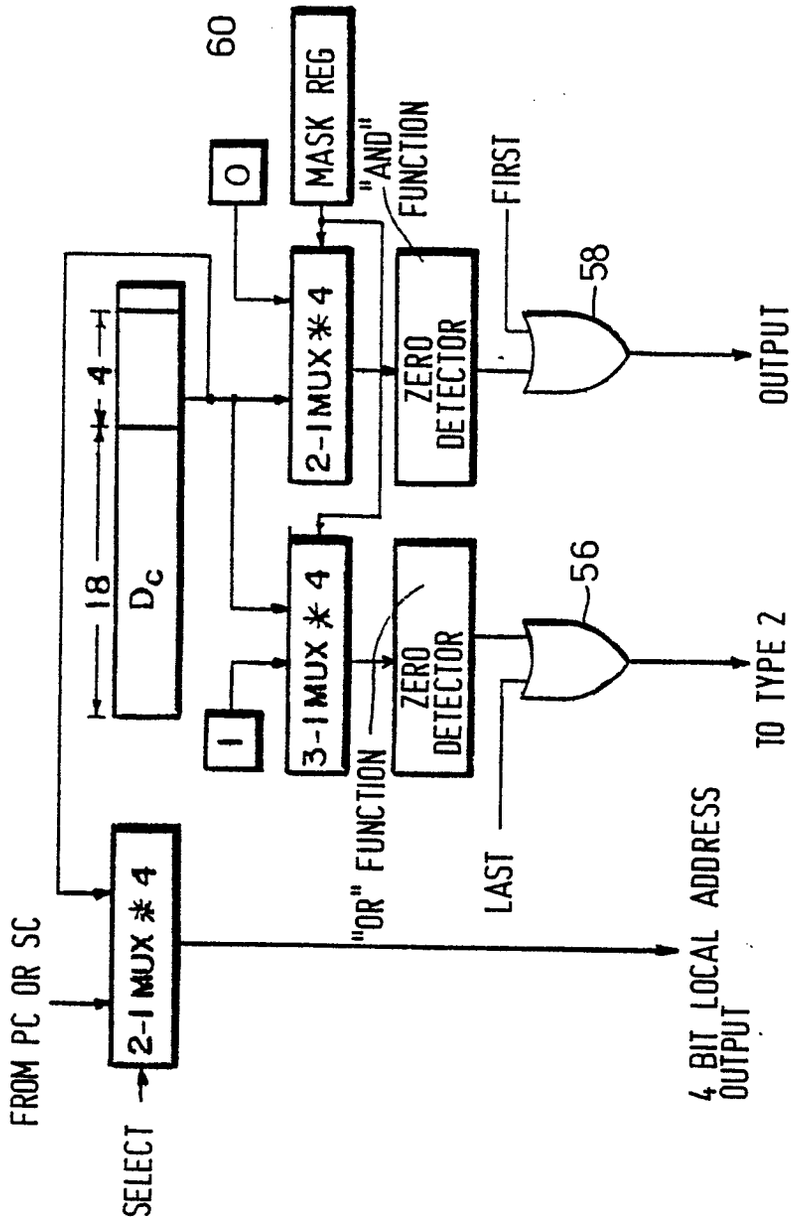

FROM INTERNAL BUS
LOAD 0
DISPLAY ADDRESS COUNTER
"INC"
0
2-1 MUX*8
MASK REG
ZERO DETECTOR
LATCH
LOAD 1
19 - BIT LATCH
TYPE 1 OUTPUT
2-1 MUX * 18
DISPLAY / UPDATE
18 BIT ADDRESS OUTPUT

FIG.5

FIG.6


FROM PC OR SC
SELECT
2-1 MUX * 4
18
4
D_c
1
0
60
3-1 MUX * 4
2-1 MUX * 4
MASK REG
"AND" FUNCTION
"OR" FUNCTION
ZERO DETECTOR
ZERO DETECTOR
LAST
FIRST
56
58
4 BIT LOCAL ADDRESS OUTPUT
TO TYPE 2
OUTPUT

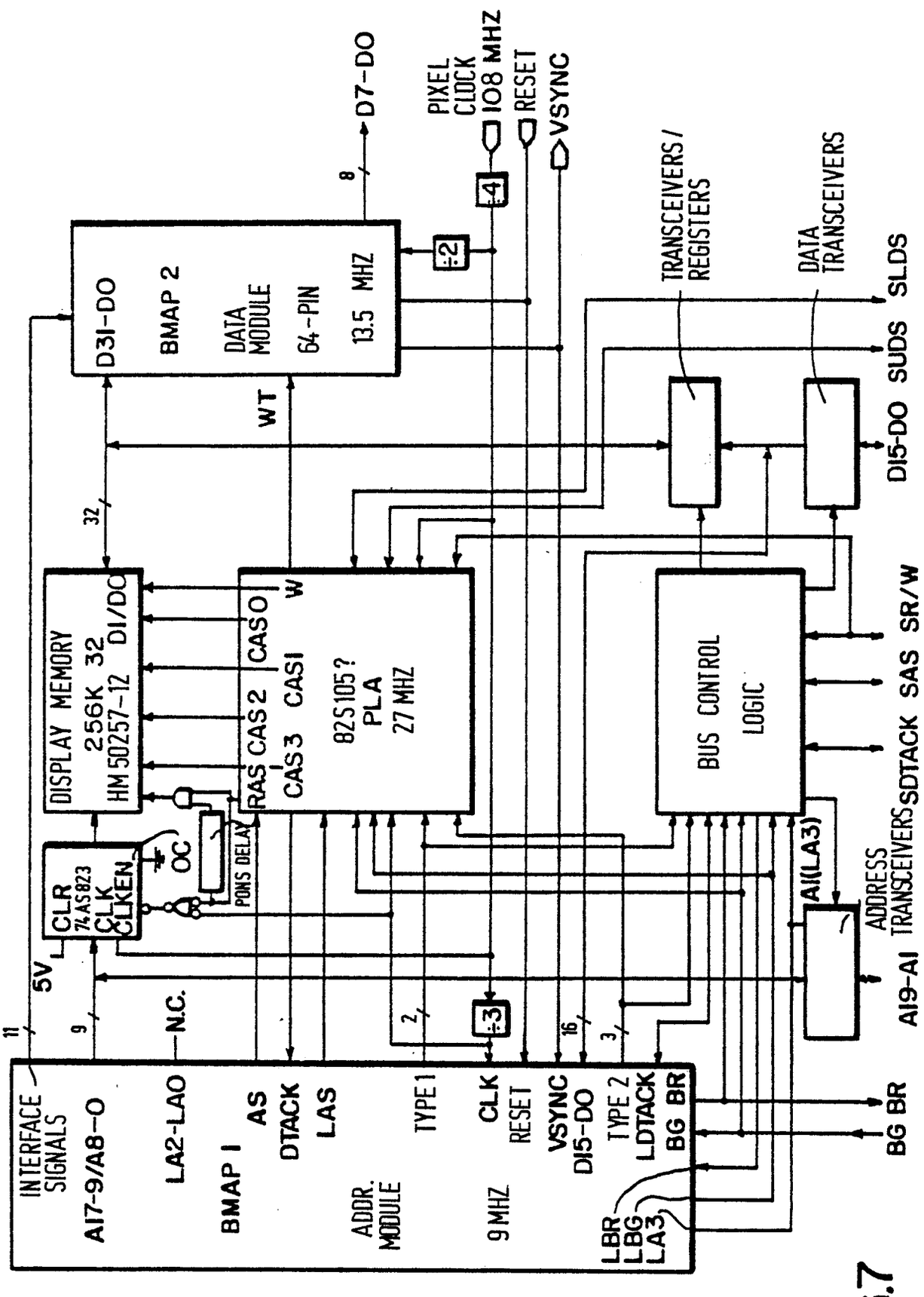

INTERFACE SIGNALS
A17-9/A8-0
LA2-LA0
BMAP 1
AS
DTACK
LAS
ADDR. MODULE
TYPE1
CLK
RESET
9 MHZ
VSYNC
DI5-DO
TYPE 2
LDTACK
BG BR
LBR
LBG
LA3
11
9
2
16
3
5V
N.C.
CLR 74AS823
CLK
CLKEN
OC
PONS DELAY
DISPLAY MEMORY
256K 32
HM 50257-12 DI/DO
32
RAS CAS2 CAS0
CAS3 CASI W
82S105?
PLA
27 MHZ
WT
D31-DO
BMAP 2
DATA MODULE
64-PIN
13.5 MHZ
8
D7-DO
÷2
÷4
÷3
PIXEL CLOCK
108 MHZ
RESET
VSYNC
TRANSCEIVERS / REGISTERS
DATA TRANSCEIVERS
DI5-DO SUDS SLDS
BUS CONTROL LOGIC
SDTACK SAS SR/W
A1(LA3)
ADDRESS TRANSCEIVERS
A19-A1
BG BR

FIG.7