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(54) **Integrated thermal ink jet printhead and method of manufacture.**

(57) This application discloses a novel thermal ink jet printhead and related integrated pulse driver circuit useful in thermal ink jet printers. This combined printhead and pulse drive integrated circuit includes a first level (5,6) of metallization comprising a refractory metal which is patterned to define the lateral dimension of the printhead resistor (4). A passivation layer or layers (7,8,9) are deposited atop this first level of metalization and patterned to have an opening or openings therein for receiving a second level (10,11) of metalization. This second level (10,11) of metallization such as aluminium may then be used for electrically interconnecting the printhead resistors to MOSFET drivers and the like which have been fabricated in the same silicon substrate (1) which provides suport for the printhead resistors. Thus, this "on-chip" driver construction enables these pulse driver transistor to be moved from external electronic circuitry to the printhead substrate.

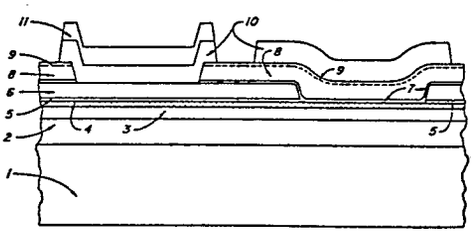

Fig 1

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Description

INTEGRATED THERMAL INK JET PRINTHEAD AND METHOD OF MANUFACTURE

This invention relates generally to thermal ink jet printing and more particularly to a novel thermal ink jet printhead with improved resistance to ink penetration and corrosion and cavitation wear. This invention is also directed to a novel integrated circuit which combines printhead interconnect metalization with MOS pulse drive circuit metalization in a unique multilevel metal MOS integrated circuit structure.

Thermal ink jet printing has been described in many technical publications, and one such publication relevant to this invention is the Hewlett Packard Journal, Volume 36, Number 5, May 1985, incorporated herein by reference.

In the manufacture of thermal ink jet printheads, it is known to provide conductive traces of aluminum over a chosen resistive material, such as tantalum-aluminum, to provide electrical lead-in conductors for conducting current pulses to the lithographically defined heater resistors in the resistive material. These conductive traces are formed by first sputtering aluminum on the surface of a layer of resistive material and thereafter defining conductive trace patterns in the aluminum using conventional photolithographic masking and etching processes.

It is also known in this art to deposit an inert refractory material such as silicon carbide or silicon nitride over the aluminum trace material and the exposed resistive material in order to provide a barrier layer between the resistive and conductive material and the ink. This ink is stored in individual reservoirs and heated by thermal energy passing from the individually defined resistors and through the barrier layer to the ink reservoirs atop the barrier layer. The ink is highly corrosive, so it is important that the barrier layer be chemically inert and highly impervious to the ink.

In the deposition process used to form the barrier layer for the above printhead structure, rather sharply rounded contours are produced in the barrier layer material at the edges of the conductive aluminum traces. These contours take the form of rounded edges in the silicon carbide layer which first extend laterally outward over the edges of the aluminum traces and then turn back in and down in the direction of the edge of the aluminum trace at the active resistor area. Here the silicon carbide barrier material forms an intersection with another, generally flat section of silicon carbide material which is deposited directly on the resistive material. This intersection may be seen on a scanning electron microscope (SEM) as a crack in the barrier layer material which manifests itself as a weak spot or area therein. This weak spot or area will often become a source of structural and operational failure when subjected to ink penetration and to cavitation-produced wear from the collapsing ink bubble during a thermal ink jet printing operation.

In addition to the specific problem with the above prior art approach to thin film resistor substrate fabrication, it has been found that, in general, thin films and Fluidic cavities in these structures which have been optimized for superior printing speed and print quality suffer from short printing resistor operating life. This is especially true when large over-energy tolerance is required. Resistor aging curves taken throughout the printing life of a thermal ink jet heater resistor reveal strongly two mechanisms which contribute to the early demise of the heater resistor. One is rapid resistor value increase due to electrochemical and mechanical interactions near the resistor terminations. The second is a slow but continuous increase of the resistance caused by the interface oxidation with the thermal standoff layer and a passivation layer. Simply stated, any mechanism contributing to the increase of the resistor value in ohms is a mechanism that leads toward the final resistor failure when its value is infinite.

Accordingly, the general purpose of this invention is to provide a new and improved thermal ink jet printhead structure and method of manufacture which, among other things, eliminates the above cracks in the barrier layer material and thus overcomes the associated problems of ink penetration through and undue cavitation wear in the barrier layer. To accomplish this purpose, the resistive heater layer for the printhead structure is formed of either polycrystalline silicon or a refractory silicide, such as tantalum silicide or titanium silicide or tungsten silicide or molybdenum silicide. Thereafter, conductive trace material of a refractory metal such as tungsten or molybdenum is deposited on the resistive heater layer. Then, a barrier layer of silicon dioxide is deposited over the conductive trace material using chemical vapor deposition (CVD) techniques and then reflowed to form smooth contours in the area of the barrier layer above the edges of the conductive trace material. Finally, an outer protective metal layer such as tantalum is sputtered on top of the reflowed silicon dioxide barrier layer material to provide even further isolation against ink penetration and cavitation-produced wear of the structure.

In a modified embodiment of my invention, the above novel printhead structure is integrated with pulse drive circuitry, such as metal-oxide-silicon-field-effect transistor (MOSFET) drivers, in a novel multi-level metal integrated circuit. In this integrated circuit, a first level of metalization comprises a refractory metal such as tungsten, titanium, tantalum or molybdenum which is patterned to define one dimension of a printhead resistor in a resistive layer on which it lies. A passivation layer or layers are deposited on the first level of metalization and selectively etched to provide an opening or openings therein. Then, a second level of metalization, such as aluminum, is deposited in this opening or openings to make electrical contact with the first level of metalization and thereby provide an interconnect path between the printhead resistor and MOSFET pulse drive circuitry and the like. Thus, MOS or even bipolar transistors or other semiconductor devices may be fabricated in one area of a silicon substrate and printhead resistors defined in another area atop the surface of the same silicon

substrate. Then, using the above multi-level interconnect scheme, aluminum interconnects from the output of these transistors may be connected to the refractory metal connections which lead into the various printhead resistors in novel MOSFET driver-ink jet printhead integrated circuit construction.

The advantages and novel features of the above summarized printhead structure and integrated circuit will become better understood and appreciated with reference to the following description of the accompanying drawings.

Figure 1 is a schematic cross section view of the printhead device structure according to a preferred embodiment of the invention.

Figures 2A through 2G illustrate schematically the processing sequence used in the manufacture of the printhead structures in Figure 1.

Referring now to Figure 1, the printhead device structure according to a preferred embodiment of the invention will be initially described by identifying the various layers therein. Then, with reference to Figure 2A through 2G, the various process steps utilized in achieving this device structure will be described in more detail.

In Figure 1, the printhead substrate starting material 1 is silicon and has a surface thermal isolation layer 2 of silicon dioxide thereon. A silicon nitride layer 3 is deposited on the surface of the silicon dioxide layer 2, and then a resistive layer 4 of tantalum silicide is deposited on the surface of the silicon nitride layer 3 to provide the layer material for the resistive heater elements in a geometry to be further described.

The next two layers 5 and 6 are both tungsten, and a layer of silicon nitride 7 is formed on the top surface of the second and thicker layer 6 of tungsten and photolithographically defined in the geometry shown to determine the lateral extent of the heater resistor. Next, a layer 8 of phosphosilicate glass is formed atop the silicon nitride layer 7, and then another layer of more lightly doped phosphorous glass 9 is formed on the previous glass layer 8. The dielectric passivation layers 7, 8 and 9 are now appropriately etched using a dry etchant such as SF_6 and argon.

A layer 10 of tantalum is deposited atop the glass layer 9 and then a further conductive layer 11 of aluminum is deposited onto the tantalum layer 10. These interconnection layers 10 and 11 are subsequently etched to define the two surface barriers for the heater resistor and the interconnect pad, respectively, on the right and left hand sides of the device structure. These conductive layers 10 and 11 on the left hand side of Figure 1 serve as an electrical interconnection to other electronics, such as pulse drive circuitry for the heater resistors designed in layer 4. Thus, the heater resistors in Figure 1 may be electrically connected by way of tungsten layers 5 and 6 and through the conductors 10 and 11 on the interconnect pad side of the structure in a metal-oxide-silicon (MOS)-printhead integrated circuit of novel construction. For example, the metal contact 11 may be extended in the form of a strip of metallization to the output or drain terminal of a MOS driver field-effect transistor which operates as an output device of a particular MOS pulse drive circuit.

Referring now to Figures 2A through 2G, the silicon substrate 1 will typically be 15 to 25 mils in thickness and of a resistivity of about 20 ohm centimeters and will have a layer 2 of thermal silicon dioxide of about 1.6 microns in thickness thereon as shown in Figure 2A.

In Figure 2B there is shown a thin 0.1 micron silicon nitride, Si_3N_4, layer 3 which is deposited on the SiO_2 layer 2 by low pressure chemical vapor deposition (LPCVD). This and other similar processes referred to herein are generally well known in the semiconductor processing arts and are disclosed for example by A. B. Glaser, et al. in a book entitled Integrated Circuit Engineering Design, Fabrication and Application, Addison-Wesley, 1979 at page 237, incorporated herein by reference.

Next, as shown in Figure 2C, a resistive layer 4 is formed on the Si_3N_4 layer 3 by sputtering tantalum sili cide to a thickness of between 500 and 1000 angstroms, and this step is followed by the sputtering of a layer 5 of tungsten to a thickness of about 250 angstroms. Next, a thicker, lower resistivity tungsten layer 6 is grown on the thin tungsten layer 5 to a thickness of about 0.5 microns by using chemical vapor deposition (CVD). Then, after etching the conductive and resistive layers 4,5, and 6 previously deposited and in the geometry shown, plasma enhanced chemical vapor deposition (PECVD) is used to deposit a layer 7 of silicon nitride, SiN_xH_y, of approximately 1000 angstroms in thickness on the surface of the tungsten layer 6 as shown in Figure 2D. These PECVD processes are known to those skilled in the semiconductor processing arts and are described, for example, by R. F. Bunshah et al in an book entitled Deposition Technologies for Films and Coatings, Noyes Publications, 1982, page 376 et seq, incorporated herein by reference.

In the next step shown in Figure 2D, a layer 8 of phosphorous doped glass, SiO_2, doped to approximately 8 percent phosphorous content is formed by chemical vapor deposition (CVD) in the contour shown, whereafter the structure is annealed for approximately 15 minutes at 1000° C to stablize a tantalum silicide resistive layer 4 and to reflow the phosphorous doped or phosphosilicate glass (PSG) over the resistor terminations. Then, a layer 9 of phospho silicate glass is formed on the surface of layer 8 to a thickness of about 2000 angstroms and doped at 4 percent phosphorous content. This PSG layer 9 is shown in Figure 2E and serves to inhibit the formation of phosphoric acid which could attack subsequently applied aluminum final conductors.

At this point in the process, the triple layer passivation (7, 8 and 9) is dry etched down to the CVD tungsten layer as shown at reference number 6 in Figure 2F. Then, cavitation barrier 10 to tantalum and the final aluminum interconnect layer 11 are sputtered respectively to thicknesses of about 0.6 microns and 0.4 microns. These steps are illustrated schematically in Figure 2G and complete the resultant structure which corresponds identically to the composite integrated circuit structure of Figure 1. The pad or interconnect layers 10 and 11 are patterned by wet chemical etching techniques to define the device geometry shown in

Figure 2G.

Thus, there has been described a novel printhead device structure and method of manufacture wherein refractory local interconnect metalization, to wit: tungsten, allows high temperature reflow of the subsequently deposited phosphorous doped silicon (PSG) glass, thereby sealing the resistor electrode terminations. Silicon nitride films are formed above and below the resistor film and thus serve as effective oxidation barriers while the overlying silicon nitride serves as an additional moisture barrier. The refractory silicide resistor film exhibits superior high temperature stability as well as the ability to anneal the structure up to 1100° C before applying the interconnect metalization.

The above structure and its silicide layer are compatible with integrated circuit processing and allow the building of the resistor, conductor and passivation layers after the resistor logic and drive transistors have been fabricated. One very significant advantage of this invention is the fact that a single common semiconductor substrate such as silicon may be used for the fabrication of MOS or bipolar driver transistors in one area of the substrate and for the fabrication of thermal ink jet printhead resistors in another area of the substrate. Then these devices may be interconnected using the above described multi-level metal interconnect scheme.

There are many technical references on the per se use of silicides as the gate level interconnect material for MOS devices, and such interconnect techniques were discussed in detail at the 1985 Semicon/East conference in Boston, Massachusetts in September of 1985. In addition, for further reference to certain other applications, treatment, and deposition of silicides, tungsten metalization and phosphosilicate glass (PSG), reference may be made to the following technical articles, all of which are incorporated herein by reference:

TECHNICAL REFERENCES

Tungsten Metalization

N. Susa, S. Ando, S. Adachi, Journal of the Electrochemical Society, Vol. 132, No. 9, p. 2245

M. L. Green, R. A. Levy, Journal of the Electrochemical Society, Vol. 132, No. 5, p. 1243

Silicides

T. P. Chow, W. Katz, R. Goehner, G. Smith, Journal of the Electrochemical Society, Vol. 132, No. 8, p. 1914

M. Tamielian, S. Blackstone, Journal of the Electrochemical Society, Vol. 132, No. 6, p. 1487

R. A. Levy, P. K. Gallagher, Journal of the Electrochemical Society, Vol. 132, No. 8, p. 1986

S. P. Murarka, "Silicides for VLSI Applications", Academic Press, NY (1983)

T. P Chow, IEEE Electron Devices, ED-30, 1480 (1983)

Phosphosilicate Glass (PSG)

K. Nassau, R. A. Levy, D. L. Chadwick, Journal of the Electrochemical Society, Vol. 132, No. 2, p.409

The following table lists the formation method, thickness and physical properties of the various layers of my preferred embodiment in accordance with the best mode known to me at the present time for practicing the invention.

TABLE OF THIN-FILM MATERIALS AND PROPERTIES

FILM	FORMATION METHOD	THICKNESS	PHYSICAL PROPERTY
SiO2	thermal oxidation	16000 A	index of refraction 1.46
Si3N4	LPCVD	1000 A	index of refraction 2.01
TaSix	co-sputter/sinter	~750 A	sheet resistance 37 ohm/square
W	sputter	250 A	sheet resistance 8 ohm/square
W	LPCVD	5000 A	sheet resistance 0.14 ohm/square
SiNxHy	PECVD	1000 A	index of refraction 2.00
SiO2/8%P	CVD	8000 A	index of refraction ~1.46
SiO2/4%P	CVD	2000 A	index of refraction ~1.46
Ta	sputter	6000 A	sheet resistance 2.7 ohm/square
Al/4%Cu	sputter	4000 A	sheet resistance 0.12 ohm/square

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Claims

1. A process for fabricating a printhead structure for a thermal ink jet printhead which includes providing a substrate support member (1), and then depositing in succession a resistive heater layer material and a conductive trace pattern to define the lateral extent of a plurality of heater resistors, **characterized** by the combination of depositing a layer (4) of resistive material atop the substrate support member and selected from the group consisting of polycrystalline silicon and a refractory silicide, and then forming a conductive pattern (5,6) of a refractory metal on the surface of said resistive material (4) for providing a path for drive current to predefined areas in said resistive material.

2. The process defined in claim 1, **characterized** in that said refractory silicide (4) is selected from the group consisting of tantalum silicide, titanium silicide, tungsten silicide and molybdenum silicide, and said refractory metal (5,6) is selected from the group consisting of tantalum, titanium, tungsten and molybdenum.

3. The process defined in claims 1 or 2, **characterized** by the formation of a multi-level metal integrated circuit including the step of forming a metal interconnect (10,11) between a metal-oxide-semiconductor (MOS) driver circuit and said refractory metal (5,6), said refractive metal extending between said electronic device and said MOS driver circuit.

4. An electronic device comprising a supporting substrate (1), a resistive heater layer disposed above said substrate and a conductive trace pattern disposed on said resistive heater layer to define the lateral extent of a plurality of heater resistors in the resistive heater layer, **characterized** in that a layer (4) of resistive material selected from the group consisting of polycrystalline silicon and a refractory silicide is disposed above said substrate, and a refractory metal (5,6) in a conductive pattern is disposed on the surface of said resistive material (4) for conducting drive current to predefined areas in said resistive material.

5. The device defined in claim 4, **characterized** in that said refractory silicide (4) is selected from the group consisting of tantalum silicide, titanium silicide, tungsten silicide and molybdenum silicide, and said refractory metal (5,6) is selected from the group consisting of tantalum, titanium, tungsten and molybdenum.

6. The device defined in claims 4 or 5, **characterized** by multi-level metal interconnects (10,11) extending between said device and a MOS driver circuit and a refractory metal conductor connected between said driver circuit and the refractory metal of said electronic device, whereby compatibility of thermal expansion coefficients of said refractory metals and refractory metal silicides is achieved.

7. A thermal ink jet printhead structure according to one of claims 4,5 or 6, **characterized** in that said resistive layer (4) is protected on selected areas of both sides by silicon nitride (3,7).

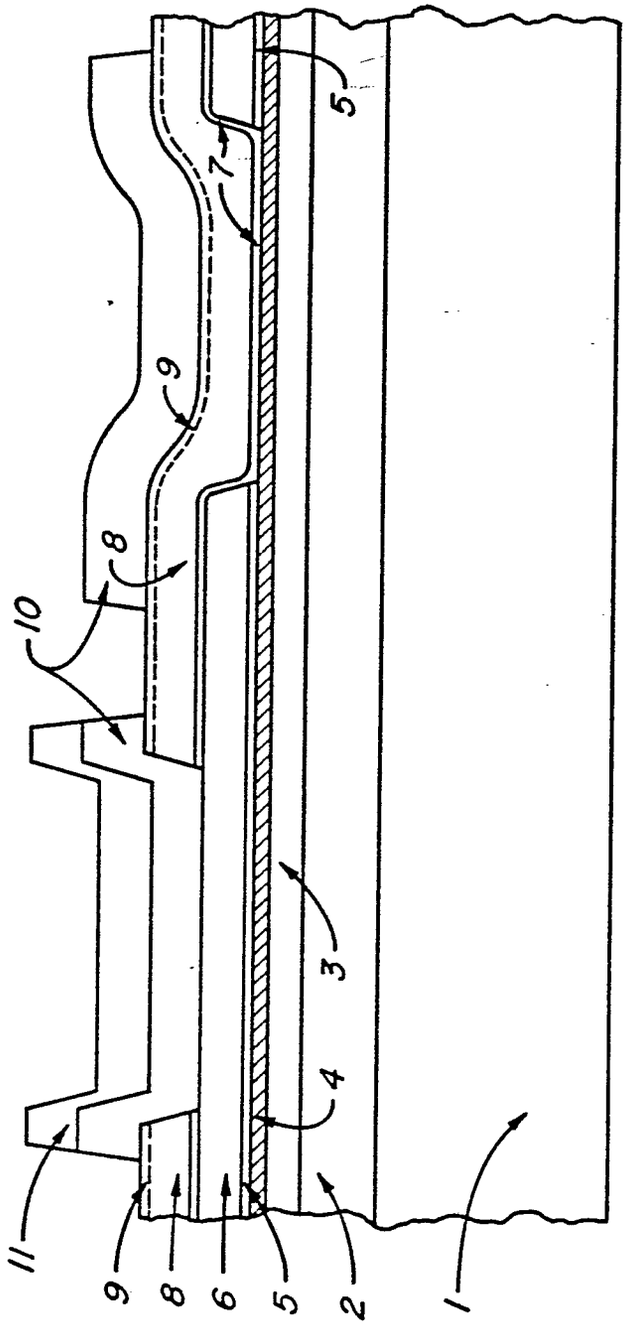

Fig 1

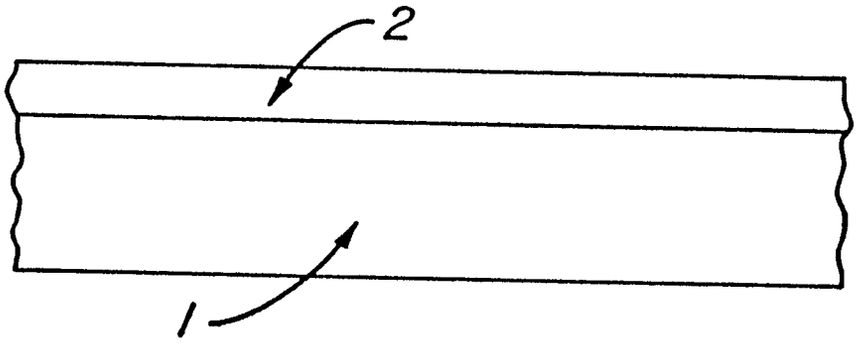

Fig 2A

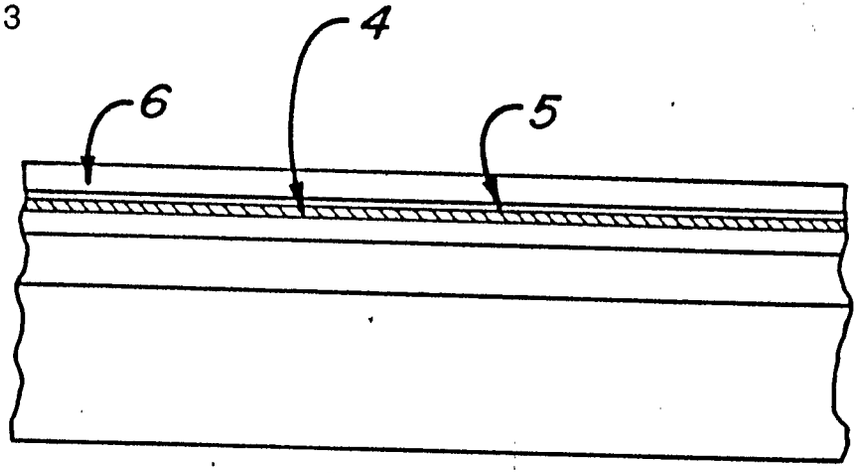

Fig 2C

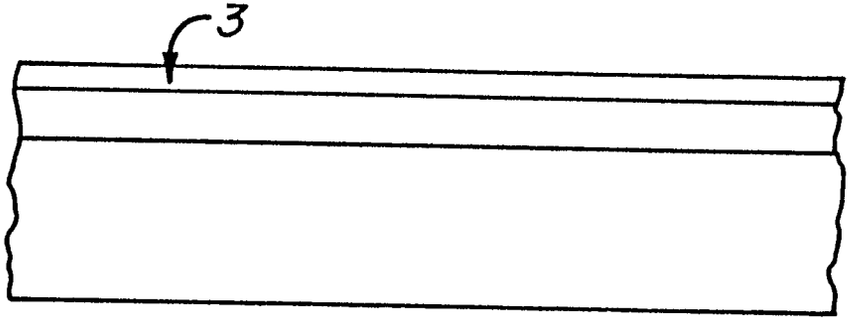

Fig 2B

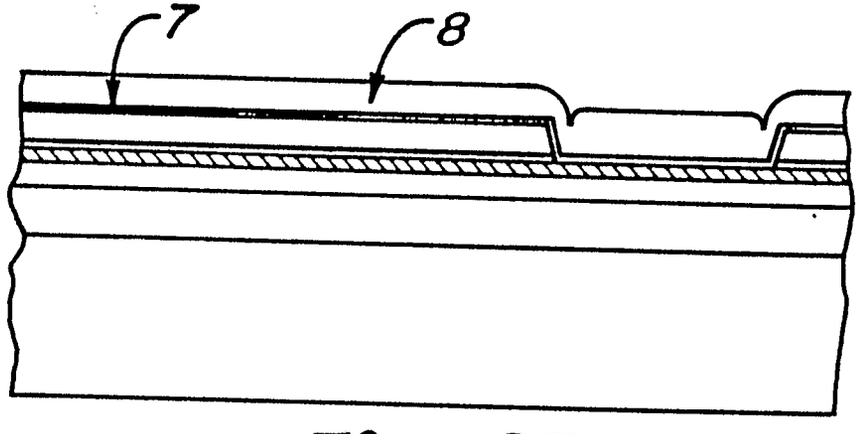

Fig 2D

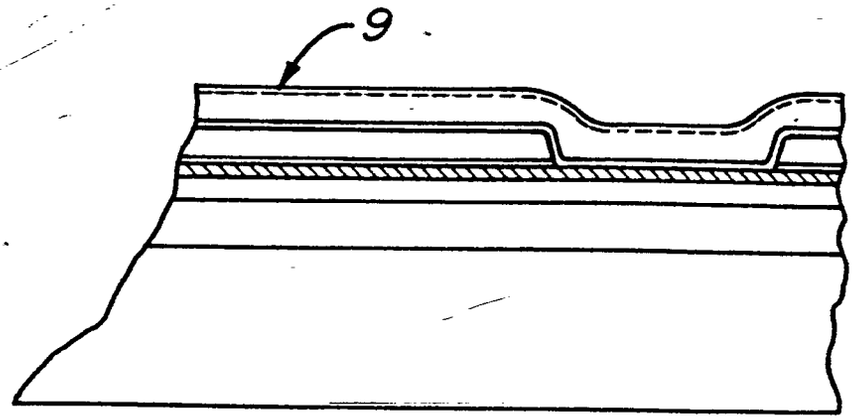

Fig 2E

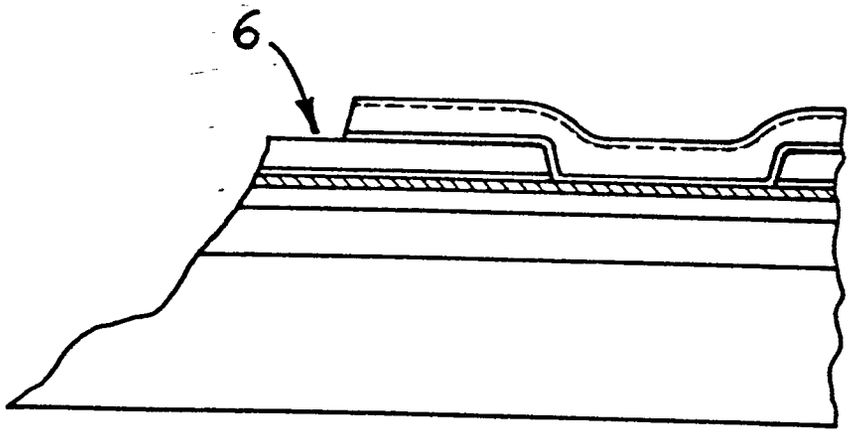

Fig 2F

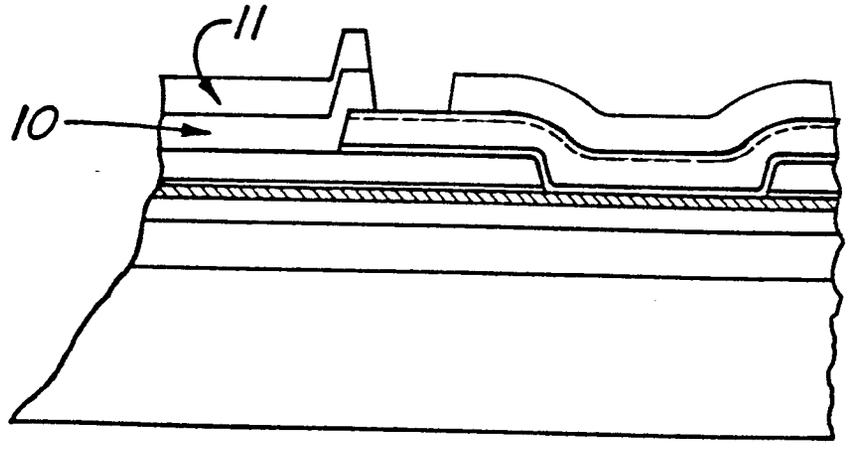

Fig 2G