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71 Applicant: **PITNEY BOWES INC.**
One Elmcroft
Stamford Connecticut 06926-0790(US)

72 Inventor: **Check, Frank T, Jr.**
999 Camillia Way
San Jose, Ca. 95117(US)

74 Representative: **Lehn, Werner, Dipl.-Ing. et al,**
Hoffmann, Eitle & Partner Patentanwälte Arabellastrasse
4
D-8000 München 81(DE)

54 **Microprocessor systems for electronic postage arrangements.**

57 A microprocessor system suitable for an electronic postage arrangement includes a microprocessor (10) and register means (20, 21) for storing accounting data. Sensors (50, 51, 52) are provided for detecting operating conditions in the system and the microprocessor (10) has a software routine stored in permanent memory (11) for periodic checking of the sensors. If the sensor outputs do not correspond with a unique code stored in permanent memory (11), an error condition is indicated.

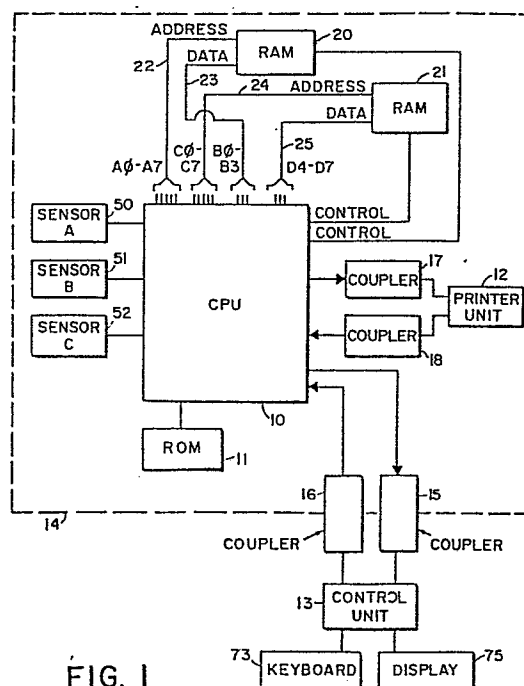


FIG. 1

MICROPROCESSOR SYSTEMS FOR ELECTRONIC POSTAGE ARRANGEMENTS

This invention relates to microprocessor systems and is applicable to electronic postage arrangements having electronic accounting units.

- 5 An electronic postage meter having an accounting unit with a microprocessor, and nonvolatile memory for storing accounting data, is disclosed, for example, in US Patent Application Serial No.089,413 (US Patent No. 4,301,507). In this system the accounting data
10 is stored in the random access memory and retrieved from the random access memory by way of common address and data lines of the microcomputer system. While in most instances it can be ensured that the accounting data stored in the memory will be correct, there
15 are certain conditions that can occur that can result in non-detectable errors in the data..

In order to overcome such problems, it has been proposed to employ redundant memories (EP-A-19515).

- 20 The microprocessor program for the postal meter thus includes a subroutine for comparing the data stored in the redundant memories, to provide an error indication if the stored data in the two memories is different. While this technique increases the
25 reliability of the stored data, there are certain conditions in which even this type of a redundant system will not enable the determination of an error. Furthermore, the known system tests during printing for various indications of malfunction of the print
30 value setting and printing mechanisms. Other types of malfunction are also detected. Upon detection of a malfunction, an appropriate failure code is written into memory and the meter is disabled. It

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must, of course, be emphasized that, in a postage meter, it is essential that the highest degree of reliability of the accounting data be obtained.

5 An object of the present invention is to provide a microprocessor system for an electronic postage meter wherein the possibility of error conditions that are not detectable is reduced.

10 According to one aspect of the invention, there is provided a microprocessor system for an electronic postage arrangement comprising: a microprocessor; register means coupled to said microprocessor for storing postage accounting data; a plurality of
15 sensors for detecting operation conditions in said postage meter; and said microprocessor having a software routine stored in a permanent memory to check said sensors periodically during operation; characterised by means responsive to the noncor-
20 respondence of the outputs of said sensors and a unique code stored in said microprocessor permanent memory, upon a comparison performed in accordance with said software routine, for indicating an error condition.

25

According to another aspect of the invention, there is provided a microprocessor system for an electronic postage meter and characterised by: a microprocessor with a plurality of address lines and a plurality
30 of data lines, and control line means, and random access memory means connected to said address and data lines and control line means to enable transfer of data between said random access memory means and microprocessor; a printer connected to be con-

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- trolled by said microprocessor; and feedback means for signalling the setting of the printer means to the microprocessor, wherein said random access memory comprises first and second random access
5 memories; and means independently responsive to feedback from said feedback means to update the accounting data in each of said first and second random access memories.
- 10 According to a further aspect of the invention, there is provided a microprocessor system for an electronic postage meter characterised by: a printing means; first and second microprocessors; first and second accounting memories connected to be separately
15 controlled by said first and second microprocessors, said first and second microprocessors having program routines for separately updating their respective accounting memories to account for the printing of postage by said printing means; and means for
20 comparing the accounting results in said first and second accounting memories for disabling said postage meter in the absence of a coincidence of data in said first and second accounting memories.
- 25 According to yet another aspect of the invention, there is provided a microprocessor system characterised by an address bus having a plurality of address lines; a data bus having a plurality of data lines; a control bus having a plurality of control lines; a micorprocessor connected to each of the
30 address lines of data lines of said

address and data bus, and coupled to said control bus;
and first and second random access memories each connected to different lines of said address bus and different lines of said data bus, whereby said random access memories may be separately addressed.

In order that the invention will be more clearly understood, it will now be disclosed in greater detail by way of example with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of one embodiment of a microprocessor system for an electronic postage meter in accordance with the invention;

Figure 2 is a time diagram illustrating the sequence of addressing the redundant memories in accordance with another embodiment of the invention;

Figure 3 is a time diagram illustrating another sequence for addressing the redundant memories in accordance with an embodiment of the invention;

Figure 4 is a block diagram of a portion of a modification of the system of Figure 1;

Figure 5 is a block diagram of a further modification of a portion of the system of Figure 1; and

Figure 6 is a block diagram of a further embodiment of the invention.

Referring now to the drawings, and more in particular to Figure 1, therein is illustrated a microprocessor system forming an electronic accounting system, such as may be

employed in an electronic postage meter. The system incorporates a central processing unit 10, such as a microprocessor, and a read only memory 11 storing programs for operation of the system. The central processing unit 10 is coupled to one or more peripherals, such as, for example, the printing unit 12 and control unit 13 of an electronic postage meter such as disclosed in copending U.S. Patent Application Serial No. 089,413 (Patent No. 4,301,507). In the system of Figure 1 a secure housing 14 surrounds various components of the system, such as the central processing unit 10 and printing unit 12. As a consequence, it is necessary to provide ports between the central processing unit and external control unit 13, in order to enable two-way communication between these units. Preferably, the ports are in the form of a pair of one-way transmission paths with opto couplers 15 and 16 at the secure housing, in order to inhibit the application of any electric potentials to the accounting unit without showing evidence of attempts to damage the unit. The opto couplers preferably provide for two-way serial intercommunication between the units on a bit-by-bit basis, in order to minimize the number of ports necessary in the housing.

In addition, it is desirable, as discussed in U.S. Application Serial No. 089,413 (Patent No. 4,301,507) to enable intercommunication between the printing unit and central processing unit 10 by way of a similar pair of opto coupling devices 17 and 18, these opto couplers preferably enabling serial two-way transmission on a bit-by-bit basis.

The printing unit, as well as the control unit may, if desired, have separate microprocessors incorporated therein, enabling the use of a plurality of dedicated

microprocessor systems. This not only enhances the security of the system, but also increases its reliability by restricting the required tasks of each microprocessor to a specific portion of the overall operation of the system. For example, the possibility of conflicting program requirement is thereby greatly reduced.

As illustrated in Figure 1, a pair of random access memories 20, 21 is also provided within the secure housing. The random access memories 20 and 21 are preferably non-volatile memories of conventional nature, so that accounting data may be stored therein without loss even though external power to the system may be lost. For example only, the random access memories may be of the type employing battery back-up, Earom or EEPROM.

The random access memory 20 is connected to the central processing unit 10 by way of a plurality of address lines 22 and a plurality of data lines 23. The random access memory is coupled to the central processing unit 10 by way of another plurality of address lines 24, and another plurality of data lines 25. It is necessary that both the address lines and the data lines coupled to the random access memories be different. For example, address lines A0 - A7 are of a conventional microprocessor system and may be coupled to the random access memory 20, while address lines C0 - C7 are coupled to the random access memory 21. Similarly, conventional data lines B0 - B3 may be coupled to the random access memory 20, with data lines D4 - D7 being coupled to the random access memory 21.

In an accounting system that requires both security and reliability, it is desirable to provide redundancy. A certain degree of redundancy may be obtained if the ran-

dom access memories are connected to the central processing unit by separate data lines, although employing the same address lines. In such a system, the same data may be stored or retrieved from the two random access memories by way of their respective separate data lines, either simultaneously or at different times under control of the respective chip enable signals. While in many instances such an arrangement will enable the detection of errors, upon comparison of data in the two memories, there are in fact possibilities of error that cannot be detected. For example, if two of the address lines are inadvertently shorted together, either in the microprocessor itself or externally thereof, the same erroneous data will be stored in the two random access memories, so that comparison of the data stored in the two memories will not reveal an error condition.

This problem is overcome by employing an entirely different set of address lines of the address bus for addressing the two random access memories. Preferably, of course, the number of address lines, and the number of data lines, connected to each of the random access memories is the same. If, now, two address lines of the system are shorted together, for example, there is little likelihood that the resultant data stored in the two memories will be the same, so that the reliability of the system, in detection of errors, is greatly increased.

While the two random access memories may be simultaneously addressed, employing their separate address lines, for the storage or recovery of the same information, this may also result in errors that could not be detectable or correctable. For example, it is possible that a transient on the bus lines could interfere, in the same manner, with the simultaneously transmitted data. According-

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ly, as illustrated in Figure 2, the two memories are addressed, with respect to the same data, in a sequential manner. For example, all of the sequential bytes of a message may be first applied to, or received from, the first memory, i.e. memory 1. Following the transfer of this message, with respect to the first memory, the same message is then transmitted with respect to the second memory. It will, of course, be apparent that the term "byte" herein refers to data of a length equal to the number of data lines connected to each memory.

In order to reduce the time necessary for updating or reading the memory, each memory may be updated or read simultaneously but with different data being transmitted to or from each memory at any instant, as illustrated in Figure 3.

Figures 2 and 3 hence illustrate two techniques for minimizing the occurrence of undetectable errors resulting from the occurrence, for example, of transient pulses. It is apparent that it would be unlikely for the same interference to occur with sequentially transmitted data.

In a still further embodiment of the invention, the data may be stored in the two memories in a different form. For example, the data stored in one or both of the memories may be coded, in order further to minimize the occurrence of errors undetectable by comparison of the data stored in the two memories. For example, as illustrated in Figure 4, a coder/decoder 30 may be employed to code and decode the data stored in the random access memory 20, applied to and received from the data bus 23. A coder/decoder 31 may optionally be provided for coding and decoding data in the random access memory 21. If such an additional coder/decoder is employed, it is preferable

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that it have a different coding than that of the coder/
decoder 30.

It will, of course, be understood that the programs of
5 the microprocessor have appropriate subroutines to de-
termine, if a comparison between the data shows an in-
consistency, which memory bears the greater likelihood
of correctness. In addition, further routines may be
provided in the event of an inability of the system to
10 determine which of the data entries are error free, to
provide an error indication that inhibits further opera-
tion of the system.

In the embodiment of the invention illustrated in Figures
15 2 and 3, the two memories are addressed under the control
of a fixed program responsive, for example, to a deter-
mined condition in the system. As a consequence, a de-
termined relationship necessarily exists between the ad-
dressing times for the two memories. As a further modi-
20 fication, when separate memory units are provided, each
memory unit may be made independently responsive to de-
termined conditions. For example, when the accounting
system is interconnected as illustrated in Figure 1 to
form a postage meter, the two memories may be indepen-
25 dently responsive to each feedback of a printer setting,
in order to update the separate memories, with an over-
riding subroutine being provided for cross-checking,
i.e., comparing the data stored in the two memories.
The independent control may be, for example, in the form
30 of a memory controller. By thus making the two memory
units operable more independently from one another, the
chances of a greater error-free operation are substan-
tially enhanced.

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In order to ensure proper operation, and thereby to maintain the integrity of the accounting information stored therein, electronic postage meters are provided with a plurality of sensors, such as the sensors 50, 51 and 52 illustrated coupled to the central processing unit 10 in Figure 1. These sensors may be employed for checking a number of conditions within the meter, such as the position of a shutter bar blocking operation of the meter, the positions of various interposers controlling operation of the postage meter, and various other condition sensors such as temperature and humidity. In non-electronic postage meters of the type employing microprocessors for control, such as disclosed in U.S. Patent 3,978,457, certain of these sensors are interrogated by a software routine upon the initial application of power to the meter. The positions of the various shutter bars and interposers, for example, are also determined by software routines initiated by various externally originating conditions, such as, for example, manually controlled operations for initiating the printing of postage. The error checking routines for checking such sensors, as well as for checking additional conditions such as the correctness of data stored in the memories, are hence invoked only when specifically requested in response to external stimuli. Thus, even though a condition may have occurred, between operations of the postage meter, that would eventually cause it to cease operation (i.e. upon the next call for printing of postage), the meter may still deceptively appear externally to be operable.

In accordance with a further feature of the invention, a program for the microprocessor effects the checking of the registers of the random access memory, as well as the various sensors, which may be optical switches, and

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all other critical data indicators at regular times during the course of operation of the postage meter, rather than simply checking these parameters at startup of the meter and uncalled for by external stimuli. By thus
5 providing periodic checks, the possibility of error-free operation is even more greatly enhanced. In other words, the main routine of the postage meter, to which it always returns following the completion of, for example, a postage printing operation, includes software subroutines
10 that periodically check critical parameters, such as the proper positioning of mechanical elements in the meter and the correct comparison of data in memories, as well as the correctness of the data in accordance with control sum data. This technique enables the additional advantageous
15 periodic checking of further sensors mounted, for example, to detect mechanical violation of the security of the housing.

For this purpose, as illustrated in Figure 5, the sensors
20 50, 51 and 52 may be connected to set a plurality of stages of a shift register 55. It will, of course, be understood that the number of such sensors may be greater than the three illustrated. The shift register 55 is coupled to the address and read out by the central processing unit 10 at determined times in the main program.
25 A coded bit pattern is provided in the read only memory 11, corresponding to the correct error-free conditions of the sensors. At the times during the program when the sensors are to be tested, the shift register, under
30 control of the central processing unit, shifts out the existing bit pattern for comparison with the stored bit pattern in the read only memory 11. Thus, the status of the various sensors in the meter may be continually determined, so that the meter may be disabled as soon as a
35 condition exists that threatens the integrity of the meter.

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The shift register may be, of course, shifted under the control of the microprocessor, by the conventional clock source of the system. Alternatively, the shift register may be preprogrammed, in accordance with a determined
5 unique pattern, so that the output of the shift register may be compared with a predetermined "good" condition. The information available from an eight or sixteen bit pattern code, in accordance with this embodiment of the
10 sophistication for the determination of any appropriate error checking for diagnostic purposes, using signature analysis techniques. This form of error checking may be imposed upon various system constraints for both diagnostic and possible error correction on an automatic
15 basis.

In the system illustrated in Figure 1, as discussed above, the printing unit 12 and control unit 13 may include dedicated microprocessors for controlling the specific
20 functions of these units, thereby enabling the use of a dedicated system for the accounting unit including the central processing unit 10, read only memory 11 and random access memories 20 and 21. In further embodiments of the invention, the printing unit 12 may further incorporate a random access memory 60, and/or the control
25 unit 13 may include a nonvolatile random access memory 61.

In a further embodiment of the invention, as illustrated
30 in Figure 6, the nonvolatile random access memories 20, 21 of the accounting system are intercoupled with separate microprocessors 60 and 61, each of the microprocessors having a separate read only memory 62, 63 respectively, for storing the operating programs for the respective
35 microprocessor. It will, of course, be apparent

in the arrangement of Figure 6, as well as in the arrangement of Figure 1, that the read only memory, as well as other components of the system, may be incorporated in the same integrated circuit as the microprocessor.

5 Since the two microprocessors are separately controlled, and have separate address and data lines 64, 65 respectively, the two random access memories are thereby entirely independently controlled. The two microprocessors separately communicate with the control unit 13 and
10 printer 82 by way of separate selector switches 70 and 71 addressed by the respective microprocessors 60 and 61. As a consequence, each of the microprocessors may receive signals from the printer and control unit, and each of them may also transmit messages. In addition,
15 data processed in the two microprocessors may be compared by means of a data latch 72 controllable by either of the microprocessors.

In the arrangement of Figure 6, input data received, for
20 example, from the keyboard 73 or other peripheral device coupled to the control unit 13, is applied by way of the opto couplers 15 and 16 and the selecting switches 70 and 71 to the two microprocessor systems. Alternatively, of course, the data may be input to the two microproces-
25 sors in response to an interrupt signal. The two microprocessors, in response to the input information, perform the necessary accounting procedures independently of one another, with respect to the data stored in the respective random access memories. The programs of the two
30 microprocessors enable interchange of accounting data for comparison, for example, on a contention basis, by way of the data latch 72. The programs of the two microprocessors may enable, for example, only one of the microprocessors to control the display 75 coupled to the
35 control unit 13, and/or to control the printer 82. Alternatively, of course, redundant control may be employed,

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whereby the control of a printer function, or the control of a display, may require the common occurrence of the output function from the two microprocessors. This may be effected, for example, in the manner disclosed in
5 U.S. Patent Application Serial No. 089,413 filed October 30, 1979, and assigned to the assignee of the present application, by controlling a pair of series transistors separately by the two microprocessors, whereby the common
10 output of the series transistors effects the desired control. It is, of course, apparent that other techniques may be employed for this purpose.

The arrangement of Figure 6 thereby increases the redundancy of the system, so that even a failure in a micro-
15 processor will enable the determination, with great reliability, the occurrence of an error condition that may require the disabling of the meter.

In the system of Figure 6, the printer unit is more completely shown as comprised of a microprocessor 80 coupled
20 to the opto couplers 17 and 18, and controlling a print setter 81. The print setter 81 sets the printwheels in a printer 82, the setting of the printwheels being fed back to the microprocessor 80 by way of a feedback path
25 83. This feedback enables the printer unit to determine if an error has occurred in the setting of the printwheels, and thereby to disable the meter in the event of an erroneous setting. The feedback setting may be applied from the microprocessor 80 to the opto couplers 17
30 and 18, thereby enabling the two microprocessors in the accounting system to be separately responsive to the feedback signals, for accounting for postage to be printed.

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It is, of course, apparent that suitable control lines are provided connected to the microprocessor and random access memories in the conventional manner, for controlling the systems.

5

The function of disabling the meter, in the illustrated embodiments, may be effected by inhibiting, under program control, operation of the mechanical elements of the meter. Alternatively, the existence of an error requiring disabling of the meter may direct the routines of the microprocessor to perform an endless loop. Errors that do not require disabling of the meter may be displayed, under control of the microprocessor, by means of the display 73 coupled to the external control unit.

15

Thus, in accordance with one aspect of the invention, redundant nonvolatile memories are provided in the accounting unit of an electronic postage meter, the accounting unit having a microprocessor controlled to store accounting data redundantly in the two memories. In order to minimize the possibility of nondetectable errors, the two redundant memories are interconnected with the microprocessor, i.e. the microcomputer bus, by way of entirely separate groups of data and address lines. As a result of the complete separation of the addressing and data, various error conditions, such as the shorting of a pair of address lines, will not result in the erroneous addressing of both of the memories. Accordingly, under such conditions, the shorting of a pair of address lines will not result in the storage of the same data in both of the memories, so that a comparison of stored data will result in the detection of the error condition.

In accordance with a further embodiment of the invention, corresponding data is applied redundantly to the redundant memories at different times. This may be effected

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by separately applying the data sequentially to the two memories. Alternatively, data may be simultaneously applied to or retrieved from the two memories, with the data transferred at any instant with respect to the two
5 memories corresponding to different information. As a result, instantaneously occurring transients on the transmission lines will not be likely to affect the corresponding data stored in the two memories in the same fashion. This system thereby minimizes the possibility
10 of nondetectable and/or noncorrectable errors resulting from transients.

In accordance with a still further embodiment of the invention, the redundancy of the accounting system may be
15 increased by also employing redundant microprocessors for controlling the two memories.

In order to still further minimize the possibility of printing postage without accounting, the program of the
20 microprocessor may be directed to the periodic testing of various critical parameters within the microprocessor, as part of a main routine, the testing routine only being interrupted, if necessary, during a conventional postage printing operation such as the printing of postage and
25 accounting therefor. As a consequence, the routine of the postage meter enables the continuous testing of such parameters, so that the postage meter may be disabled as soon as a condition exists that threatens the integrity of the accounting data. The error checking on a periodic
30 basis may test not only the physical parameters, such as positions of various mechanical elements, but also may effect the comparison of the data stored in the two memories, as well as performing control sum checks to determine if the data stored in each memory is in accordance
35 with determined relationships.

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Other types of memory can, of course, be employed instead of RAM such as serial memory.

5 While the invention has been disclosed and described with reference to a limited number of embodiments, it will be apparent that variations and modifications may be made therein, and it is intended in the following claims to cover each such variation and modification as falls within the true scope of the invention.

CLAIMS:

1. A microprocessor system for an electronic postage arrangement comprising: a microprocessor (10); register means (20, 21) coupled to said microprocessor for storing postage accounting data; a
5 plurality of sensors (50, 51, 52) for detecting operation conditions in said postage meter; and said microprocessor having a software routine stored in a permanent memory (11) to check said sensors periodically during operation; characterised by
10 means responsive to the noncorrespondence of the outputs of said sensors and a unique code stored in said microprocessor permanent memory, upon a comparison performed in accordance with said software routine, for indicating an error condition.
- 15 2. A system according to claim 1 characterised in that said sensors are arranged to sense physical conditions of said meter.
3. A system according to claim 1 characterised in that one of said sensors is arranged to sense
20 the position of a shutter bar which blocks the operation of said meter.
4. A system according to claim 1 characterised in that one of said sensors is connected to sense temperature.
- 25 5. A system according to claim 1 characterised in that one of said sensors is connected to sense humidity.

6. A system according to claim 1 characterised in that said postage meter has a memory, and said software routine periodically checks the correctness of data stored in said memory.
- 5 7. A system according to claim 1 characterised by a pair of memories wherein said software routine also periodically compares information stored in said memories.
8. A microprocessor system for an electronic
10 postage arrangement and comprising: a microprocessor (10, 80) with a plurality of address lines, a plurality of data lines, and control line means, the microprocessor being arranged to selectively control said address and data lines; random access memory
15 means (20, 21) connected to said address and data lines and control line means to enable transfer of data between said random access memory means and said microprocessor; a printer means (12; 82) connected to be controlled by said microprocessor;
20 and feedback means (18; 83) for signalling the setting of the printer means to the microprocessor, wherein said random access memory comprises first (20) and second (21) random access memories; and means independently responsive to feedback from said feedback
25 means to update the accounting data in each of said first and second random access memories.
9. A microprocessor system for an electronic postage arrangement comprising: a printing means (80, 81, 82); first and second microprocessors (60,
30 61); first and second accounting memories (20,21) connected to be separately controlled by said first

and second microprocessors, said first and second microprocessors having program routines for separately updating their respective accounting memories to account for the printing of postage by said printing means; and means for comparing the accounting results in said first and second accounting memories for disabling said postage meter in the absence of a coincidence of data in said first and second accounting memories.

10 10. A system according to claim 9 wherein said routines of said first and second microprocessors are arranged to store data in their respective accounting memories with different coding.

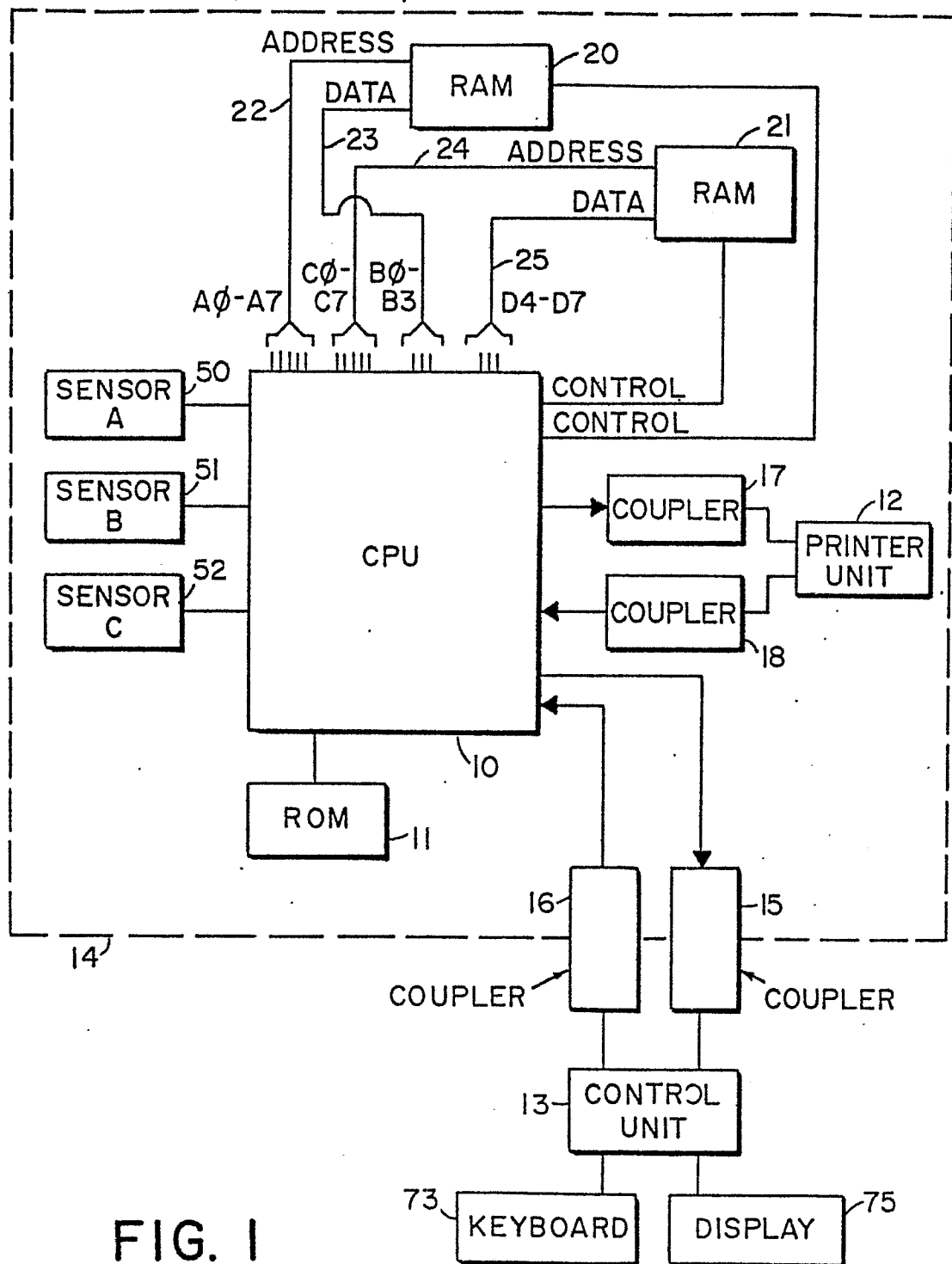
11. A system according to claim 9 or 10 wherein
15 said printing means comprises a further microprocessor (80) having a postage printing program for controlling printing of said postage meter.

12. A microprocessor system characterised by an address bus (22, 24) having a plurality of address
20 lines; a data bus (23, 25) having a plurality of data lines; a control bus having a plurality of control lines; a microprocessor (10) connected to each of the address lines of data lines of said address and data bus, and coupled to said control
25 bus; and first and second random access memories (20, 21) each connected to different lines of said address bus and different lines of said data bus, whereby said random access memories may be separately addressed.

30 13. A system according to claim 12 characterised

by a program memory (11) for controlling the operation of said microprocessor (10) and having a program for addressing said first and second random access memories (20, 21) to store the same data therein.

- 5 14. A system according to claim 13 characterised in that said program addresses correspond to storage locations of said first and second memories (20, 21), corresponding data being stored therein or read therefrom at different times.
- 10 15. A system according to claim 14 characterised in that said program simultaneously stores different data in said first and second memories (20, 21) at noncorresponding address locations, whereby instantaneously occurring errors affect the data stored
15 in said first and second memories in different manners.
16. A system according to any one of claims 12 to 15 characterised in that said random access memories (20, 21) are nonvolatile.
17. A system according to any one of claims 12
20 to 16 characterised by means responsive to differences in data stored in first and second memories (20, 21) for disabling further operation of said microprocessor (10).
18. An accounting system characterised by a micro-
25 processor system according to any one of the preceding claims.
19. A postage meter characterised by an accounting system according to claim 18.



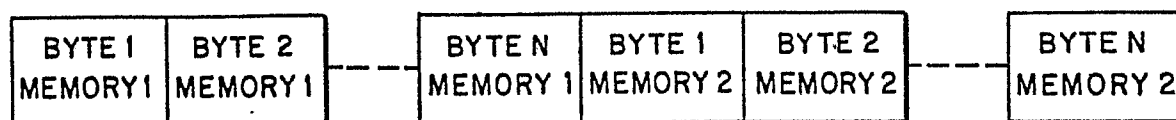


FIG. 2

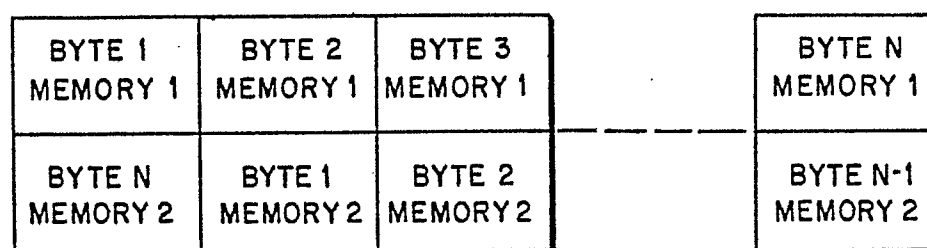


FIG. 3

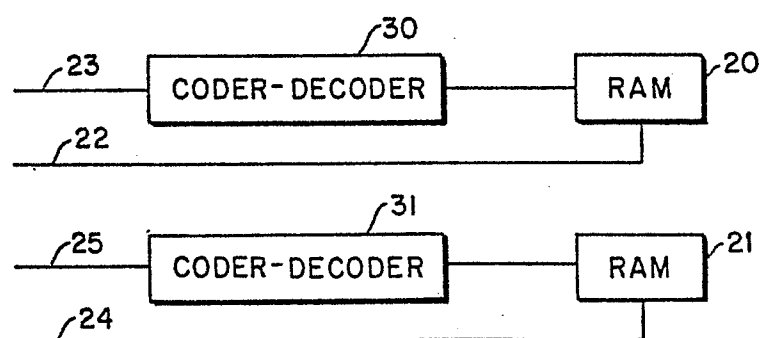


FIG. 4

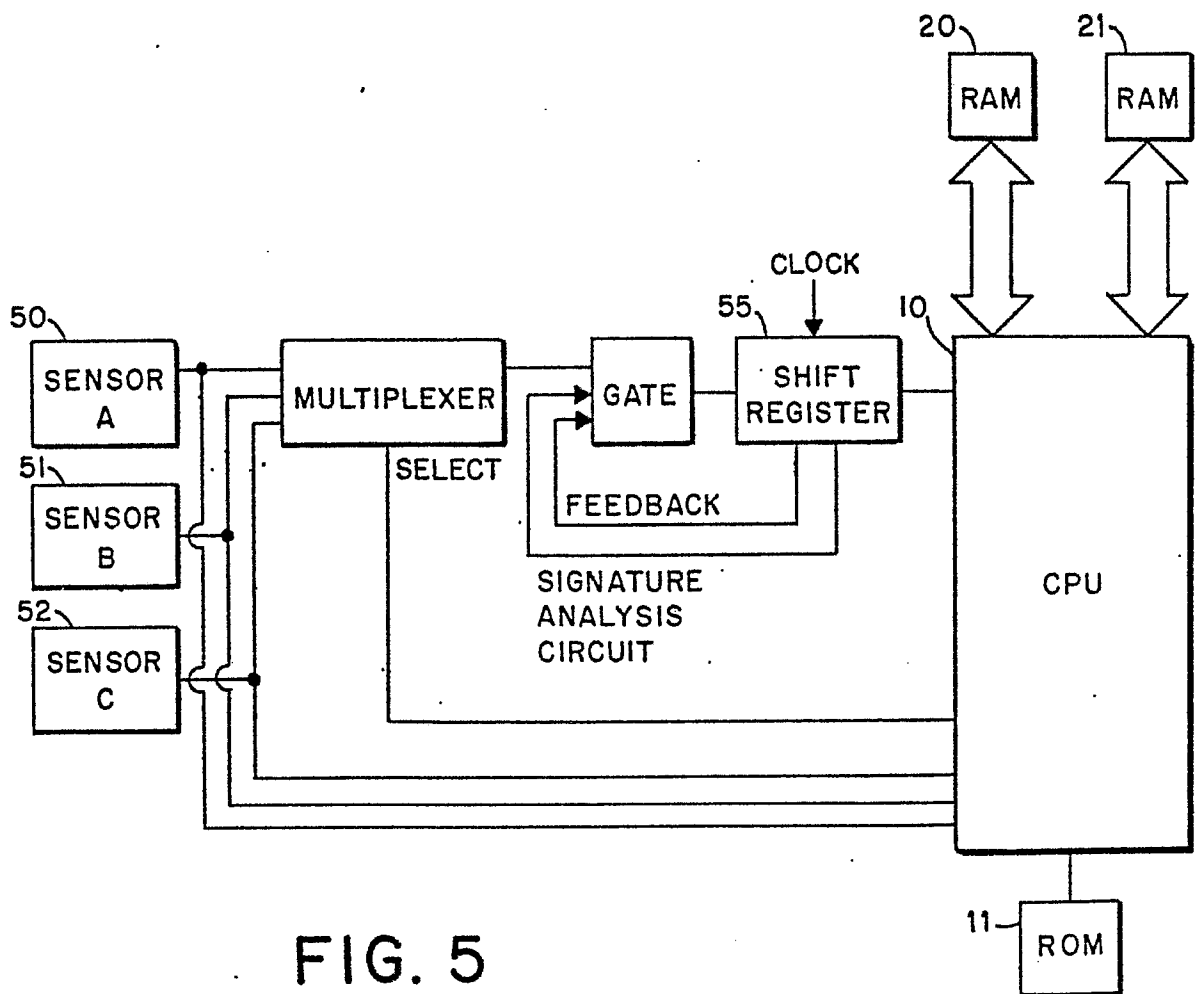


FIG. 5

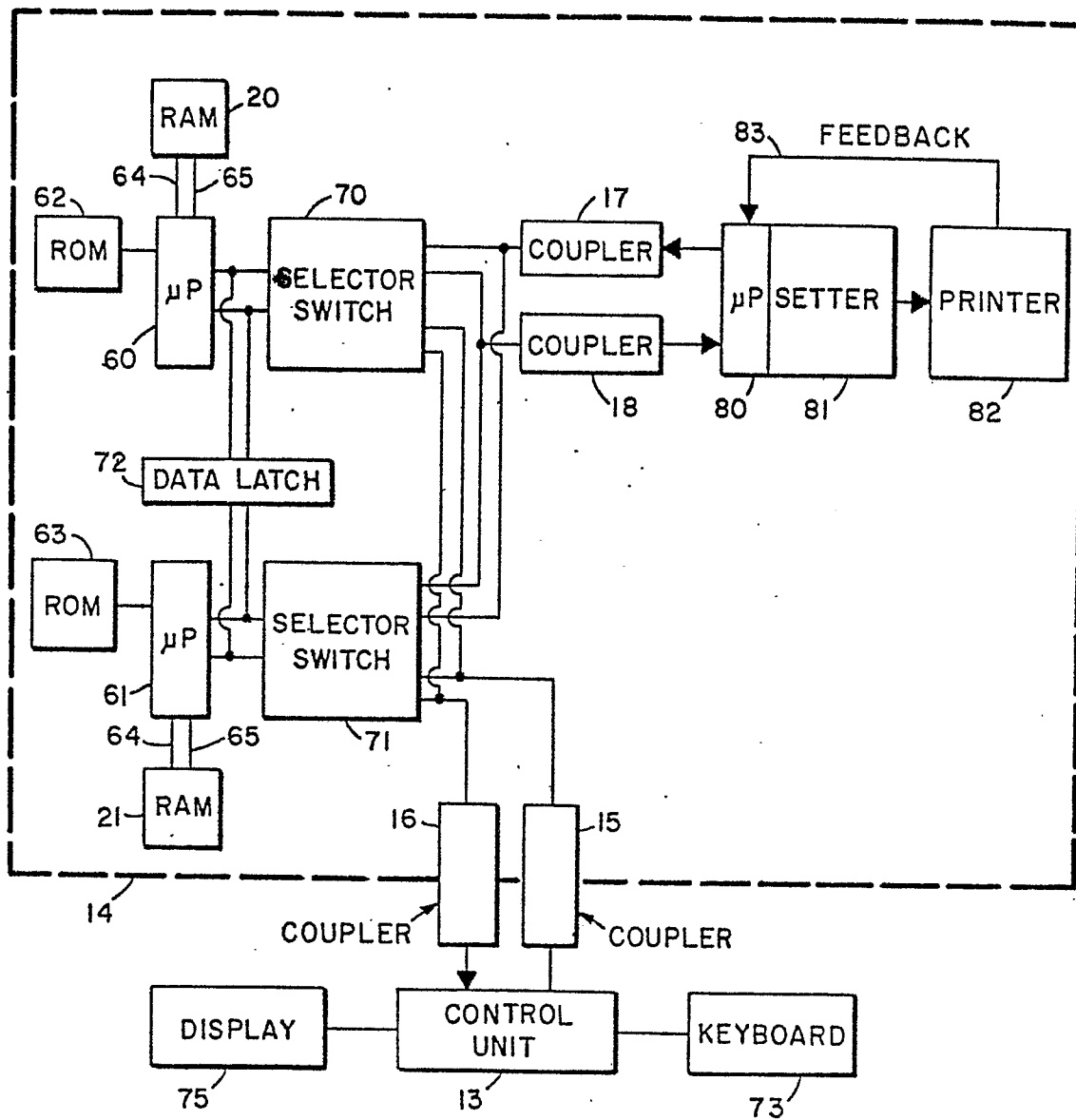


FIG. 6