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(54) **Microprocessor systems for electronic postage arrangements**

Mikroprozessorsysteme für elektronische Frankiereinrichtungen

Systèmes à microprocesseur pour dispositif d'affranchissement électronique

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## Description

**[0001]** This invention relates to electronic postage meter systems. EP-A-0 019 515 discloses an electronic postage meter system comprising: an address bus having a plurality of address lines; a data bus having a plurality of data lines; a control bus having a plurality of control lines; a microprocessor connected to each of the address lines and data lines of said address and data bus, and coupled to said control bus; and first and second random access memory units, the microprocessor being directly connected to each of the address and data lines. (See also GB-A-2 079 223).

**[0002]** An electronic postage meter having an accounting unit with a microprocessor, and non-volatile memory for storing accounting data, is disclosed, for example, in US Patent Application Serial No. 089,413 (US Patent No. 4,301,507). In this system the accounting data is stored in the random access memory and retrieved from the random access memory by way of common address and data lines of the microcomputer system. While in most instances it can be ensured that the accounting data stored in the memory will be correct, there are certain conditions that can occur that can result in non-detectable errors in the data.

**[0003]** In order to overcome such problems, it has been proposed to employ redundant memories (EP-A-19 515). The microprocessor program for the postal meter thus includes a subroutine for comparing the data stored in the redundant memories, to provide an error indication if the stored data in the two memories is different. While this technique increases the reliability of the stored data, there are certain conditions in which even this type of a redundant system will not enable the determination of an error. Furthermore, the known system tests during printing for various indications of malfunction of the print value setting and printing mechanisms. Other types of malfunction are also detected. Upon detection of a malfunction, an appropriate failure code is written into memory and the meter is disabled. It must, of course, be emphasized that, in a postage meter, it is essential that the highest degree of reliability of the accounting data be obtained.

**[0004]** An object of the present invention is to provide an electronic postage meter system wherein the possibility of error conditions that are not detectable is reduced.

**[0005]** According to one aspect of the invention, there is provided an electronic postage meter system according to claim 1.

**[0006]** IBM Technical Disclosure Bulletin vol.10, no. 10, March 1968, pages 1484/1485 discloses a high-availability memory system having redundant storage units each using different address and data lines. These, however, are only indirectly connected to the CPU through a selection unit.

**[0007]** DE-A-30 24 370 provides redundant memories which, however, are not connected to the same central computer.

**[0008]** According to a further aspect of the invention, there is provided an electronic postage meter system according to claim 7.

**[0009]** In order that the invention will be more clearly understood, it will now be disclosed in greater detail by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of one embodiment of a microprocessor system for an electronic post-age meter in accordance with the invention;
Fig. 2 is a time diagram illustrating the sequence of addressing the redundant memories in accordance with another embodiment of the invention;
Fig. 3 is a time diagram illustrating another sequence for addressing the redundant memories in accordance with an emobodiment of the invention;
Fig. 4 is a block diagram of a portion of a modification of the system of Fig. 1;
Fig. 5 is a block diagram of a further modification of a portion of the system of Fig. 1: and
Fig. 6 is a block diagram of a further embodiment of the invention.

**[0010]** Referring now to the drawings, and more in particular to Fig. 1, therein is illustrated a microprocessor system forming an electronic accounting system, such as may be employed in an electronic postage meter. The system incorporates a central processing unit 10, such as a microprocessor, and a read only memory 11 storing programs for operation of the system. The central processing unit 10 is coupled to one or more peripherals, such as, for example, the printing unit 12 and control unit 13 of an electronic postage meter such as disclosed in copending U.S. Patent Application Serial No. 089,413 (Patent No. 4,301,507). In the system of Figure 1 a secure housing 14 surrounds various components of the system, such as the central processing unit 10 and printing unit 12. As a consequence, it is necessary to provide ports between the central processing unit and external control unit 13, in order to enable two-way communication between these units. Preferably, the ports are in the form of a pair of one-way transmission paths with opto couplers 15 and 16 at the secure housing, in order to inhibit the application of any electric potentials to the accounting unit without showing evidence of attempts to damage the unit. The opto couplers preferably provide for two-way serial intercommunication between the units on a bit-by-bit basis, in order to minimize the number of ports necessary in the housing.

**[0011]** In addition, it is desirable, as discussed in U. S. Application Serial No. 089,413 (Patent No. 4,301,507) to enable intercommunication between the printing unit and central processing unit 10 by way of a similar pair of opto coupling devices 17 and 18, these opto couplers preferably enabling serial two-way transmission on a bit-by-bit basis.

**[0012]** The printing unit, as well as the control unit may, if desired, have separate microprocessors incorporated therein, enabling the use of a plurality of dedicated microprocessor systems. This not only enhances the security of the system, but also increases its reliability by restricting the required tasks of each microprocessor to a specific portion of the overall operation of the system. For example, the possibility of conflicting program requirement is thereby greatly reduced.

**[0013]** As illustrated in Figure 1, a pair of random access memories 20, 21 is also provided within the secure housing. The random access memories 20 and 21 are preferably non-volatile memories of conventional nature, so that accounting data may be stored therein without loss even though external power to the system may be lost. For example only, the random access memories may be of the type employing battery back-up, Earom or EEPROM.

**[0014]** The random access memory 20 is connected to the central processing unit 10 by way of a plurality of address lines 22 and a plurality of data lines 23. The random access memory is coupled to the central processing unit 10 by way of another plurality of address lines 24, and another plurality of data lines 25. It is necessary that both the address lines and the data lines coupled to the random access memories be different. For example, address lines A0 - A7 are of a conventional microprocessor system and may be coupled to the random access memory 20, while address lines C0 - C7 are coupled to the random access memory 21. Similarly, conventional data lines B0 - B3 may be coupled to the random access memory 20, with data lines D4 - D7 being coupled to the random access memory 21.

**[0015]** In an accounting system that requires both security and reliability, it is desirable to provide redundancy. A certain degree of redundancy may be obtained if the random access memories are connected to the central processing unit by separate data lines, although employing the same address lines. In such a system, the same data may be stored or retrieved from the two random access memories by way of their respective separate data lines, either simultaneously or at different times under control of the respective chip enable signals. While in many instances such an arrangement will enable the detection of errors, upon comparison of data in the two memories, there are in fact possibilities of error that cannot be detected. For example, if two of the address lines are inadvertently shorted together, either in the microprocessor itself or externally thereof, the same erroneous data will be stored in the two random access memories, so that comparison of the data stored in the two memories will not reveal an error condition.

**[0016]** This problem is overcome by employing an entirely different set of address lines of the address bus for addressing the two random access memories. Preferably, of course, the number of address lines, and the number of data lines, connected to each of the random access memories is the same. If, now, two address lines of the system are shorted together, for example, there is little likelihood that the resultant data stored in the two memories will be the same, so that the reliability of the system, in detection of errors, is greatly increased.

**[0017]** While the two random access memories may be simultaneously addressed, employing their separate address lines, for the storage or recovery of the same information, this may also result in errors that could not be detectable or correctable. For example, it is possible that a transient on the bus lines could interfere, in the same manner, with the simultaneously transmitted data. Accordingly, as illustrated in Figure 2, the two memories are addressed, with respect to the same data, in a sequential manner. For example, all of the sequential bytes of a message may be first applied to, or received from, the first memory, i.e. memory 1. Following the transfer of this message, with respect to the first memory, the same message is then transmitted with respect to the second memory. It will, of course, be apparent that the term "byte" herein refers to data of a length equal to the number of data lines connected to each memory.

**[0018]** In order to reduce the time necessary for updating or reading the memory, each memory may be updated or read simultaneously but with different data being transmitted to or from each memory at any instant, as illustrated in Figure 3.

**[0019]** Figures 2 and 3 hence illustrate two techniques for minimizing the occurrence of undetectable errors resulting from the occurrence, for example, of transient pulses. It is apparent that it would be unlikely for the same interference to occur with sequentially transmitted data.

**[0020]** In a still further embodiment of the invention, the data may be stored in the two memories in a different form. For example, the data stored in one or both of the memories may be coded, in order further to minimize the occurrence of errors undetectable by comparison of the data stored in the two memories. For example, as illustrated in Figure 4, a coder/decoder 30 may be employed to code and decode the data stored in the random access memory 20, applied to and received from the data bus 23. A coder/decoder 31 may optionally be provided for coding and decoding data in the random access memory 21. If such an additional coder/decoder is employed, it is preferable that it have a different coding than that of the coder/decoder 30.

**[0021]** It will, of course, be understood that the programs of the microprocessor have appropriate subroutines to determine, if a comparison between the data shows an inconsistency, which memory bears the greater likelihood of correctness. In addition, further routines may be provided in the event of an inability of the system to determine which of the data entries are error free, to provide an error indication that inhibits further operation of the system.

**[0022]** In the embodiment of the invention illustrated in Figures 2 and 3, the two memories are addressed under the control of a fixed program responsive, for exam-

ple, to a determined condition in the system. As a consequence, a determined relationship necessarily exists between the addressing times for the two memories. As a further modification, when separate memory units are provided, each memory unit may be made independently responsive to determined conditions. For example, when the accounting system is interconnected as illustrated in Figure 1 to form a postage meter, the two memories may be independently responsive to each feedback of a printer setting, in order to update the separate memories, with an overriding subroutine being provided for cross-checking, i.e., comparing the data stored in the two memories. The independent control may be, for example, in the form of a memory controller. By thus making the two memory units operable more independently from one another, the chances of a greater error-free operation are substantially enhanced.

**[0023]** In order to ensure proper operation, and thereby to maintain the integrity of the accounting information stored therein, electronic postage meters are provided with a plurality of sensors, such as the sensors 50, 51 and 52 illustrated coupled to the central processing unit 10 in Figure 1. These sensors may be employed for checking a number of conditions within the meter, such as the position of a shutter bar blocking operation of the meter, the positions of various interposers controlling operation of the postage meter, and various other condition sensors such as temperature and humidity. In non-electronic postage meters of the type employing microprocessors for control, such as disclosed in U.S. Patent 3,978,457, certain of these sensors are interrogated by a software routine upon the initial application of power to the meter. The positions of the various shutter bars and interposers, for example, are also determined by software routines initiated by various externally originating conditions, such as, for example, manually controlled operations for initiating the printing of post-age. The error checking routines for checking such sensors, as well as for checking additional conditions such as the correctness of data stored in the memories, are hence invoked only when specifically requested in response to external stimuli. Thus, even though a condition may have occurred, between operations of the postage meter, that would eventually cause it to cease operation (i. e. upon the next call for printing of postage), the meter may still deceptively appear externally to be operable.

**[0024]** In accordance with a further feature of the invention, a program for the microprocessor effects the checking of the registers of the random access memory, as well as the various sensors, which may be optical switches, and all other critical data indicators at regular times during the course of operation of the postage meter, rather than simply checking these parameters at startup of the meter and uncalled for by external stimuli. By thus providing periodic checks, the possibility of error-free operation is even more greatly enhanced. In other words, the main routine of the postage meter, to which it always returns following the completion of, for example, a post-age printing operation, includes software subroutines that periodically check critical parameters, such as the proper positioning of mechanical elements in the meter and the correct comparison of data in memories, as well as the correctness of the data in accordance with control sum data. This technique enables the additional advantageous periodic checking of further sensors mounted, for example, to detect mechanical violation of the security of the housing.

**[0025]** For this purpose, as illustrated in Figure 5, the sensors 50, 51 and 52 may be connected to set a plurality of stages of a shift register 55. It will, of course, be understood that the number of such sensors may be greater than the three illustrated. The shift register 55 is coupled to the address and read out by the central processing unit 10 at determined tines in the main program. A coded bit pattern is provided in the read only memory 11, corresponding to the correct error-free conditions of the sensors. At the times during the program when the sensors are to be tested, the shift register, under control of the central processing unit, shifts out the existing bit pattern for comparison with the stored bit pattern in the read only memory 11. Thus, the status of the various sensors in the meter may be continually determined, so that the meter may be disabled as soon as a condition exists that threatens the integrity of the meter.

**[0026]** The shift register may be, of course, shifted under the control of the microprocessor, by the conventional clock source of the system. Alternatively, the shift register may be preprogrammed, in accordance with a determined unique pattern, so that the output of the shift register may be compared with a predetermined "good" condition. The information available from an eight or sixteen bit pattern code, in accordance with this embodiment of the invention, may thus provide a very large degree of sophistication for the determination of any appropriate error checking for diagnostic purposes, using signature analysis techniques. This form of error checking may be imposed upon various system constraints for both diagnostic and possible error correction on an automatic basis.

**[0027]** In the system illustrated in Figure 1, as discussed above, the printing unit 12 and control unit 13 may include dedicated microprocessors for controlling the specific functions of these units, thereby enabling the use of a dedicated system for the accounting unit including the central processing unit 10, read only memory 11 and random access memories 20 and 21. In further embodiments of the invention, the printing unit 12 may further incorporate a random access memory 60, and/or the control unit 13 may include a nonvolatile random access memory 61.

**[0028]** In a further embodiment of the invention, as illustrated in Figure 6, the nonvolatile random access memories 20, 21 of the accounting system are intercoupled with separate microprocessors 60 and 61, each of the microprocessors having a separate read only memory 62, 63 respectively, for storing the operating pro-

grams for the respective microprocessor. It will, of course, be apparent in the arrangement of Figure 6, as well as in the arrangement of Figure 1, that the read only memory, as well as other components of the system, may be incorporated in the same integrated circuit as the microprocessor. Since the two microprocessors are separately controlled, and have separate address and data lines 64, 65 respectively, the two random access memories are thereby entirely independently controlled. The two microprocessors separately communicate with the control unit 13 and printer 82 by way of separate selector switches 70 and 71 addressed by the respective microprocessors 60 and 61. As a consequence, each of the microprocessors may receive signals from the printer and control unit, and each of them may also transmit messages. In addition, data processed in the two microprocessors may be compared by means of a data latch 72 controllable by either of the microprocessors.

**[0029]** In the arrangement of Figure 6, input data received, for example, from the keyboard 73 or other peripheral device coupled to the control unit 13, is applied by way of the opto couplers 15 and 16 and the selecting switches 70 and 71 to the two microprocessor systems. Alternatively, of course, the data may be input to the two microprocessors in response to an interrupt signal. The two microprocessors, in response to the input information, perform the necessary accounting procedures independently of one another, with respect to the data stored in the respective random access memories. The programs of the two microprocessors enable interchange of accounting data for comparison, for example, on a contention basis, by way of the data latch 72. The programs of the two microprocessors may enable, for example, only one of the microprocessors to control the display 75 coupled to the control unit 13, and/or to control the printer 82. Alternatively, of course, redundant control may be employed, whereby the control of a printer function, or the control of a display, may require the common occurrence of the output function from the two microprocessors. This may be effected, for example, in the manner disclosed in U.S. Patent Application Serial No. 089,413 filed October 30, 1979, and assigned to the assignee of the present application, by controlling a pair of series transistors separately by the two microprocessors, whereby the common output of the series transistors effects the desired control. It is, of course, apparent that other techniques may be employed for this purpose.

**[0030]** The arrangement of Figure 6 thereby increases the redundancy of the system, so that even a failure in a microprocessor will enable the determination, with great reliability, the occurrence of an error condition that may require the disabling of the meter.

**[0031]** In the system of Figure 6, the printer unit is more completely shown as comprised of a microprocessor 80 coupled to the opto couplers 17 and 18, and controlling a print setter 81. The print setter 81 sets the printwheels in a printer 82, the setting of the printwheels being fed back to the microprocessor 80 by way of a feedback path 83. This feedback enables the printer unit to determine if an error has occurred in the setting of the printwheels, and thereby to disable the meter in the event of an erroneous setting. The feedback setting may be applied from the microprocessor 80 to the opto couplers 17 and 18, thereby enabling the two microprocessors in the accounting system to be separately responsive to the feedback signals, for accounting for postage to be printed.

**[0032]** It is, of course, apparent that suitable control lines are provided connected to the microprocessor and random access memories in the conventional manner, for controlling the systems.

**[0033]** The function of disabling the meter, in the illustrated embodiments, may be effected by inhibiting, under program control, operation of the mechanical elements of the meter. Alternatively, the existence of an error requiring disabling of the meter may direct the routines of the microprocessor to perform an endless loop. Errors that do not require disabling of the meter may be displayed, under control of the microprocessor, by means of the display 73 coupled to the external control unit.

**[0034]** Thus, in accordance with one aspect of the invention, redundant nonvolatile memories are provided in the accounting unit of an electronic post-age meter, the accounting unit having a microprocessor controlled to store accounting data redundantly in the two memories. In order to minimize the possibility of nondetectable errors, the two redundant memories are interconnected with the microprocessor, i.e. the microcomputer bus, by way of entirely separate groups of data and address lines. As a result of the complete separation of the addressing and data, various error conditions, such as the shorting of a pair of address lines, will not result in the erroneous addressing of both of the memories. Accordingly, under such conditions, the shorting of a pair of address lines will not result in the storage of the same data in both of the memories, so that a comparison of stored data will result in the detection of the error condition.

**[0035]** In accordance with a further embodiment of the invention, corresponding data is applied redundantly to the redundant memories at different times. This may be effected by separately applying the data sequentially to the two memories. Alternatively, data may be simultaneously applied to or retrieved from the two memories, with the data transferred at any instant with respect to the two memories corresponding to different information. As a result, instantaneously occurring transients on the transmission lines will not be likely to affect the corresponding data stored in the two memories in the same fashion. This system thereby minimizes the possibility of nondetectable and/or noncorrectable errors resulting from transients.

**[0036]** In accordance with a still further embodiment of the invention, the redundancy of the accounting system may be increased by also employing redundant mi-

croprocessors for controlling the two memories.

**[0037]** In order to still further minimize the possibility of printing postage without accounting, the program of the microprocessor may be directed to the periodic testing of various critical parameters within the microprocessor, as part of a main routine, the testing routine only being interrupted, if necessary, during a conventional postage printing operation such as the printing of postage and accounting therefor. As a consequence, the routine of the postage meter enables the continuous testing of such parameters, so that the postage meter may be disabled as soon as a condition exists that threatens the integrity of the accounting data. The error checking on a periodic basis may test not only the physical parameters, such as positions of various mechanical elements, but also may effect the comparison of the data stored in the two memories, as well as performing control sum checks to determine if the data stored in each memory is in accordance with determined relationships.

**[0038]** Other types of memory can, of course, be employed instead of RAM such as serial memory.

**[0039]** While the invention has been disclosed and described with reference to a limited number of embodiments, it will be apparent that variations and modifications may be made therein within the scope of the following claims.

## Claims

**1.** An electronic postage meter system comprising:

an address bus (22, 24) having a plurality of address lines;
a data bus (23, 25) having a plurality of data lines;
a control bus having a plurality of control lines;
a microprocessor (10) directly connected to each of the address lines and data lines of said address and data bus, and coupled to said control bus; and
first and second random access memory units (20, 21),

**characterised in that**:

each memory unit is connected to different lines of said address bus and different lines of said data bus, so that said random access memory unit may be separately addressed.

**2.** A system according to claim 1 **characterized by** a program memory (11) for controlling the operation of said microprocessor (10) and a program for addressing said first and second random access memory units (20,21) to store the same data therein.

**3.** A system according to claim 2 **characterized in that** said program addresses correspond to storage locations of said first and second memory units (20,21), corresponding data being stored therein or read therefrom at different times.

**4.** A system according to claim 2 or 3 **characterized in that** said program simultaneously stores different data in said first and second memory units (20, 21) at non-corresponding address locations, whereby instantaneously occurring errors affect the data stored in said first and second memory units in different manners.

**5.** A system according to any one of claims 1 to 4 **characterized by** means responsive to differences in data stored in first and second memory units (20,21) for disabling further operation of said microprocessor (10).

**6.** A system according to any one of claims 1 to 5 **characterized in that** said random access memory units (20,21) are nonvolatile.

**7.** An electronic postage meter system having, a microprocessor (10), addressable and redundant nonvolatile memory means (20,21), said nonvolatile memory means having two separate nonvolatile memory units (20,21), a control bus having a plurality of control lines coupled to the microprocessor, an address bus means (22,24) connected to said nonvolatile memory means and said microprocessor (10), and a data bus means (23,25) connected to said nonvolatile memory means (20,21) and said microprocessor (10), each memory unit being connected to different lines of said address bus and different lines of said data bus, so that said random access memory units may be separately addressed, wherein:

said microprocessor (10) is programmed to generate data for sequentially writing to said nonvolatile memory means (20,21) and to read data from said nonvolatile memory means (20,21) such that said data is redundantly written in respective ones of said memory units; and
means are provided for causing said data to be stored in said respective nonvolatile memory units (20,21) in different forms.

**8.** An electronic postage meter system as claimed in claim 7 wherein said means for causing said data to be stored in different forms comprises a coder-decoder means (30,31) for receiving said data and encoding said data prior to said data being written to a first one of said nonvolatile memory units and for decoding said data upon retrieval of said data

from said first nonvolatile memory unit.

**9.** An electronic postage meter system as claimed in claim 7 wherein said means for causing said data to be stored in different forms comprises:

a first coder-decoder means (30) for receiving said data and encoding said data prior to said data being written to a first one of said nonvolatile memory units (20) and for decoding said data upon retrieval of said data from said first nonvolatile memory unit; and
a second coder-decoder means (31) for receiving said data and encoding said data prior to said data being written to a second one (21) of said nonvolatile memory units and for decoding said data upon retrieval of said data from said second nonvolatile memory unit.

**10.** An electronic postage meter system as claimed in any of claims 6 to 9 wherein said nonvolatile memory units are of the type employing battery back-up, EAROM or EEPROM.

**Patentansprüche**

**1.** Elektronisches Frankiermaschinensystem mit

einem Adressbus (22, 24) mit einer Vielzahl von Adressleitungen;

einem Datenbus (23, 25) mit einer Vielzahl von Datenleitungen;

einem Steuerbus mit einer Vielzahl von Steuerleitungen;

einem Mikroprozessor (10), der direkt mit jeder der Adressleitungen und Datenleitungen des Adress- und Datenbusses verbunden und mit dem Steuerbus gekoppelt ist; und

ersten und zweiten Speichereinheiten (20, 21) mit wahlfreiem Zugriff,

***dadurch gekennzeichnet, dass***

jeder Speicher mit verschiedenen Leitungen des Adressbusses und verschiedenen Leitungen des Datenbusses verbunden ist, so dass die Speicher mit wahlfreiem Zugriff separat adressiert werden können.

**2.** System nach Anspruch 1, ***gekennzeichnet durch*** einen Programmspeicher (11) zum Steuern des Betriebs des Mikroprozessors (10) und ein Programm zum Adressieren der ersten und zweiten Speichereinheiten (20, 21) mit wahlfreiem Zugriff, um dieselben Daten darin zu speichern.

**3.** System nach Anspruch 2, ***dadurch gekennzeichnet, dass*** die Programmadressen Speicherstellen der ersten und zweiten Speichereinheiten (20, 21) entsprechen, wobei entsprechende Daten zu verschiedenen Zeiten darin gespeichert oder daraus gelesen werden.

**4.** System nach Anspruch 2 oder 3, ***dadurch gekennzeichnet, dass*** das Programm gleichzeitig verschiedene Daten in den ersten und zweiten Speichereinheiten (20, 21) an nicht entsprechenden Adressenstellen speichert, wodurch momentan auftretende Fehler die in den ersten und zweiten Speichereinheiten gespeicherten Daten in verschiedenen Weisen beeinflussen.

**5.** System nach einem der Ansprüche 1 bis 4, ***gekennzeichnet durch*** Einrichtungen, die auf Unterschiede in ersten und zweiten Speichereinheiten (20, 21) gespeicherten Daten ansprechen, um einen weiteren Betrieb des Mikroprozessors (10) zu sperren.

**6.** System nach einem der Ansprüche 1 bis 5, ***dadurch gekennzeichnet, dass*** die Speichereinheiten (20, 21) mit wahlfreiem Zugriff nicht flüchtig sind.

**7.** Elektronisches Frankiermaschinensystem mit einem Mikroprozessor (10), adressierbaren und redundanten, nicht flüchtigen Speichereinrichtungen (20, 21), wobei die nicht flüchtigen Speichereinrichtungen zwei separate, nicht flüchtige Speichereinheiten (20, 21) aufweisen, einen Steuerbus mit einer Vielzahl von mit dem Mikroprozessor gekoppelten Steuerleitungen, einer Adressbuseinrichtung (22, 24), die mit den nicht flüchtigen Speichereinrichtungen und dem Mikroprozessor (10) verbunden ist, und einer Datenbuseinrichtung (23, 25), die mit den nicht flüchtigen Speichereinrichtungen (20, 21) und dem Mikroprozessor (10) verbunden ist, wobei jede Speichereinheit mit unterschiedlichen Leitungen des Adressbus und mit unterschiedlichen Leitungen des Datenbus verbunden, so dass sich Speichereinheiten mit wahlfreiem Zugriff getrennt adressieren lassen, wobei der Mikroprozessor (10) programmierbar ist, Daten zum sequentiellen Schreiben in die nicht flüchtigen Speichereinrichtungen (20, 21) zu erzeugen, und Daten aus den nicht flüchtigen Speichereinrichtungen (20, 21) zu lesen, so dass die Daten redundant in jeweilige der Speichereinheiten eingeschrieben werden; und Einrichtungen vorgesehen sind, um zu bewirken, dass die Daten in die jeweiligen, nicht flüchtigen Speichereinheiten (20, 21) in verschiedenen For-

men gespeichert werden.

**8.** Elektronisches Frankiermaschinensystem nach Anspruch 7, ***dadurch gekennzeichnet, dass*** die Einrichtung zum Bewirken, dass die Daten in verschiedenen Formen gespeichert werden, eine Codier-Decodiereinrichtung (30, 31) zum Empfangen der Daten und Codieren der Daten, bevor die Daten in eine erste der nicht flüchtigen Speichereinheiten geschrieben werden, und zum Decodieren der Daten nach Auslesen der Daten aus der ersten, nicht flüchtigen Speichereinheit umfasst.

**9.** Elektronisches Frankiermaschinensystem nach Anspruch 7, ***dadurch gekennzeichnet, dass*** die Einrichtung zum Bewirken, dass die Daten in verschiedenen Formen gespeichert werden, umfasst:

eine erste Codier-Decodiereinrichtung (30) zum Empfangen der Daten und Codieren der Daten, bevor die Daten in eine erste der nicht flüchtigen Speichereinrichtungen (20) eingeschrieben werden, und zum Decodieren der Daten nach Auslesen der Daten aus der ersten, nicht flüchtigen Speichereinheit;

eine zweite Codier-Decodiereinrichtung (31) zum Empfangen der Daten und Codieren der Daten, bevor die Daten in eine zweite (21) der nicht flüchtigen Speichereinheiten eingeschrieben werden, und zum Decodieren der Daten nach Auslesen der Daten aus der zweiten, nicht flüchtigen Speichereinheit.

**10.** Elektronisches Frankiermaschinensystem nach einem der Ansprüche 6 bis 9, ***dadurch gekennzeichnet, dass*** die flüchtigen Speichereinheiten vom Typ mit Batterieunterstützung EAROM oder EEPROM sind.

**Revendications**

**1.** Système de machine à affranchir électronique comprenant :

un bus d'adresse (22, 24) comportant une pluralité de lignes d'adresse ;
un bus de données (23, 25) comportant une pluralité de lignes de données ;
un bus de commande comportant une pluralité de lignes de commande ;
un microprocesseur (10) directement connecté à chacune des lignes d'adresse et des lignes de données desdits bus d'adresse et de données, et couplé audit bus de commande ; et
un premier et un second modules de mémoire à accès aléatoire (20, 21), **caractérisé en ce que** :

chaque module de mémoire est connecté à des lignes différentes dudit bus d'adresse et à des lignes différentes dudit bus de données, de sorte que lesdites mémoires à accès aléatoire peuvent être adressées séparément.

**2.** Système selon la revendication 1, **caractérisé par** une mémoire de programme (11) pour commander le fonctionnement dudit microprocesseur (10) et un programme pour adresser lesdits premier et second modules de mémoire à accès aléatoire (20, 21) pour y stocker les mêmes données.

**3.** Système selon la revendication 2, **caractérisé en ce que** les adresses dudit programme correspondent aux emplacements de stockage desdits premier et second modules de mémoire (20, 21), les données correspondantes y étant stockées ou en étant lues à des instants différents.

**4.** Système selon la revendication 2 ou 3, **caractérisé en ce que** ledit programme stocke simultanément des données différentes dans lesdits premier et second modules de mémoire (20, 21) à des emplacements d'adresses qui ne correspondent pas, de sorte que des erreurs ayant lieu instantanément modifient les données stockées dans lesdits premier et second modules de mémoire de manières différentes.

**5.** Système selon l'une quelconque des revendications 1 à 4, **caractérisé par** des moyens réagissant aux différences des données stockées dans les premier et second modules de mémoire (20, 21), pour désactiver le fonctionnement ultérieur dudit microprocesseur (10).

**6.** Système selon l'une quelconque des revendications 1 à 5, **caractérisé en ce que** lesdits modules de mémoire à accès aléatoire (20, 21) sont non volatiles.

**7.** Système de machine à affranchir électronique comportant, un microprocesseur (10), des moyens de mémoire non volatile adressables et redondants (20, 21), lesdits moyens de mémoire non volatile comportant deux modules de mémoire non volatile séparés (20, 21), un bus de commande comportant une pluralité de lignes de commande couplées au microprocesseur, des moyens de bus d'adresse (22, 24) connectés auxdits moyens de mémoire non volatile et audit microprocesseur (10), et des moyens de bus de données (23, 25) connectés auxdits moyens de mémoire non volatile (20, 21) et audit microprocesseur (10), chaque module de mé-

moire étant connecté à des lignes différentes dudit bus d'adresse et à des lignes différentes dudit bus de données, de façon que lesdits modules de mémoire à accès aléatoire puissent être adressés séparément, dans lequel :

ledit microprocesseur (10) est programmé pour produire des données pour écrire en séquence dans lesdits moyens de mémoire non volatile (20, 21) et pour lire des données provenant desdits moyens de mémoire non volatile (20, 21) de façon que lesdites données soient écrites de manière redondante dans des modules respectifs desdits modules de mémoire ; et
des moyens sont prévus pour provoquer le stockage desdites données dans lesdits modules de mémoire non volatile respectifs (20, 21) sous des formes différentes.

**8.** Système de machine à affranchir électronique selon la revendication 7, dans lequel lesdits moyens pour provoquer le stockage desdites données sous des formes différentes comprennent des moyens de codeur-décodeur (30, 31) pour recevoir lesdites données et coder lesdites données avant que lesdites données ne soient écrites dans un premier module desdits modules de mémoire non volatile et à décoder lesdites données lors de la récupération desdites données provenant dudit premier module de mémoire non volatile.

**9.** Système de machine à affranchir électronique selon la revendication 7, dans lequel lesdits moyens pour provoquer le stockage desdites données sous des formes différentes comprennent :

des premiers moyens de codeur-décodeur (30) pour recevoir lesdites données et coder lesdites données avant que lesdites données ne soient écrites dans un premier module desdits modules de mémoire non volatile (20) et pour décoder lesdites données lors de la récupération desdites données provenant dudit premier module de mémoire non volatile ; et
des seconds moyens de codeur-décodeur (31) pour recevoir lesdites données et coder lesdites données avant que lesdites données ne soient écrites dans un second module (21) desdits modules de mémoire non volatile et pour décoder lesdites données lors de la récupération desdites données provenant dudit second module de mémoire non volatile.

**10.** Système de machine à affranchir électronique selon l'une quelconque des revendications 6 à 9, dans lequel lesdits modules de mémoire non volatile sont du type utilisant une sauvegarde par batterie, EAROM ou EEPROM.

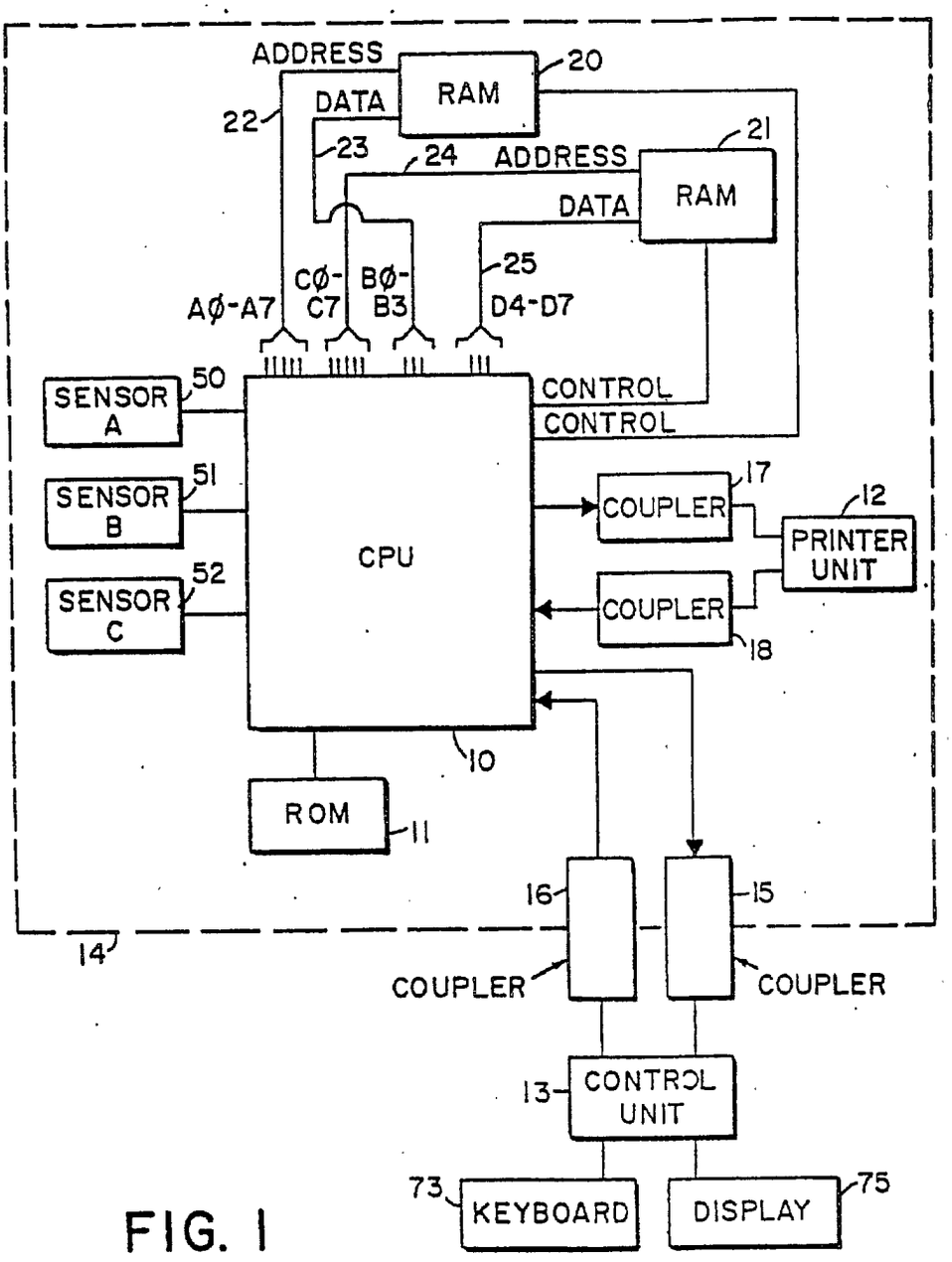
ADDRESS
RAM
20
DATA
22
23
24
ADDRESS
21
RAM
DATA
25
AØ-A7
CØ-C7
BØ-B3
D4-D7
SENSOR A
50
SENSOR B
51
SENSOR C
52
CONTROL
CONTROL
CPU
COUPLER
17
12
PRINTER UNIT
COUPLER
18
10
ROM
11
16
15
14
COUPLER
COUPLER
13
CONTROL UNIT
73
KEYBOARD
DISPLAY
75

FIG. 1

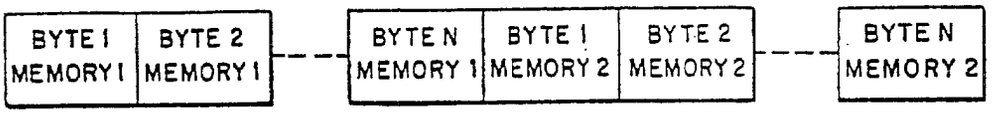


FIG. 2

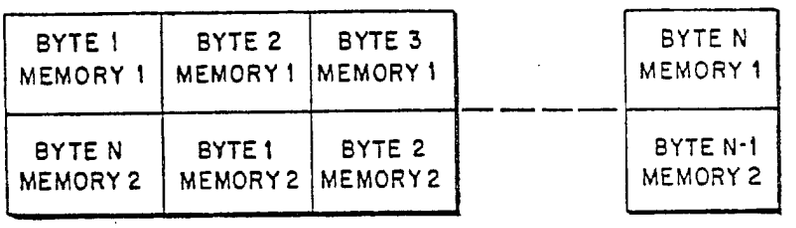


FIG. 3

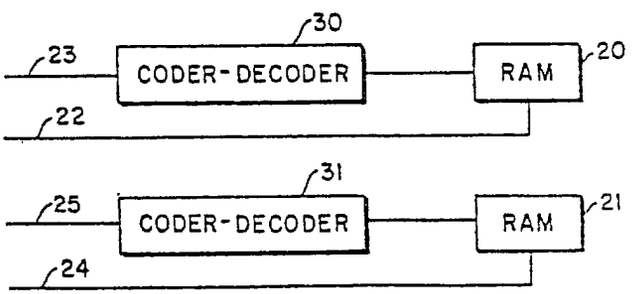


FIG. 4

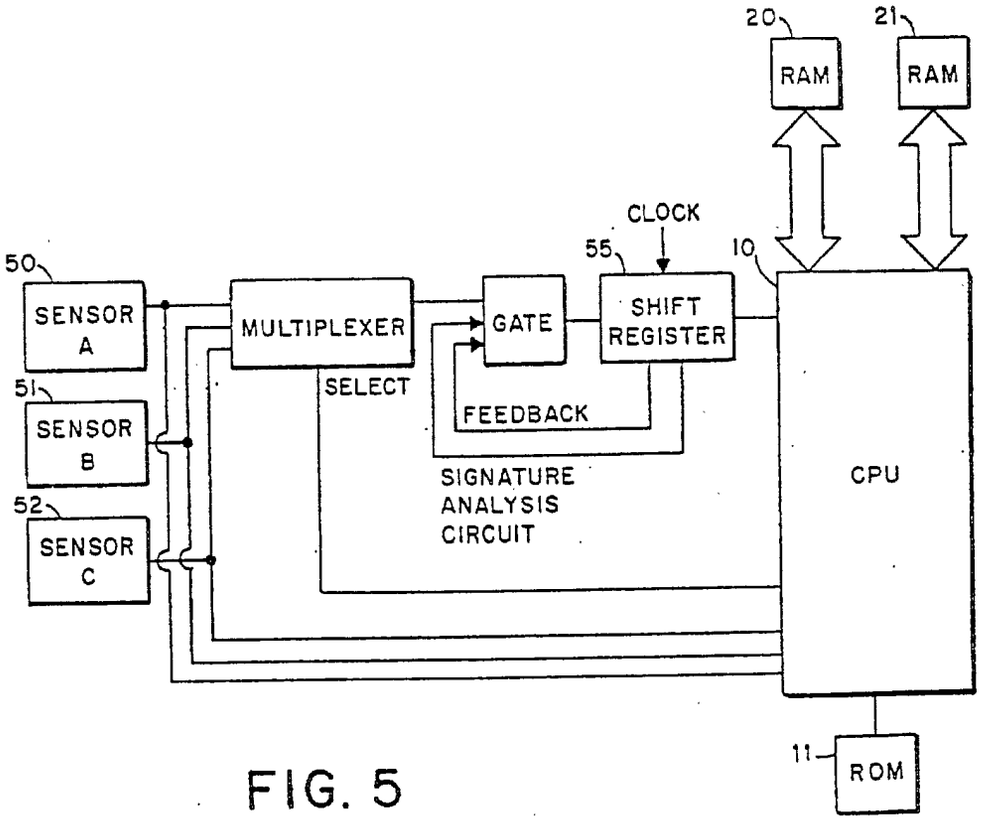
20
RAM
21
RAM
CLOCK
55
10
50
SENSOR A
MULTIPLEXER
GATE
SHIFT REGISTER
51
SENSOR B
SELECT
FEEDBACK
SIGNATURE ANALYSIS CIRCUIT
CPU
52
SENSOR C
11
ROM

FIG. 5

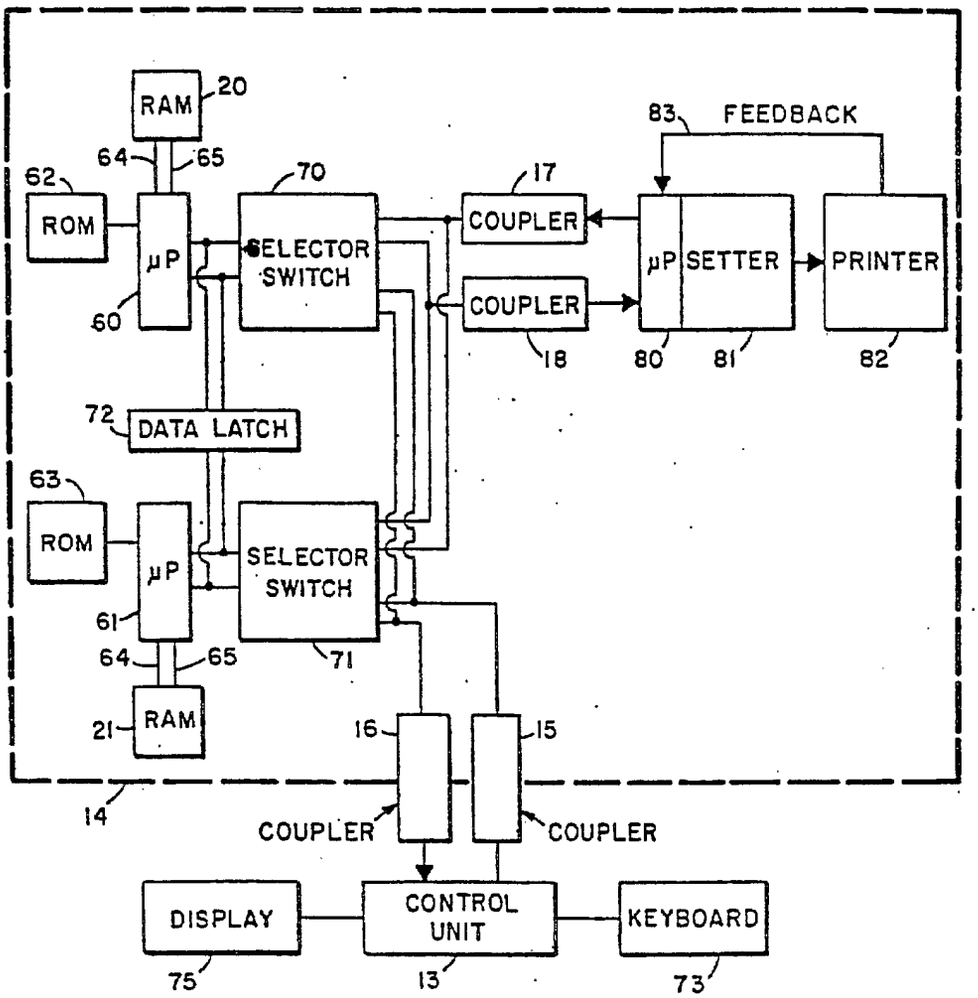
RAM
20
64
65
62
ROM
μP
60
70
SELECTOR SWITCH
17
COUPLER
COUPLER
18
83
FEEDBACK
μP
SETTER
80
81
PRINTER
82
72
DATA LATCH
63
ROM
μP
61
64
65
RAM
21
SELECTOR SWITCH
71
16
15
14
COUPLER
COUPLER
DISPLAY
CONTROL UNIT
KEYBOARD
75
13
73

FIG. 6