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(54) **Microprocessor video display system.**

(57) In a microprocessor video display system a pixel-mapped video memory (10) can be accessed both by the CPU (12) and by video display logic (14) which delivers video data to the display. Contrary to accepted practice, contention between simultaneous access requests from the CPU and video display logic is avoided by the video display logic deferring its access request for one video memory access period. This is acceptable because: the video control logic can access data at a rate twice that required by the display, the video memory access cycle rate is the same as the CPU clock rate, and the microprocessor accesses the memory for one clock period during operation cycles lasting three or four clock pulses. The CPU operation is thus kept at its maximum speed without the video data being adversely delayed.

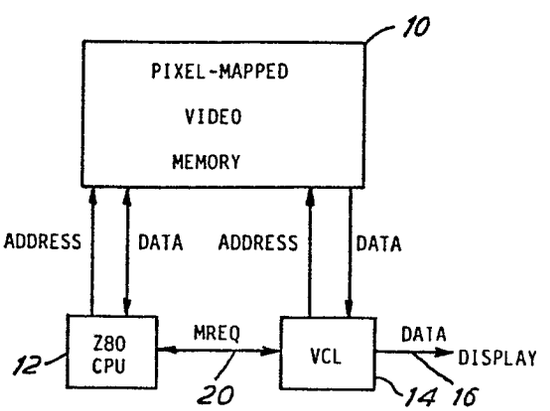

FIG. 2

EP 0 241 288 A2

MICROPROCESSOR VIDEO DISPLAY SYSTEM

This invention relates to a microprocessor video display system of the type in which a microprocessor CPU (central processor unit) and video control logic for producing the video image signal for display share a common video memory.

A Z80 microprocessor can be used in such an arrangement, with the video memory directly accessible by both the microprocessor CPU and the video control logic (VCL). In this situation, it is necessary to provide an arbitration scheme to cope with the situation where simultaneous memory accesses are attempted by both the CPU and the VCL. This situation is termed "contention".

The standard solution to the problem of providing a piece of memory accessable by both the CPU and the VCL is to prevent access by the CPU to the video memory during video data read operations by the VCL. This is normally done with a signal called WAIT, which forces the CPU to suspend memory access cycles and go into an inactive state, and so prevents contention. However, this reduces the performance of the CPU because it must then spend part of its time inactive, with the result that the programs running on it run more slowly.

The present inventor has however appreciated that this inactivity can be avoided in normal circumstances. The invention is defined in the appended claims to which reference should now be made.

In a microcomputer system such as for example one based on the Z80 microprocessor and with a pixel-mapped video display, it is necessary for the video control logic to read data regularly from the video memory to convert it into the signals to drive the display device, which may be, for example, a television set. It is not possible for the VCL to delay data read operations, or there would be gaps visible in the displayed picture. The display system is therefore organised so that the time necessary for the given video data read operation, i.e. the time it takes for that data to be displayed on the video display device, corresponds to the time it

takes for twice that amount of data to be read from the video memory. The inventor has appreciated therefore, that it may be considered that a given video data read cycle has an interval of two video memory cycle times during which the video data read cycle may take place.

The inventor has also appreciated that it can be assumed that the CPU will not perform two video memory access cycles in a row, providing the video memory access rate and the CPU clock rate are substantially the same. This assumption is valid because the Z80 performs two basic types of memory cycle, the opcode fetch cycle and the data read or write cycle. The opcode fetch cycle is four clock periods long, and the memory read or write cycle is three clock periods long. Therefore, the shortest possible interval is between two consecutive memory read or write cycles, which will be three cycle times apart.

Thus in accordance with this invention in such a system the contention mechanism operates on the basis that during the first of the two video memory cycles available to the VCL for each pixel the video data ready cycle will occur, unless the CPU wishes to perform a video memory cycle, in which case the video data ready cycle is deferred until the second of the cycles times in its interval. If a video memory read cycle has taken place in the first of these two cycles then a CPU cycle may freely take place in the second. Therefore both the video display mechanism and the CPU have what is effectively non-delayed access to the video memory.

An example of the invention will now be described in more detail by way of example with reference to the accompanying drawing, in which:

Figure 1 is a block diagram of the relevant part of a known microprocessor video display system, and

Figure 2 is a block diagram of the corresponding part of a microprocessor video display system embodying the invention.

Both figures illustrate a pixel-mapped video memory 10 accessible both by a Z80 CPU 12 and by video control logic (VCL) 14 which supplies data on an output 16 to a video display device (not shown) incorporating a cathode ray tube screen.

In the known arrangement of Figure 1, when the VCL 14 calls for a data item from the memory 10 it also sends a WAIT command 18 to the CPU, if the CPU is also attempting to address the video memory, to render the CPU inactive for one video memory access cycle so as to avoid any danger of contention. This is logical enough because the display device has to be fed an uninterrupted supply of data otherwise the display will have gaps in it.

In accordance with this invention the VCL does not send a WAIT command to the CPU but, as shown in Figure 2, the VCL makes an enquiry MREQ of the CPU as to whether the CPU is attempting to addrerss video memory, and if it is the VCL defers its video memory read operation by one video memory cycle period. This goes contrary to the accepted practice because it introduces delay into the video data for the display.

However, because the video data can in fact be read from the video memory twice as fast as is necessary to supply the display, the present inventor has appreciated that a delay of just one video memory cycle period can be tolerated. Furthermore, because the video memory access rate is equal to the CPU clock rate, and each CPU operation cycle takes at least two CPU clock periods, only one of which will ever involve a video memory access, the CPU will never call for video memory access on two successive CPU clock periods.

Deferring of a VCL video memory read cycle will thus never arise on two successive video memory access cycles and the VCL will thus always be able to maintain delivery of video data at the required rate to the display.

In summary, therefore, the mechanism described and illustrated is used in a microcomputer application to allow the memory which holds the video display data to be read by both the microprocessor and the video display hardware. This it does in a manner which causes no reduction in the performance of the microprocessor, by interleaving the video read cycles between the microprocessor memory cycles in such a manner that a video read cycle may be shifted to allow the microprocessor immediate access to the memory. The standard mechanism to perform this would delay the microprocessor cycle, and therefore reduce the performance of the microprocessor.

In the present system the microprocessor CPU can have the maximum possible performance as it is not degraded by the video control logic.

CLAIMS

1. A microprocessor video display system comprising a video memory, a CPU capable of accessing the video memory for one clock period during operation cycles each lasting two or more CPU clock periods, video control logic for accessing the video memory during selected video memory read cycles to provide data to a video display device, the video control logic being capable of accessing the video memory at a rate twice as fast as the rate at which data is required to be delivered to the video display device, and the video memory read cycle rate being substantially equal to the CPU clock rate, and in which when both the CPU and the video display device desire access to the video memory the operation of the video control logic is deferred by one video memory access period.

2. A microprocessor video display system according to claim 1, in which the CPU is comprised by a Z80 microprocessor.

3. A microprocessor video display system according to claim 1 or 2 in which the video memory is a pixel-mapped video memory.

4. A microprocessor video display system substantially as herein described with reference to and as shown in Figure 2 of the drawing.

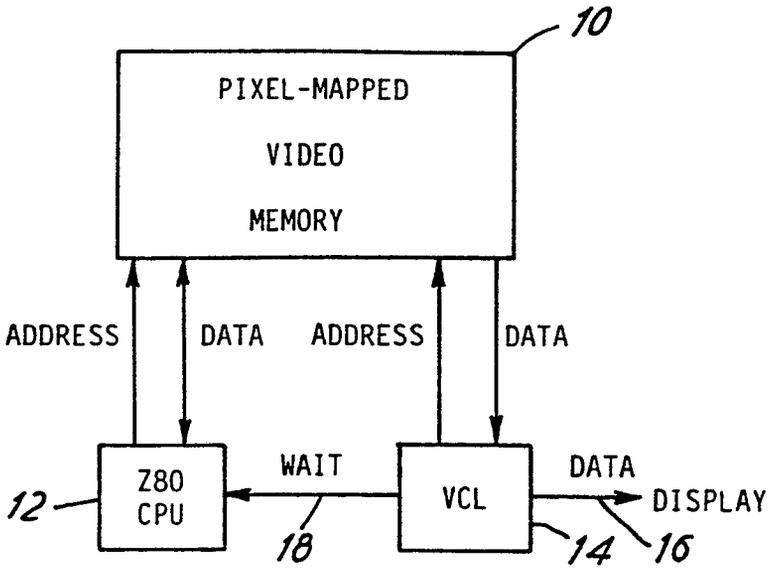
10
PIXEL-MAPPED
VIDEO
MEMORY
ADDRESS
DATA
ADDRESS
DATA
Z80
CPU
12
WAIT
18
VCL
DATA
DISPLAY
14
16

FIG. 1

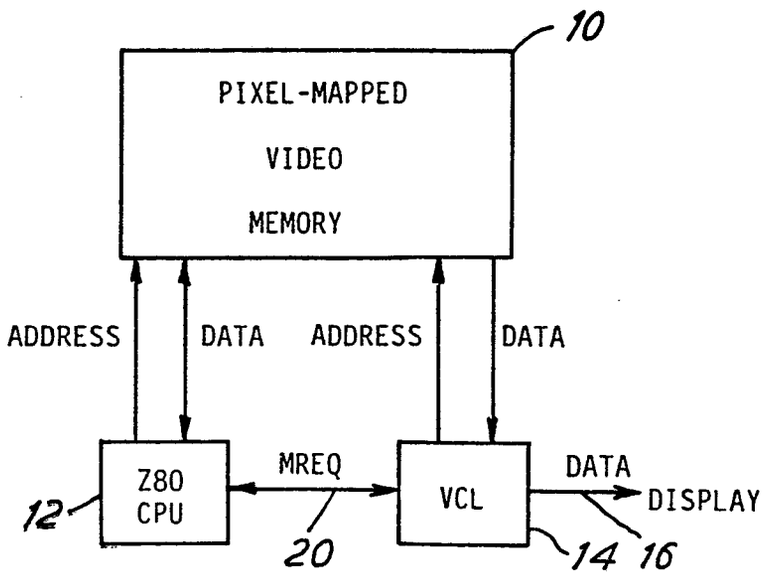
10
PIXEL-MAPPED
VIDEO
MEMORY
ADDRESS
DATA
ADDRESS
DATA
Z80
CPU
12
MREQ
20
VCL
DATA
DISPLAY
14
16

FIG. 2