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(54) **Microprocessor video display system.**

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EP 0 241 288 B1

Description

This invention relates to a microprocessor video display system of the type in which a microprocessor CPU (central processor unit) and video control logic for producing the video image signal for display share a common video memory.

A Z80 microprocessor can be used in such an arrangement, with the video memory directly accessible by both the microprocessor CPU and the video control logic (VCL). In this situation, it is necessary to provide an arbitration scheme to cope with the situation where simultaneous memory accesses are attempted by both the CPU and the VCL. This situation is termed "contention".

The stardard solution to the problem of providing a piece of memory accessable by both the CPU and the VCL, an example of which is described in Electronics Volume 52, No. 14, pages 136-139, is to prevent access by the CPU to the video memory during video data read operations by the VCL. This is normally done with a signal called WAIT, which forces the CPU to suspend memory access cycles and go into an inactive state, and so prevents contention. However, this reduces the performance of the CPU because it must then spend part of its time inactive, with the result that the programs running on it run more slowly.

The present inventor has however appreciated that this inactivity can be avoided in normal circumstances. The invention is defined in the appended claims to which reference should now be made.

In a microcomputer system such as for example one based on the Z80 microprocessor and with a pixel-mapped video display, it is necessary for the video control logic to read data regularly from the video memory to convert it into the signals to drive the display device, which may be, for example, a television set. It is not possible for the VCL to delay data read operations, or there would be gaps visible in the displayed picture. The display system is therefore organised so that the time necessary for the given video data read operation, i.e. the time it takes for that data to be displayed on the video display device, corresponds to the time it takes for twice that amount of data to be read from the video memory. The inventor has appreciated therefore, that it may be considered that a given video data read cycle has an interval of two video memory cycle times during which the video data read cycle may take place.

The inventor has also appreciated that it can be assumed that the CPU will not perform two video memory access cycles in a row, providing the video armory access rate and the CPU clock rate are substantially the same. This assumption is valid because the Z80 performs two basic types of memory cycle, the opcode fetch cycle and the data read or write cycle. The opcode fetch cycle is four clock periods long, and the memory read or write cycle is three clock periods long. Therefore, the shortest possible interval is between two consecutive memory read or write cycles, which will be three cycle times apart.

Thus in accordance with this invention in such a system the contention mechanism operates on the basis that during the first of the two video memory cycles available to the VCL for each pixel the video data ready cycle will occur, unless the CPU wishes to perform a video armory cycle, in which case the video data ready cycle is deferred until the second of the cycles times in its interval. If a video memory read cycle has taken place in the first of these two cycles then a CPU cycle may freely take place in the second. Therefore both the video display mechanism and the CPU have what is effectively non-delayed access to the video memory.

An example of the invention will now be described in more detail by way of example with reference to the accompanying drawing, in which:

Figure 1 is a block diagram of the relevant part of a known microprocessor video display system, and

Figure 2 is a block diagram of the corresponding part of a microprocessor video display system embodying the invention.

Both figures illustrate a pixel-mapped video memory 10 accessible both by a Z80 CPU 12 and by video control logic (VCL) 14 which supplies data on an output 16 to a video display device (not shown) incorporating a cathode ray tube screen.

In the known arrangement of Figure 1, when the VCL 14 calls for a data item from the memory 10 it also sends a WAIT command 18 to the CPU, if the CPU is also attempting to address the video armory, to render the CPU inactive for one video memory access cycle so as to avoid any danger of contention. This is logical enough because the display device has to be fed an uninterrupted supply of data otherwise the display will have gaps in it.

In accordance with this invention the VLC does not send a WAIT command to the CPU but, as shown in Figure 2, the VCL makes an enquiry MREQ of the CPU as to whether the CPU is attempting to address video memory, and if it is the VCL defers its video memory read operation by one video memory cycle period. This goes contrary to the accepted practice because it introduces delay into the video data for the display.

However, because the video data can in fact be read from the video memory twice as fast as is necessary to supply the display, the present inventor has appreciated that a delay of just one video memory cycle period can be tolerated. Furthermore, because the video memory access rate is equal to the CPU clock rate, and each CPU operation cycle takes at least two CPU clock periods, only one of which will ever involve a video memory access, the CPU will

never call for video memory access on two successive CPU clock periods.

Deferring of a VCL video memory read cycle will thus never arise on two successive video memory access cycles and the VCL will thus always be able to maintain delivery of video data at the required rate to the display.

In summary, therefore, the mechanism described and illustrated is used in a microcomputer application to allow the memory which holds the video display data to be read by both the microprocessor and the video display hardware. This it does in a manner which causes no reduction in the performance of the microprocessor, by interleaving the video read cycles between the microprocessor memory cycles in such a manner that a video read cycle may be shifted to allow the microprocessor immediate access to the memory. The standard mechanism to perform this would delay the microprocessor cycle, and therefore reduce the performance of the microprocessor. In the present system the microprocessor CPU can have the maximum possible performance as it is not degraded by the video control logic.

Claims

1. A microprooessor video display system comprising a video memory (10), a CPU (12) capable of accessing the video memory for one clock period during operation cycles each lasting two or more CPU clock periods, video control logic (14) for accessing the video memory during selected video memory read cycles to provide data to a video display device, the video control logic being capable of accessing the video memory at a rate twice as fast as the rate at which data is required to be delivered to the video display device, characterised in that the video memory read cycle rate is substantially equal to the CPU clock rate, and in that when both the CPU and the video display device desire access to the video memory the operation of the video control logic is deferred by one video memory access period.

2. A microprocessor video display system according to claim 1, characterised in that the CPU is comprised by a Z80 microprocessor.

3. A microprocessor video display system according to claim 1 or 2, characterised in that the video memory is a pixel-mapped video memory.

4. A method of operating a microprocessor video display system including a CPU, a video memory, video control logic, and a video display device, the method comprising the steps of accessing the video memory with the CPU for one clock period during an operation cycle lasting two or more CPU clock periods, reading data from the video memory with the video control logic at a read cycle rate twice as fast as the rate at which data is required to be delivered to the video display device, delivering data to the video display device at the required rate, characterised in that the read cycle rate is substantially equal to the CPU clock rate and by deferring the operation of the video control logic by one video memory access period when the CPU is accessing the video memory.

Patentansprüche

1. Ein Mikroprozessor-Video-Anzeigesystem mit einem Video-Memory (10), einem zentralen Prozessor CPU (12), der so ausgelegt ist, daß er für ein Taktintervall während Betriebszyklen auf das Video-Memory zugreifen kann, die jeweils zwei oder mehr Taktzyklen des zentralen Prozessors dauern, einer Video-Steuerlogik (14) zum Zugreifen auf den Video-Speicher während ausgewählter Lesezyklen bezüglich des Video-Speichers, um Daten für eine Video-Anzeigeeinrichtung bereitzustellen, wobei die Video-Steuerlogik so ausgelegt ist, daß sie auf den Video-Speicher mit einer Geschwindigkeit zugreift, die doppelt so schnell ist wie die Geschwindigkeit, mit der Daten zur Video-Anzeigeeinrichtung geliefert werden, dadurch gekennzeichnet, daß die Lesezyklengeschwindigkeit bezüglich des Video-Speichers im wesentlichen dem Taktzyklus des zentralen Prozessors entspricht und daß dann, wenn sowohl der zentrale Prozessor als auch die Video-Anzeigeeinrichtung auf den Video-Speicher zugreifen wollen, der betrieb der Video-Steuerlogik um einen Zugriffszyklus bezüglich des Video-Speichers verzögert wird.

2. Mikroprozessor-Video-Anzeigesystem gemäß Anspruch 1, dadurch gekennzeichnet, daß als zentraler Prozessor ein Z80-Mikroprozessor vorgesehen ist.

3. Mikroprozessor-Video-Anzeigesystem gemäß einem der Ansprüche 1 oder 2, dadurch gekennzeichnet, daß der Video-Speicher ein Pixel-Format aufweist.

4. Verfahren zum Betreiben einer Mikroprozessor-Video-Anzeigeeinrichtung mit einem zentralen Prozessor, einem Video-Speicher, einer Video-Steuerlogik und mit einer Video-Anzeigeeinrichtung, wobei folgende Schritte vorgesehen sind: Zugreifen auf den Video-Speicher mittels des zentralen Prozessors für einen Taktzyklus während eines Betriebszyklus, der zwei oder mehr Taktzyklen des zentralen Prozessors dauert, Auslesen von Daten aus dem Video-Speicher mit der Video-Steuerlogik mit einer Lesezyklusgeschwindigkeit, die doppelt so schnell ist wie die Geschwindigkeit, mit der Daten zur Video-Anzeigeinrichtung zu übertragen sind, und Abgeben von Daten an die Video-Anzeigeeinrichtung mit der geforderten Geschwindigkeit, dadurch gekennzeichnet, daß die Lesezyklusgeschwindigkeiet im wesentlichen gleich ist der Taktgeschwindigkeit des zentralen Prozessors und daß der Betrieb der Video-

Steuerlogik dann um eine Zugriffszeitspanne bezüglich des Video-Speichers verzögert wird, wenn der zentrale Prozessor auf den Video-Speicher zugreift.

Revendications

1. Système d'affichage vidéo à microprocesseur comprenant une mémoire vidéo (10), une CPU (12) capable d'accéder à la mémoire vidéo pendant une période d'horloge lors de cycles de fonctionnement qui durent chacun deux ou plus périodes d'horloge de la CPU, une logique de'commande vidéo (14) pour accéder à la mémoire vidéo pendant des cycles choisis de lecture de la mémoire vidéo pour fournir des données à un dispositif d'affichage vidéo, la logique de commande vidéo étant capable d'accéder à la mémoire vidéo à une fréquence double de celle à laquelle les données doivent être fournies au dispositif d'affichage vidéo, caractérisé en ce que la fréquence du cycle de lecture de la mémoire vidéo est à peu près égale à la fréquence d'horloge de la CPU, et en ce que lorsque la CPU et le dispositif d'affichage vidéo désirent accéder en même temps à la mémoire vidéo, le fonctionnement de la logique de commande vidéo est retardé d'une période d'accès à la mémoire vidéo.

2. Système d'affichage vidéo à microprocesseur selon la revendication 1, caractérisé en ce que la CPU comprend un microprocesseur Z80.

3. Système d'affichage vidéo à microprocesseur selon la revendication 1 ou 2, caractérisé en ce que la mémoire vidéo est une mémoire vidéo organisée en pixels.

4. Procédé de fonctionnement d'un système d'affichage vidéo à microprocesseur comprenant une CPU, une mémoire vidéo, une logique de commande vidéo et un dispositif d'affichage vidéo, ledit procédé comprenant les étapes d'accès à la mémoire vidéo par la CPU pendant une période d'horloge lors d'un cycle de fonctionnement qui dure deux ou plus périodes d'horloge de la CPU, de lecture de données provenant de la mémoire vidéo par la logique de commande vidéo à une fréquence de cycle de lecture double de la fréquence à laquelle les données doivent être fournies au dispositif d'affichage vidéo, de fourniture des données au dispositif d'affichage vidéo à la fréquence requise, caractérisé en ce:que la fréquence de cycle de lecture est à peu près égale à la fréquence d'horlogue de la CPU et en ce que le fonctionnement de la logique de commande vidéo est retardé d'une période d'accès à la mémoire vidéo lorsque la CPU accède à la mémoire vidéo.

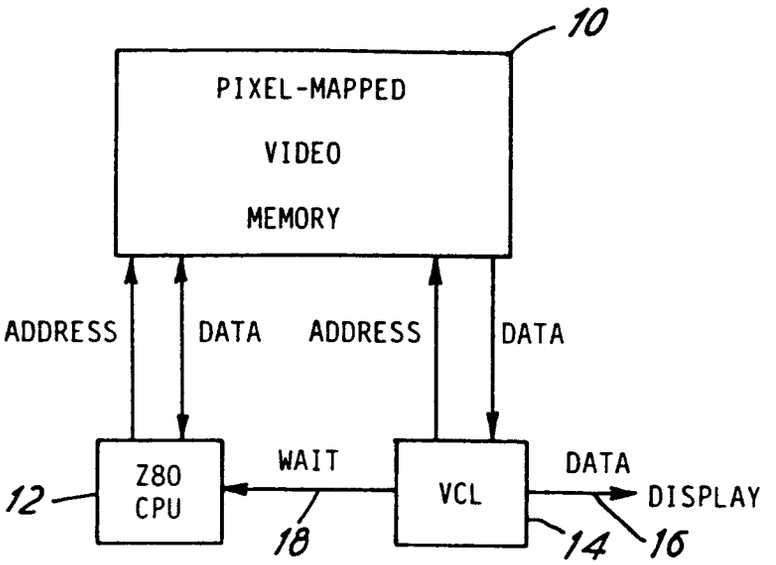
10
PIXEL-MAPPED
VIDEO
MEMORY
ADDRESS
DATA
ADDRESS
DATA
12
Z80
CPU
WAIT
18
VCL
DATA
DISPLAY
14
16

FIG. 1

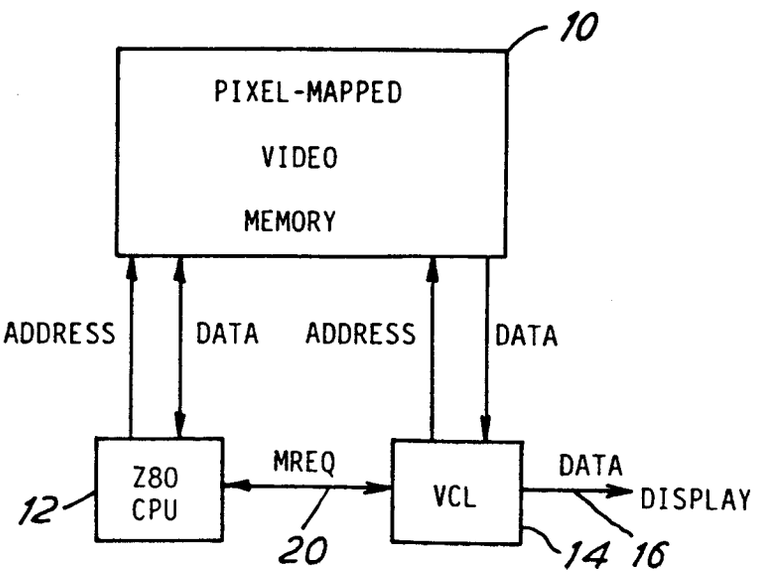
10
PIXEL-MAPPED
VIDEO
MEMORY
ADDRESS
DATA
ADDRESS
DATA
12
Z80
CPU
MREQ
20
VCL
DATA
DISPLAY
14
16

FIG. 2