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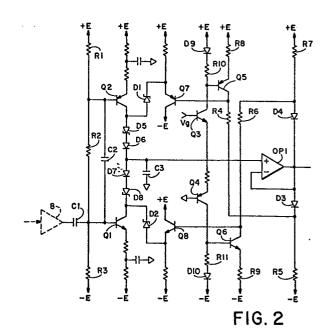
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- Applicant: TEKTRONIX, INC. Tektronix Industrial Park D/S Y3-121 4900 S.W. Griffith Drive P.O. Box 500 Beaverton Oregon 97077(US)
- Inventor: Agoston, Agoston 9995 S.W. Buckskin Terrace Beaverton Oregon 97005(US)
- Representative: Wombwell, Francis et al Potts, Kerr & Co. 15, Hamilton Square Birkenhead Merseyside L41 6BR(GB)
- (54) Memory gate for error sampler.
- 57 A memory gate for an error sampler comprises a memory capacitor having one terminal connected to a reference potential level. A current steering network has an input terminal at which it receives signal current and also has an output terminal connected to the other terminal of the memory capacitor. The current steering network either directs current received at its input terminal to its output terminal or diverts the current from the output terminal, depending on the relationship between the potential at a control terminal of the current steering network and the potential at the output terminal of the current steering network. The potential at the control terminal is biased to follow the potential at the output terminal of the current steering network, and therefore the amount by which the potential at the control terminal must be changed in order to change the state of the current steering network is independent of the voltage on the memory capacitor. A switch circuit is responsive to a gate control signal to place the current steering network in one or other of its states.



**EP 0 24** 

## **EUROPEAN SEARCH REPORT**

EP 87 30 0445

	DOCUMENTS CONSII		1111	
Category	Citation of document with indication, where appropriate, of relevant passages		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Х	FR-A-1 561 347 (ELE RESEARCH) * Figure 2; page 3; column *		1-4	G 01 R 13/34 G 11 C 27/00
Α	US-A-3 474 259 (SIN	IGER)		
Α	US-A-4 142 117 (PRE	ECISION MONOLITHICS)		
A	US-A-3 480 795 (IBM	1)		·
				TECHNICAL FIELDS SEARCHED (Int. Cl.4)
				G 01 R
				G 11 C
	The present search report has be	een drawn up for all claims		
	Place of search	Date of completion of the search		Examiner
TH	E HAGUE	12-05-1988	HOOL	RNAERT W.

CATEGORY OF CITED DOCUMENTS

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