(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 242 468**
A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 86303037.5

(51) Int. Cl.4: G09G 3/36

(22) Date of filing: 22.04.86

(43) Date of publication of application:
28.10.87 Bulletin 87/44

(84) Designated Contracting States:
CH DE FR GB IT LI NL

(71) Applicant: **SEIKO INSTRUMENTS & ELECTRONICS LTD.**
31-1, Kameido 6-chome
Koto-ku Tokyo 136(JP)

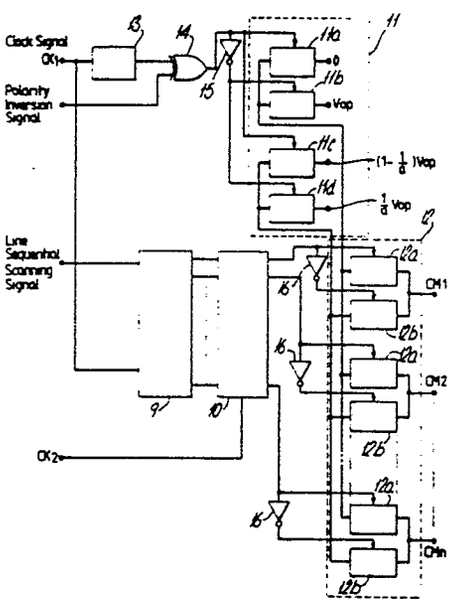
(72) Inventor: **Hara, Mitsuyoshi**
c/o Seiko Instruments & Electronics Ltd
6-31-1, Kameido Koto-ku Tokyo(JP)
Inventor: **Harada, Takamasa**
c/o Seiko Instruments & Electronics Ltd
6-31-1, Kameido Koto-ku Tokyo(JP)
Inventor: **Kondo, Kenichi**
c/o Seiko Instruments & Electronics Ltd
6-31-1, Kameido Koto-ku Tokyo(JP)

(74) Representative: **Caro, William Egerton et al**
J. MILLER & CO. Lincoln House 296-302 High Holborn
London WC1V 7JH(GB)

(54) Liquid crystal display device and method of driving same.

(57) A liquid crystal display device is arranged to be dynamically driven and has a settable frequency divider (13) and a gate circuit (14) for generating a polarity inversion signal at a high frequency at or adjacent a predetermined value in any display state.

Fig.3.



EP 0 242 468 A1

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING SAME

This invention relates to liquid crystal display devices and methods of driving same.

Liquid crystal display devices of the dot matrix type have drawn increasing attention recently, and the size of the display surface of such devices and the number of scanning lines have been increased.

One conventional dynamic driving system for a liquid crystal display device is an A.C. driving method which inverts the polarity of the voltage applied to a liquid crystal material between an electrode selection time and an electrode non-selection time, whenever all the scanning lines are scanned once. This will be referred to hereinafter as the "two-frame A.C. driving system". Such a driving system is described, for example, in "Nikkei Electronics", 1980, August 18, pp 150 - 174.

Figure 7 shows a conventional common electrode driving circuit for a liquid crystal display device. A shift register 27 sequentially shifts a line sequential scanning signal by a clock signal CK1 which is in synchronism with a common electrode scanning speed. A latch circuit 28 latches the signal from the shift register 27 in synchronism with the clock signal CK2 and supplies a driving voltage from a voltage generation circuit 30 to common electrodes CM'_1, CM'_2, ..., CM'_n of the liquid crystal display device through an output gate circuit 29. The driving voltage generation circuit 30 described above receives liquid crystal driving voltages V_{op}, $(1 - \frac{1}{\alpha})V_{op}$, $\frac{1}{\alpha}V_{op}$ and zero (0) potential supplied from a power source (not shown), through analog switches 31a, 31b, 31c, 31d such as transmission gates, respectively, and produces an output pair from the analog switches 31a, 31b which receive the driving voltage V_{op} and the zero potential and also produces an output pair from the analog switches 31c, 31c which receive the driving voltages $(1 - \frac{1}{\alpha})V_{op}$ and $\frac{1}{\alpha}V_{op}$. These output pairs are fed to the output gate circuit 29. The symbol a can be expressed by the equation $a = \sqrt{n} + 1$ where n is the number of scanning lines.

A polarity inversion signal is applied directly and through an inverter 33 to control terminals of the pair of analog switches 31a, 31b and the pair of analog switches 31c, 31d of the driving voltage generation circuit 30 so as to generate zero potential and the driving voltages $(1 - \frac{1}{\alpha})V_{op}$ or V_{op} and $\frac{1}{\alpha}V_{op}$from the driving voltage generation circuit 30.

The output gate circuit 29 has a pair of two analog switches 32a, 32b , for each common electrode and each pair receives the voltages from the driving voltage generation circuit 30. The analog switches 32a directly receive the output signal from the latch circuit 28, and the analog switches 32b receive the output signal from the latch circuit 28 after inversion by an inverter 16.

Figure 8 shows a conventional segment electrode driving circuit of the liquid crystal display device. A shift register 38 receives a data signal and a segment electrode scanning timing, that is, a sub-scanning clock signal CK_2 and shifts the data signal by the clock signal CK_2. A latch circuit 39 latches the signal from the shift register 38 in synchronism with the clock signal CK_2 and supplies the driving voltage from a driving voltage generation circuit 36 to segment electrodes SG'_1, SG'_2, ... SG'_m of the liquid crystal display device through the output gate circuit 37. The driving voltage generation circuit 36 receives liquid crystal driving voltages V_{op}, $(1 - \frac{2}{\alpha})V_{op}$ and $\frac{2}{\alpha}V_{op}$ and a zero potential supplied from a power source (not shown), through analog switches 36 a, 36b, 36c, 36d such as transmission gates, and produces an output pair from the analog switches 36a, 36b that receive the driving voltage V_{op} and the zero potential, and produces an output pair from the analog switches 36c, 36d which receive the driving voltages $(1 - \frac{2}{\alpha})V_{op}$ and $\frac{2}{\alpha}V_{op}$. These output pairs are fed to the output gate circuit 37.

A polarity inversion signal is applied directly and through an inverter 34 to the control terminals of the pairs of analog swtiches 36a, 36b, and 36c, 36d of the driving voltage generation circuit 36 so as to generate the zero potential and the driving voltage $\frac{2}{\alpha}V_{op}$ or the driving voltages V_{op} and $(1 - \frac{2}{\alpha})V_{op}$. The output gate circuit consists of a pair of analog switches 37a, 37b for each segment electrode. Each pair receives voltages from the driving voltage generation circuit 36. The output signal from the latch circuit 39 is directly applied to each analog switch 37a and each analog switch 37b receives the the output of the latch circuit 39 after inversion by an inverter 35.

Next, the operation of the driving circuits of Figures 7 and 8 will be described with reference to Figure 9.

When the line sequential scanning signal is outputted, it is latched by the latch circuit 28 through the shift register 27 and the first common electrode CM'_1 is in a selection state with the other common electrodes CM'_2 .. CM'_n being in a non-selection state.

When the polarity inversion signal is at low level, the driving voltage generation circuit 30 generates the driving voltages V_{op} and $\frac{1}{\alpha}V_{op}$ so that the driving voltage V_{op} is applied to the common electrode CM'_1 whilst the driving voltage a $\frac{1}{\alpha}V_{op}$to the other common electrodes.

In the segment electrode driving circuit of Figure 8, the driving voltage generation circuit 36 outputs the zero potential and the driving voltage $\frac{2}{a}V_{op}$ when the polarity inversion signal is at low level. When the data signal from the latch circuit 39 is at high level, the segment is in the selection state and output zero potential. When the data signal is at low level, it outputs the voltage $\frac{2}{a}V_{op}$.

Figure 9 shows the case where all the data signals are ON and the output waveform is of the common electrode CM'$_1$.

When the polarity inversion signal is at high level, the voltage generation circuit 30 (Figure 7) generates the zero potential and the driving voltage $(1 - \frac{1}{a})V_{op}$ and the voltage generation circuit 36 (Figure 8) generates the driving voltages V_{op} and $(1 - \frac{2}{a})V_{op}$. Therefore, the polarity of the impressed voltage applied to the liquid crystal material of the liquid crystal display device (the potential difference between the common electrode output waveform and the segment electrode output waveform of a pixel) is inverted depending upon the high and low levels of the polarity inversion signal.

Figure 10 shows driving waveforms in the aforementioned two frame A.C. driving system in the case where the number of scanning lines (i.e. the number of common electrodes) is 12. Reference letter H represents the output waveform of the common electrode and reference letter I shows the output waveform of segment electrodes when all of them are ON. Reference letter J representes the output waveform when all the segment electrodes are OFF and reference letter K shows the output waveform when ON and OFF appear alternately. Reference letter L represents the output waveform of the impressed voltage when all the segment electrodes are ON and reference letter M shows the waveform of the liquid crystal impressed voltage when all the segment electrodes are OFF. Reference letter N represents the waveform of the impressed voltage when the segment electrodes are ON and OFF alternately.

With this conventional two frame A.C. driving system, however, the display contrast is defective due to the rise of driving frequency which occurs with increase in the number of scanning lines. For example, when characters are displayed in several lines, cross-talk frequently occurs on the display signal lines between one displayed character and another. When ON pixels are concentrated on one display signal line, cross-talk of the type in which OFF pixels on the same display signal line are turned ON also occurs.

As can be seen clearly from the waveforms indicated by reference letters L, M, N in Figure 10, these problems occur because the frequency of polarity inversion within the non-selection period of the impressed voltage waveform varies markedly depending upon the display content.

The frequency of the impressed voltage in the case of all pixels on a display signal line being ON or all pixels being OFF is very different from that in the case of pixels on a display signal line being ON and OFF in turn. Consequently the cross-talk phenomenon is apt to occur in the case of particular display states. Figure 11 shows the relationship between the frequency of the voltage applied to the liquid crystal material and the threshold voltage of the electro-optical characteristics of the liquid crystal material. The threshold voltage is low at low frequency and high at high frequency. Therefore, even if the display device is driven by the same voltage value, the cross-talk phenomenon occurs partly in the case of particular display states.

Several methods of solving these problems have been proposed in the past.

A first solution is to increase the frame frequency. Since there is a limit to the driving frequency of a liquid crystal controller IC, however, it is not possible to increase the frame frequency to such an extent as to extinguish the cross-talk. Another problem is that current consumption becomes relatively large because the current consumption of the liquid crystal material and the CMOS circuit is determined by charge-discharge current at the time of switching.

A second solution is to reduce the resistance of a transparent conductive film of which the electrodes of the liquid crystal display device are formed, but this does not overcome the problem that transmissivity drops if the film thickness is incre-sed in order to reduce its resistance.

A third solution is to develop liquid crystal materials having less dependency upon the driving waveform frequency, but such liquid crystal materials have not yet been produced.

The present invention seeks to provide a liquid crystal display device free from non-uniform display that is caused by cross-talk.

According to one aspect of the present invention there is provided a liquid crystal display device arranged to be dynamically driven characterised by means for generating a polarity inversion signal at a frequency at or adjacent a predetermined value in any display state.

Preferably further means are provided for inverting the polarity of the voltage applied to liquid crystal material for each scanning frame.

In the preferred embodiment the first-mentioned means comprises frequency divider means settable to a predetermined division ratio and means for modulating a high frequency signal in dependence upon the division ratio to produce said inversion signal.

The divider means may be selectively settable.

According to a further aspect of the present invention there is provided a method of dynamically driving a liquid crystal display device characterised by generating a polarity inversion signal at a frequency at or adjacent a predetermined value in any display state.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a section prospective view of a liquid crystal panel used in one embodiment of a liquid crystal display device according to the present invention,

Figure 2 is a block diagram showing the construction of a liquid crystal display device according to the present invention;

Figures 3 and 4 are block diagrams showing a common electrode driving circuit and a segment electrode driving circuit respectively of the liquid crystal display device of Figure 2;

Figures 5 and 6 are waveform diagrams showing the operation of the liquid crystal display device of Figures 2 to 4;

Figures 7 and 8 show a conventional common electrode driving circuit and a conventional segment electrode driving circuit respectively of a liquid crystal display device;

Figures 9 and 10 are waveform diagrams showing the operation of the driving circuits of Figures 7 and 8;

Figure 11 is a graph showing the relationship between the frequency of applied voltage to liquid crystal material and the threshold voltage thereof; and

Figure 12 is a detailed block diagram showing an embodiment of a liquid crystal display device according to the present invention.

Figure 1 is a perspective view of a liquid crystal display panel of a liquid crystal display device according to the present invention. Substrates 1,2 constitute a cell of a liquid crystal display panel. The substrates 1,2 include common electrodes 1a, 2a respectively which are disposed on the surface of electrically insulating, transparent sheets such as glass, and an insulating film such as, for example, polyimide, Teflon (Trade Mark), etc. is formed on each sheet surface by printing, dipping, etc., and is then rubbed unidirectionally to form uniaxially orientated films 1b,2b, respectively. The substrates 1,2 are disposed parallel to one another in such a manner that their orientated films are opposed with a gap of from several to some dozens of microns between them. A liquid crystal material 5 is charged into this gap. A pair of polariser plates 3,4 are disposed on the outer surfaces of the substrates 1,2 so that the state of orientation of the molecules of the liquid crystal material can be displayed in contrast as darkness and brightness.

The pair of polariser plates 3,4 are arranged in such a fashion that their axes of polarisation are substantially at right angles or parallel to each other, and the rubbing directions are substantially at right angles or parallel to the axes of polarisation.

Incidentally, the present invention is applicable to a liquid crystal display device wherein the liquid crystal material is less than 10 microns thick, a twist angle is greater than 180° but less than 360°, and the ratio d/p is from 0.5 to 0.95 (d: thickness of liquid crystal layer, p: rotation pitch of twist angle of liquid crystal molecules), such as disclosed in Published European Patent Application No. 131,216.

Figure 2 is a block diagram of a liquid crystal display device according to the present invention using the liquid crystal display panel of Figure 1. The reference numeral 6 represents the liquid crystal display panel, the common electrodes and the segment electrodes of which are connected to a common electrode driving circuit 7 and a segment electrode driving circuit 8, respectively.

Figure 3 shows the common electrode driving circuit 7 in detail. A shift register 9 sequentially shifts a line sequential scanning signal in synchronism with a common electrode scanning speed determined by a clock signal CK_2. A latch circuit latches the signal from the shift register 9 in synchronism with the clock signal, and supplies a driving voltage from a driving voltage generation circuit 11 to common electrodes CM_1, CM_2 ... $CM_n$to an output gate circuit 12. The driving voltage generation circuit 11 receives liquid crystal driving voltages V_{op}, $(1 - \frac{1}{a})V_{op}$, $\frac{1}{a}V_{op}$ and zero potential supplied from a power source, (not shown), through analog switches 11a, 11b, 11c, 11d, such as transmission gates, and supplies an output pair from the analog switches 11a, 11 b, that receive the driving voltage V_{op} and the zero potential and an output pair from the analog switches 11c, 11d, that receive the driving voltages $(1 - \frac{1}{a})V_{op}$ and $\frac{1}{a}V_{op}$. The output pairs are fed to the output gate circuit 12.

A 1/N frequency divider 13 divides the frequency of a clock signal CK, and outputs a signal having a frequency which is from 6 to 7 times the frequency of a polarity inversion signal. An exclusive-OR gate 14 receives the signal from the frequency divider 13 and the polarity inversion signal, inverts the former when the polarity inversion signal is applied thereto, and applies, in turn, a signal to the control terminals of the pairs of analog switches 11a, 11b and 11c, 11d directly and through an inverter 15, respectively, so that the driving voltage generation circuit 11 generates the zero potential and the driving voltage $(1 - \frac{1}{a})V_{op}$or the

driving voltage V_{op} and $\frac{1}{a}V_{op}$. The output gate circuit 12 consists of a pair of analog switches 12a, 12b corresponding to each common electrode and receives voltages from the driving voltage circuit 11. The analog switch 12a receives directly the output signal from the latch circuit 10, while the other analog switch 12b receives the output signal from the latch circuit 10 after inversion by an inverter 16.

Figure 4 shows the segment electrode driving circuit 8 in detail. A shift register 18 receives a data signal and segment electrode scanning timing, that is, a sub-scanning clock signal CK_2, to shift the data signal by the clock signal CK_2. A latch circuit 19 latches the signal from the shift register 18 in synchronism with the clock signal CK_2, and supplies driving voltages from a driving voltage generation circuit 20 to segment electrodes SG_1, SG_2... SG_m to an output gate circuit 21. The driving voltage generation circuit 20 receives liquid crystal driving voltages V_{op}, $(1 - \frac{2}{a})V_{op}$, $\frac{2}{a}V_{op}$ and zero potential supplied from a power source (not shown), through analog switches 20a, 20b, 20 c, 20d such as transmission gates, respectively. Output pairs from the analog switches 20a and 20b that receive the driving voltage V_{op} and the zero potential, and output pairs from the analog switches 20c and 20d, that receive the driving voltages $(1 - \frac{2}{a})$-$V_{op}$and $\frac{2}{a}V_{op}$ are fed to the output gate circuit 21.

A 1/N frequency divider 22 and an exclusive-OR gate 23 operate in the same way as the frequency divider 13 and the exclusive-OR gate 14 shown in Figure 3, respectively.

When a polarity inversion signal is applied, the signal phase from the frequency divider 22 is inverted and is applied directly and through an inverter 24 to the pairs of analog switches 20a, 20b and 20c, 20d of the driving voltage generation circuit 20 which thus produces the zero potential and the driving signal $\frac{2}{a}V_{op}$or the driving voltages V_{op} and $(1 - \frac{2}{a})V_{op}$. The output gate circuit 21 consists of a pair of analog switches 21a, 21b for each segment electrode. Each pair of analog switches receives voltages from the driving voltage generation circuit 20. The output signal from the latch circuit 19 is directly applied to one of the analog switches 21a which the other analog switch 21b receives the output signal from the latter circuit after inversion by the inverter 25.

The operation of the liquid crystal display device thus far described will now be explained with reference to the waveform diagram of Figure 5. Figure 5 shows the case where the number of scanning lines is 12 and the output frequency of the frequency divider 13 shown in Figure 3 and the frequency divider 22 shown in Figure 4 is 6 times the polarity inversion signal frequency.

When the line segment scanning signal is outputted, it is latched by the latch circuit 10 through the shift register 9, whereby the first common electrode CM_1 is in a selection state with the other common electrodes CM_2 ... CM_n being in the non-selection state.

On the other hand, the clock signal CK_1 is frequency divided by the frequency divider 13 and a signal having a frequency which is 6 times the polarity inversion signal frequency is produced and applied to the exclusive-OR gate 14. The phase of the signal is inverted when the polarity inversion signal is inputted, and is applied to the driving voltage generation circuit 11. Due to this signal, the voltages tabulated below are outputted to the common electrodes CM_n:

Out put of exclusive-OR gate 14	High		Low	
state of latch circuit 10	selection	non-selection	selection	non-selection
scanning line output voltage	0	$(1 - \frac{1}{a})V_{op}$	V_{op}	$\frac{1}{a}V_{op}$

Figure 5 shows the common electrode output waveform that is outputted in the manner described above.

In the segment electrode driving circuit (Figure 4), the output of the exclusive-OR gate 23 is the same as that of the exclusive-OR gate shown in Figure 3. Due to this signal, the voltages tabulated below are outputted to the segment electrodes SG_m:

Output of exclusive-OR gate 23	High		Low	
state of latch circuit 19	selection	non-selection	selection	non-selection
signal line output voltage	V_{op}	$(1 - \frac{2}{a})V_{op}$	0	$\frac{2}{a}V_{op}$

The segment electrode output waveform shown in Figure 5 represents the case where all the display pixels are ON.

Figure 6 shows an example of the driving waveform in the liquid crystal display device. Figure 6 illustrates the case where the number of common electrodes is 12. Reference letter A represents a common electrode output waveform; reference letter B is a segment electrode output waveform when the data signals are all ON; reference letter C is a segment electrode output waveform at the time all the data signals are OFF; reference letter D is a segment electrode output waveform when ON and OFF data signals apear alternately; reference letter E is a liquid crystal impressed voltage waveform at the time all the segment electrodes are ON; reference letter F is a liquid crystal impressed voltage waveform at the time all the segment electrodes are OFF; and reference letter G is a liquid crystal impressed voltage waveform when the segment electrodes are ON and OFF alternately.

Figure 12 is a detailed block diagram showing an embodiment of the circuit of a liquid crystal display device according to the present invention. In Figure 12, variable counters 40,41 divide the frequency of the clock signal CK_i, a flip-flop circuit 42 divides the output of the variable counter 41 by 2 and an OR circuit or an exclusive-OR gate 43 receives the output of the flip-flop circuit 42 and a polarity inversion signal M. Reference numerals 20,21,11 and 12 represent a segment side driving voltage generation circuit, a segment electrode driving circuit, a common side driving voltage generation circuit and a common electrode driving circuit respectively. The setting values of the variable counters 40, 41 are determined by setting switches 55 to 62 ON or OFF.

The setting values are set by carry signals C1, C2 inverted by inverters 45,46, respectively. A bias voltage supplying circuit 80 comprises resistors 71 to 75 connected in series and the driving voltage (bias voltage) is taken from connecting points between each pair of resistors.

The operation of the circuit shown in Figure 12 will now be explained. The switches 56 and 59 are changed to ON so that the variable counters 40 and 41 have setting values of 1/3 and 1/2, respectively. The clock signal CK_i is divided into 1/3 through the variable counter 40 and the divided signal is further divided by 2 through the variable counter 41. The output signal of the variable counter 41 is furthermore divided by 2 by the flip-flop circuit 42 and is changed into a rectangular wave signal with a duty ratio 1:1. The resulting output Q1 enters one terminal of the exclusive-OR gate 43 and the plurality inversion signal M is received at the other terminal. Therefore, the output Q1 of the flip-flop 42 has its polarity inverted for each frame and operates as a control signal for the segment side driving voltage generation circuit 20 and the common side driving voltage generation circuit 11. The segment side and common side driving voltage generation circuits 20, 11 are formed of transmission gates 63 to 66 and 67 to 70, respectively. In the case where the output of the exclusive-OR gate 43 is 1, the states of transistors 63, 65, 67, 69 are ON, so that the driving voltage is V_{op} and $(1 - \frac{2}{a})V_{op}$ are applied to the segment electrode driving circuit 21, and zero potential and the driving voltage $(1 - \frac{1}{a})V_{op}$ are applied to the common electrode driving circuit 12. On the other hand, in the case where the output of the exclusive-OR gate 43 is 0 the states of the transmission gates 64, 66, 68 and 70 are ON, so that zero potential and the driving voltage $\frac{2}{a}V_{op}$ are applied to the segment electrode driving circuit 21, and the driving voltages V_{op} and $\frac{1}{a}V_{op}$ are applied to the common electrode driving circuit 12. The segment electrode driving circuit 21 and the common electrode driving circuit 12 are formed by transmission gates 76 to 79, the transmission gates being changed by 1 or 0 by the SEG signal and the COM signal, so that the transmission gates produce ON or OFF driving signals.

As described above, the exclusive-OR gate 43 inverts the oututs of the driving voltage generating circuits 20, 11 by the high frequency signal Q1 which is 1/N ^{x} the frequency of the clock signal CK, and inverts for each frame by the polarity inversion signal M.

If the division ratio 1/N is set not to be equal to $1/2^n$, a driving voltage which has a frequency near a predetermined value and the polarity of which is inverted for each frame may be applied to any part of the picture element.

Claims

1. A liquid crystal display device arranged to be dynamically driven characterised by means (13,14; 22,23; 40-43) for generating a polarity inversion signal at a frequency at or adjacent a predetermined value in any display state.

2. A liquid crystal display device as claimed in claimed in claim 1 characterised in that further means (15; 24) are provided for inverting the polarity of the voltage applied to liquid crystal material for each scanning frame.

3. A liquid crystal display device as claimed in claim 1 or 2, characterised in that the first-mentioned means comprises frequency divider means (13; 22; 40,41) settable to a predetermined division ratio and means (14; 23; 43) for modulating a high frequency signal in dependence upon the division ratio to produce said inversion signal.

4. A liquid crystal display device as claimed in claim 1 or 2, characterised in that the divider means (13; 22; 40,41) are selectively settable.

5. A method of dynamically driving a liquid crystal display device characterised by generating a polarity inversion signal at a frequency at or adjacent a predetermined value in any display state.

6. A liquid crystal display device driven by dynamic driving method, wherein the polarity inversion frequency of liquid crystal applied voltage is near a predetermined value in any display states.

7. A liquid crystal display device as claimed in claim 6, wherein the polarity of the liquid crystal applied voltage is inverted for each frame.

Fig.1.

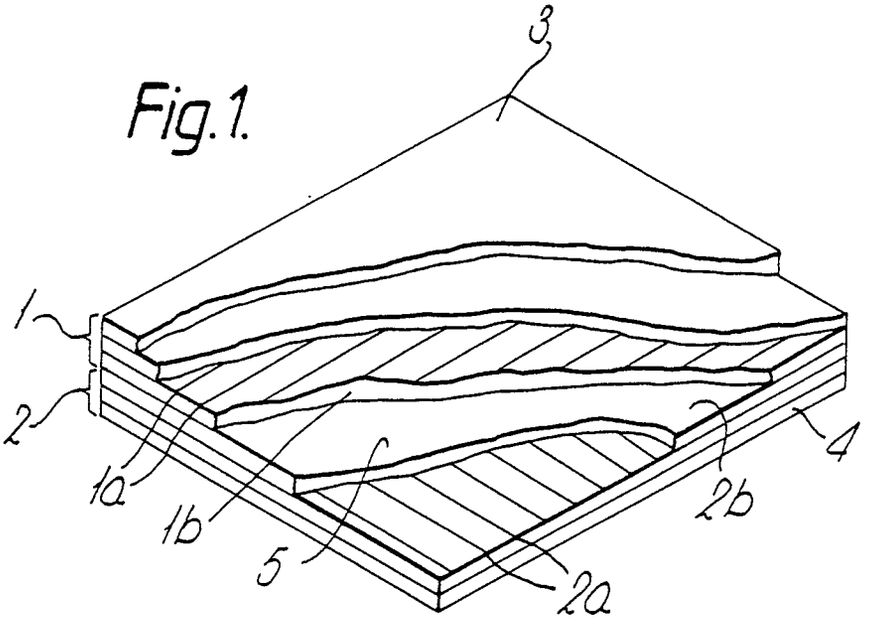

3
1
2
1a
1b
5
2a
2b
4

Fig.2.

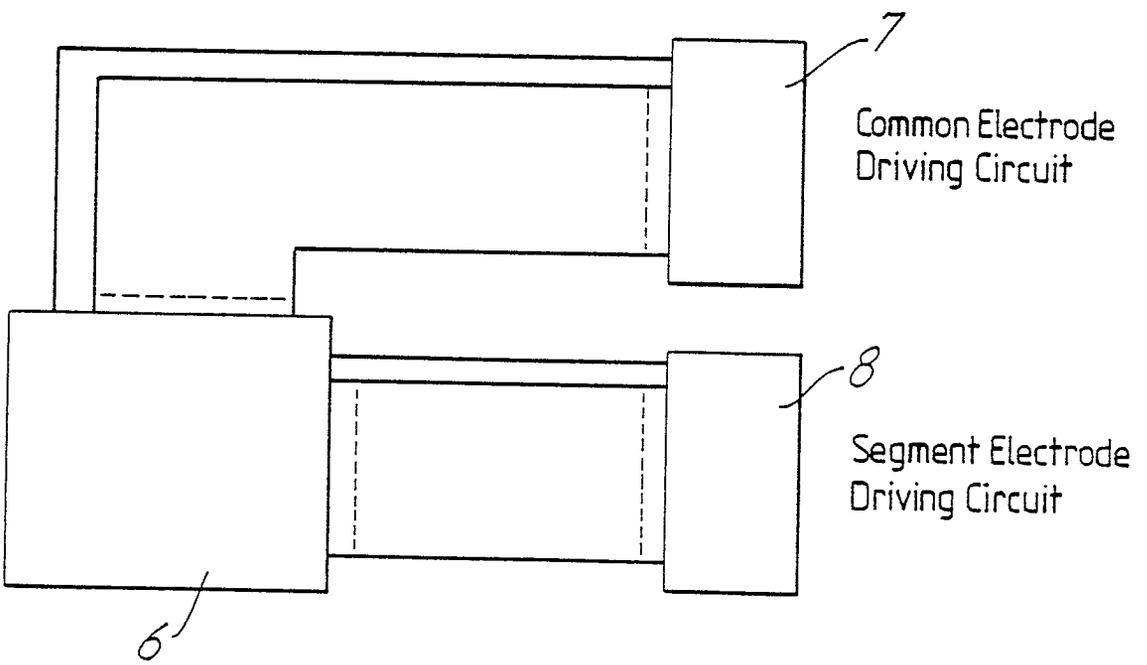

7
Common Electrode
Driving Circuit
8
Segment Electrode
Driving Circuit
6

Fig. 3.

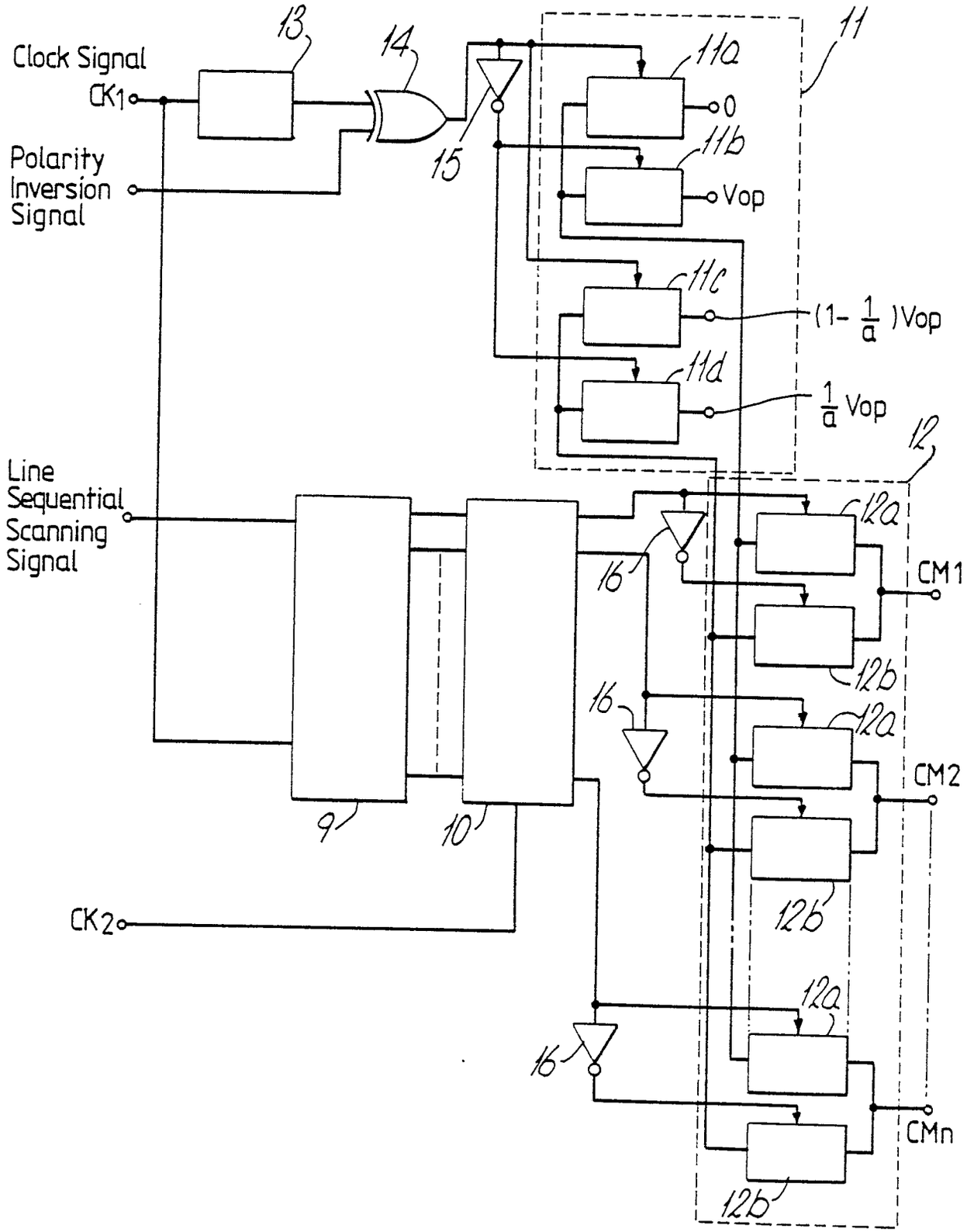

Clock Signal
CK1
Polarity Inversion Signal
13
14
15
11
11a
0
11b
Vop
11c
(1- 1/a)Vop
11d
1/a Vop
12
Line Sequential Scanning Signal
12a
12b
16
CM1
CM2
CMn
9
10
CK2

Fig. 4.

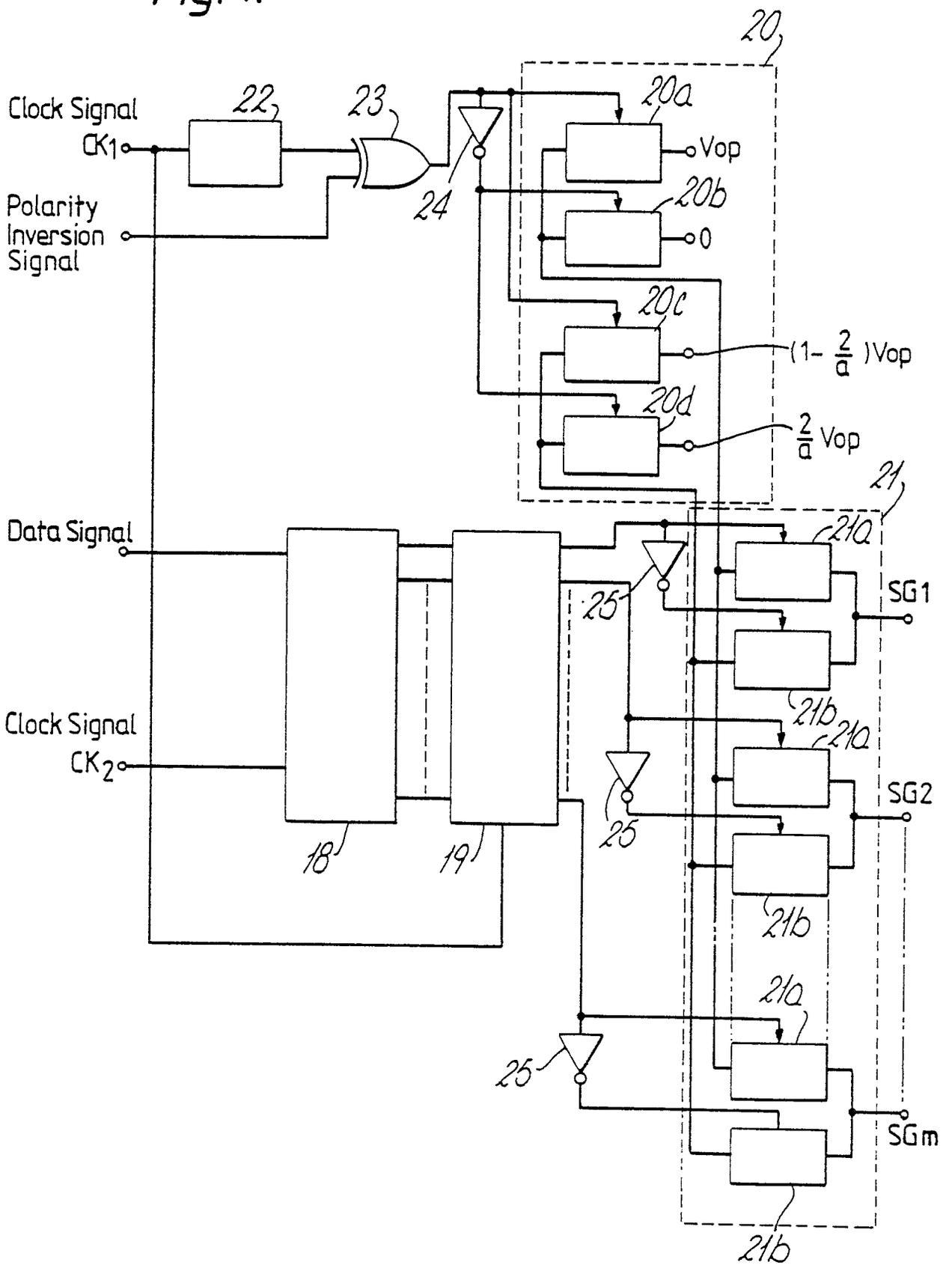

20
Clock Signal
CK1
22
23
24
20a
Vop
20b
0
Polarity Inversion Signal
20c
(1- 2/a)Vop
20d
2/a Vop
21
Data Signal
21a
25
SG1
21b
Clock Signal
CK2
18
19
SG2
SGm

Fig.5.

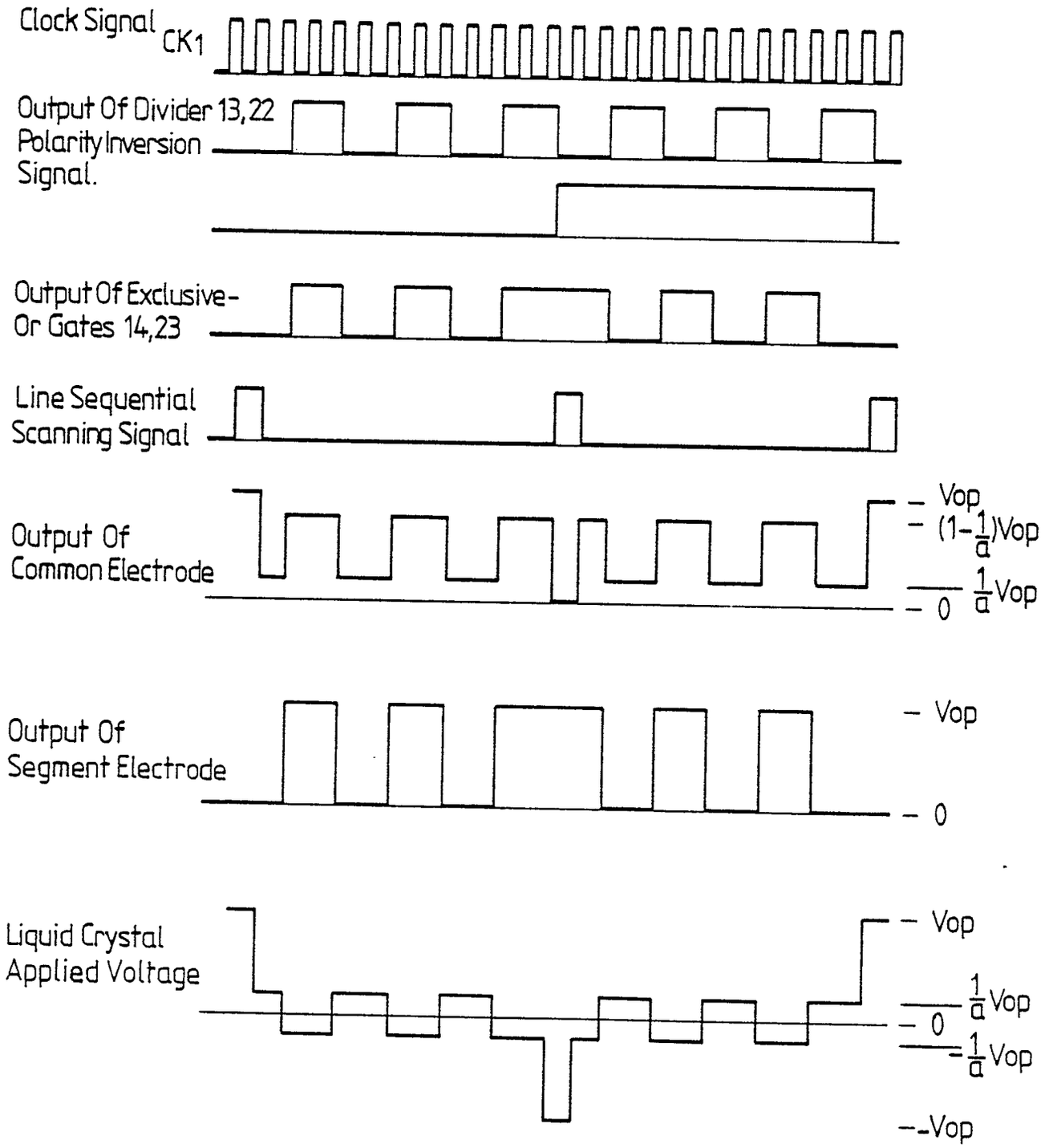

Clock Signal CK1
Output Of Divider 13,22 Polarity Inversion Signal.
Output Of Exclusive-Or Gates 14,23
Line Sequential Scanning Signal
Output Of Common Electrode
Vop
(1-1/a)Vop
1/a Vop
0
Output Of Segment Electrode
Vop
0
Liquid Crystal Applied Voltage
Vop
1/a Vop
0
-1/a Vop
-Vop

Fig.6.

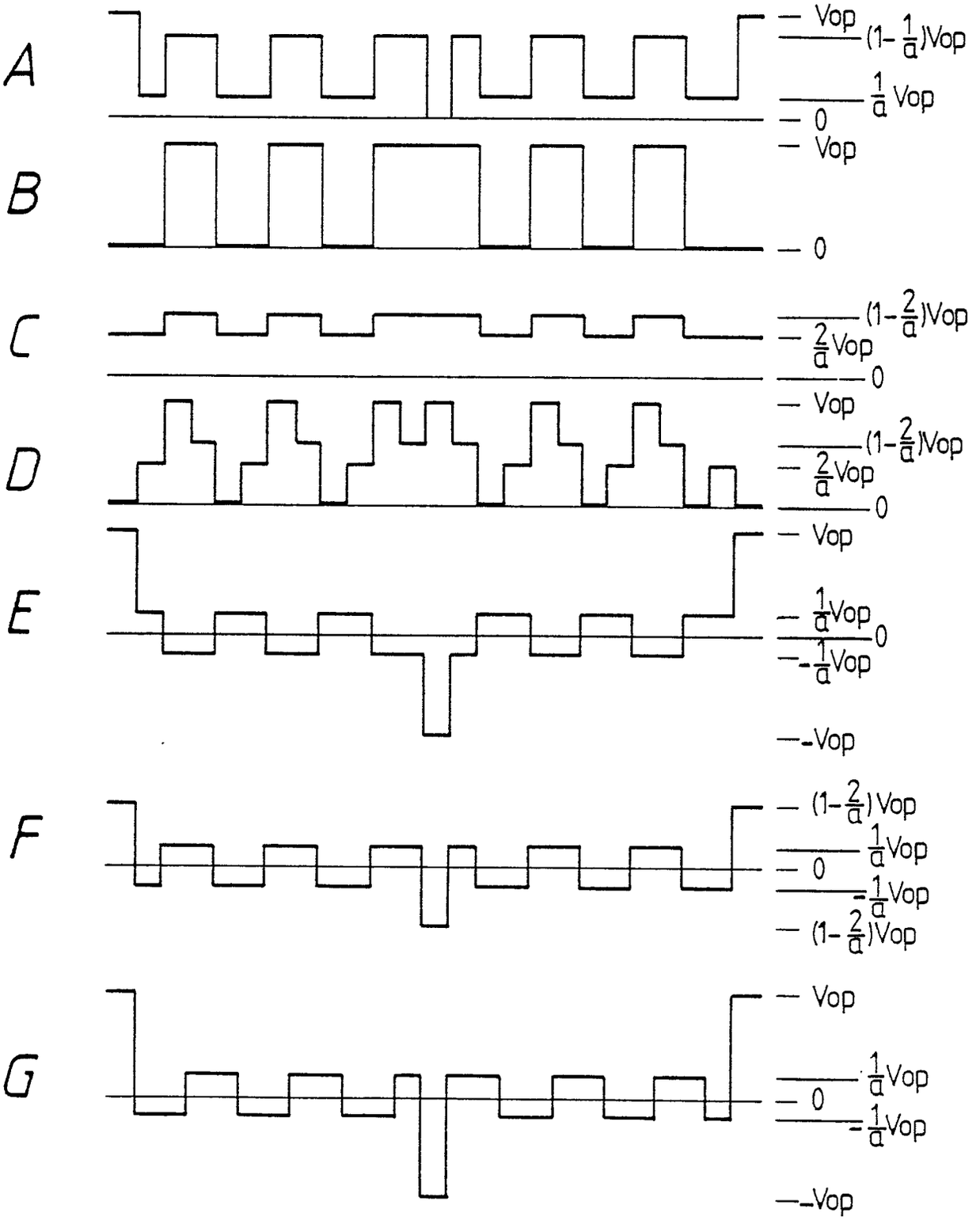

A
B
C
D
E
F
G
Vop
(1-1/a)Vop
1/a Vop
0
Vop
0
(1-2/a)Vop
2/a Vop
0
Vop
(1-2/a)Vop
2/a Vop
0
Vop
1/a Vop
0
-1/a Vop
-Vop
(1-2/a) Vop
1/a Vop
0
-1/a Vop
(1-2/a)Vop
Vop
1/a Vop
0
-1/a Vop
-Vop

Fig. 7.

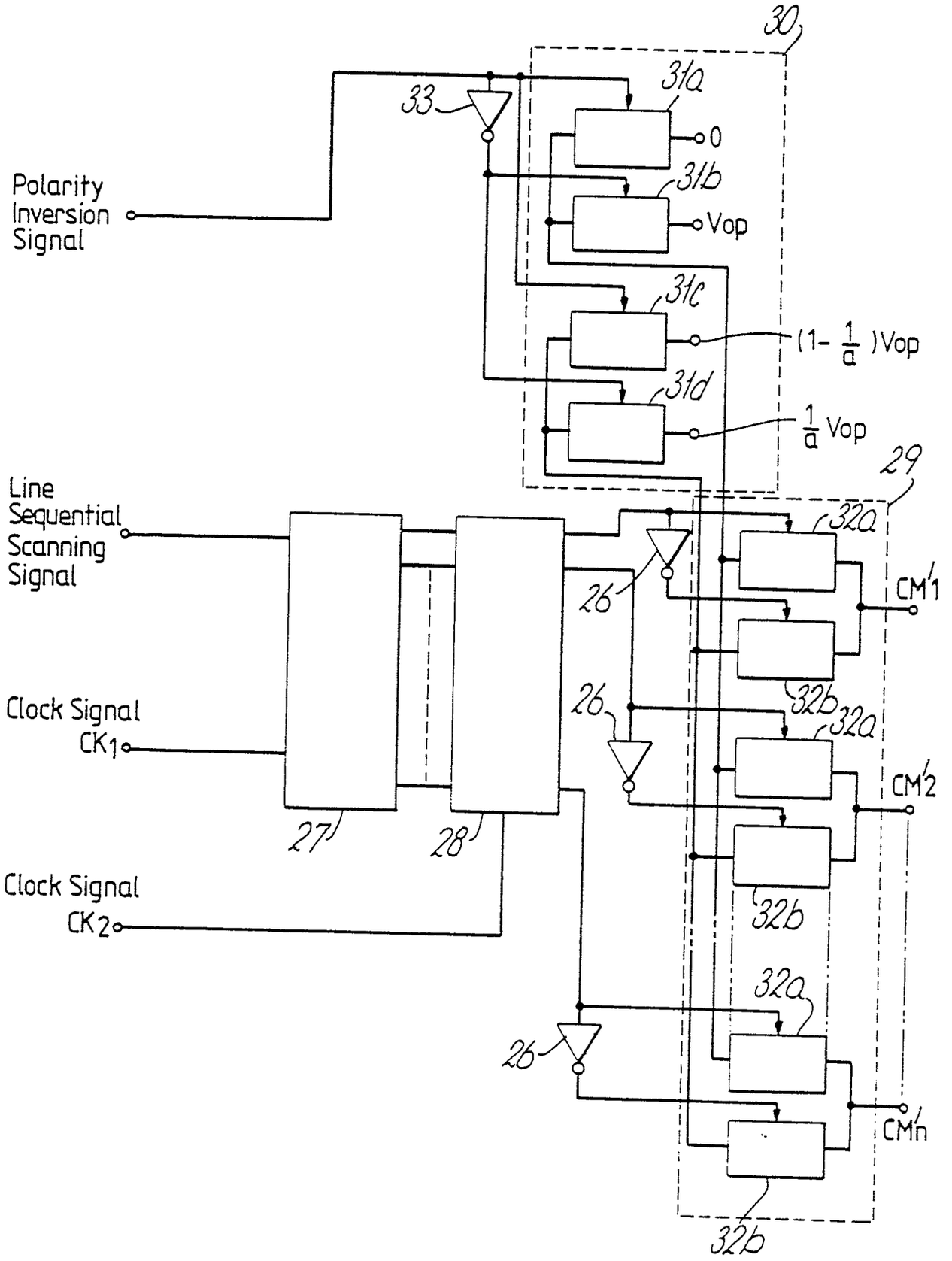

30
31a
33
0
31b
Vop
Polarity Inversion Signal
31c
(1- 1/a)Vop
31d
1/a Vop
29
Line Sequential Scanning Signal
32a
CM'1
26
32b
26
32a
CM'2
Clock Signal CK1
27
28
Clock Signal CK2
32b
32a
26
CM'n
32b

Fig. 8.

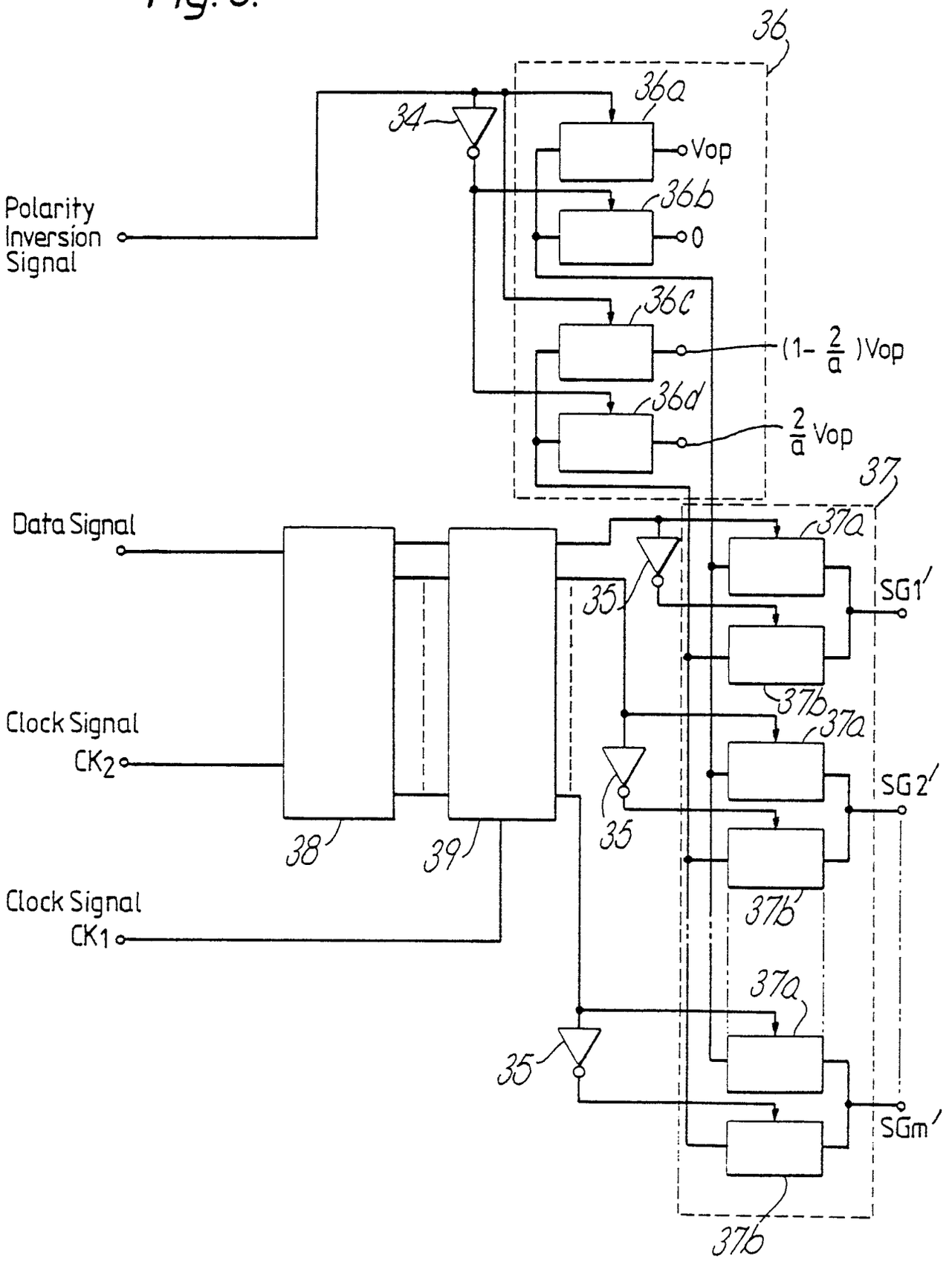

36
36a
34
Vop
36b
0
Polarity
Inversion
Signal
36c
(1- 2/a)Vop
36d
2/a Vop
37
Data Signal
37a
35
SG1'
37b
37a
Clock Signal
CK2
SG2'
35
38
39
37b
Clock Signal
CK1
37a
35
SGm'
37b

Fig.9.

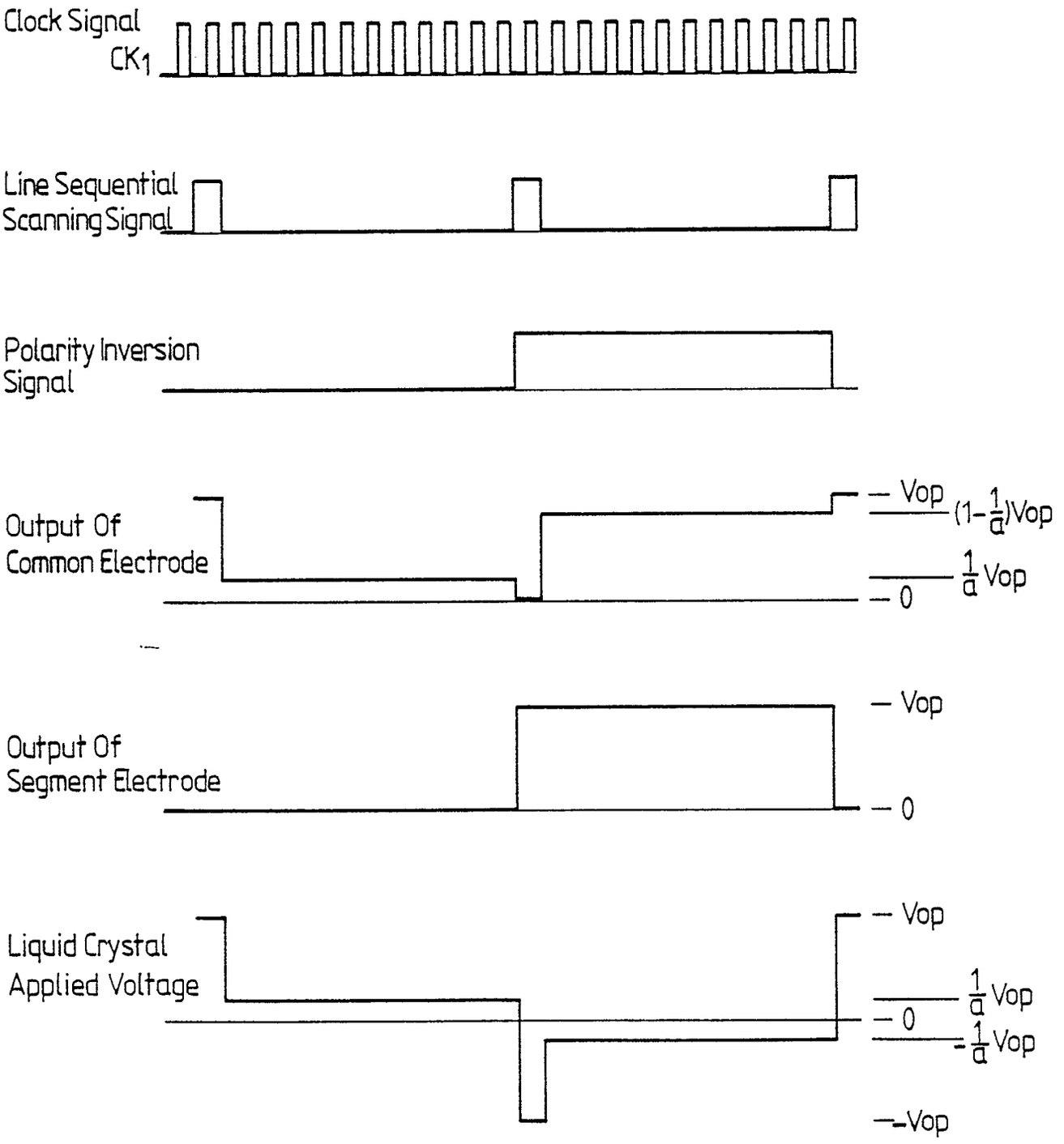

Clock Signal
CK1
Line Sequential
Scanning Signal
Polarity Inversion
Signal
Output Of
Common Electrode
— Vop
(1-1/a)Vop
1/a Vop
— 0
Output Of
Segment Electrode
— Vop
— 0
Liquid Crystal
Applied Voltage
— Vop
1/a Vop
— 0
-1/a Vop
—Vop

Fig.10.

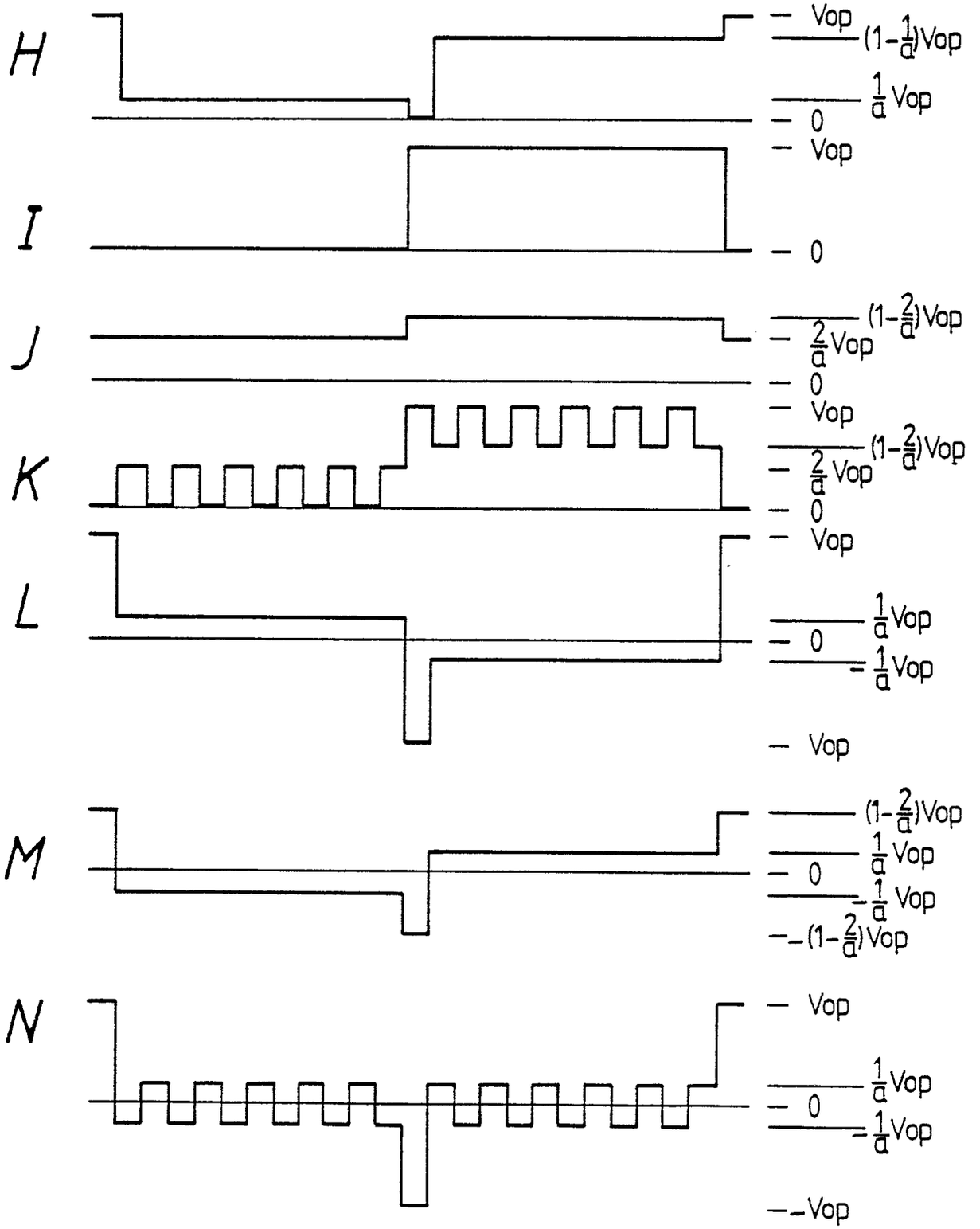
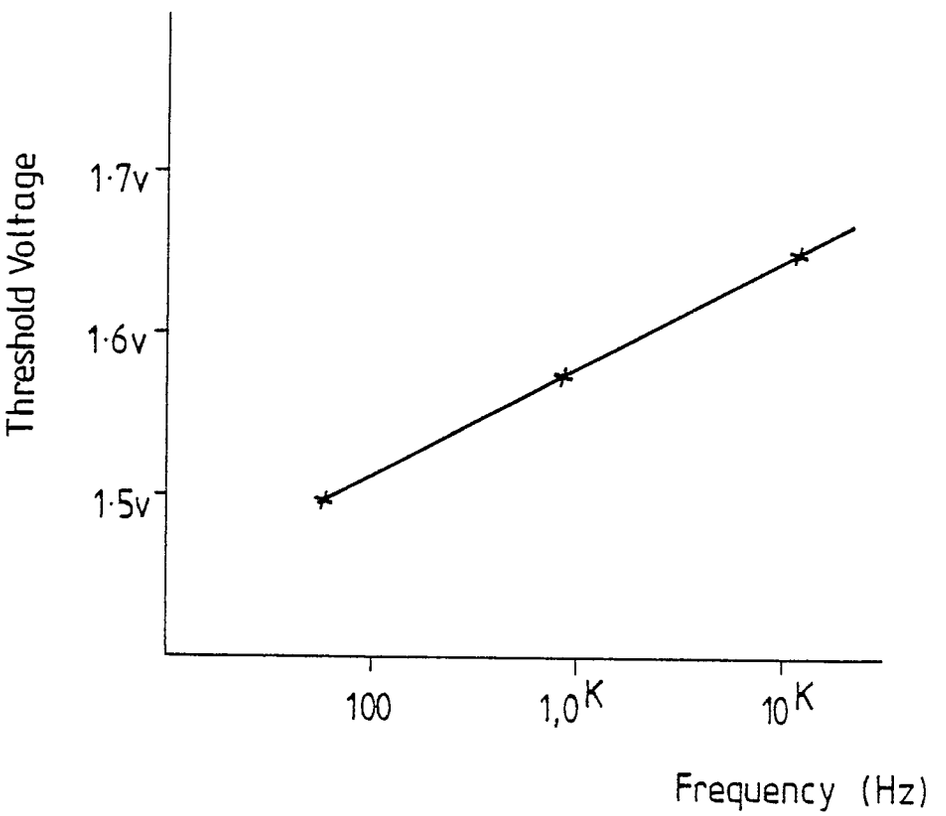

H
Vop
(1-1/a)Vop
1/a Vop
0
I
Vop
0
J
(1-2/a)Vop
2/a Vop
0
K
Vop
(1-2/a)Vop
2/a Vop
0
L
Vop
1/a Vop
0
-1/a Vop
-Vop
M
(1-2/a)Vop
1/a Vop
0
-1/a Vop
-(1-2/a)Vop
N
Vop
1/a Vop
0
-1/a Vop
-Vop

Fig.11.



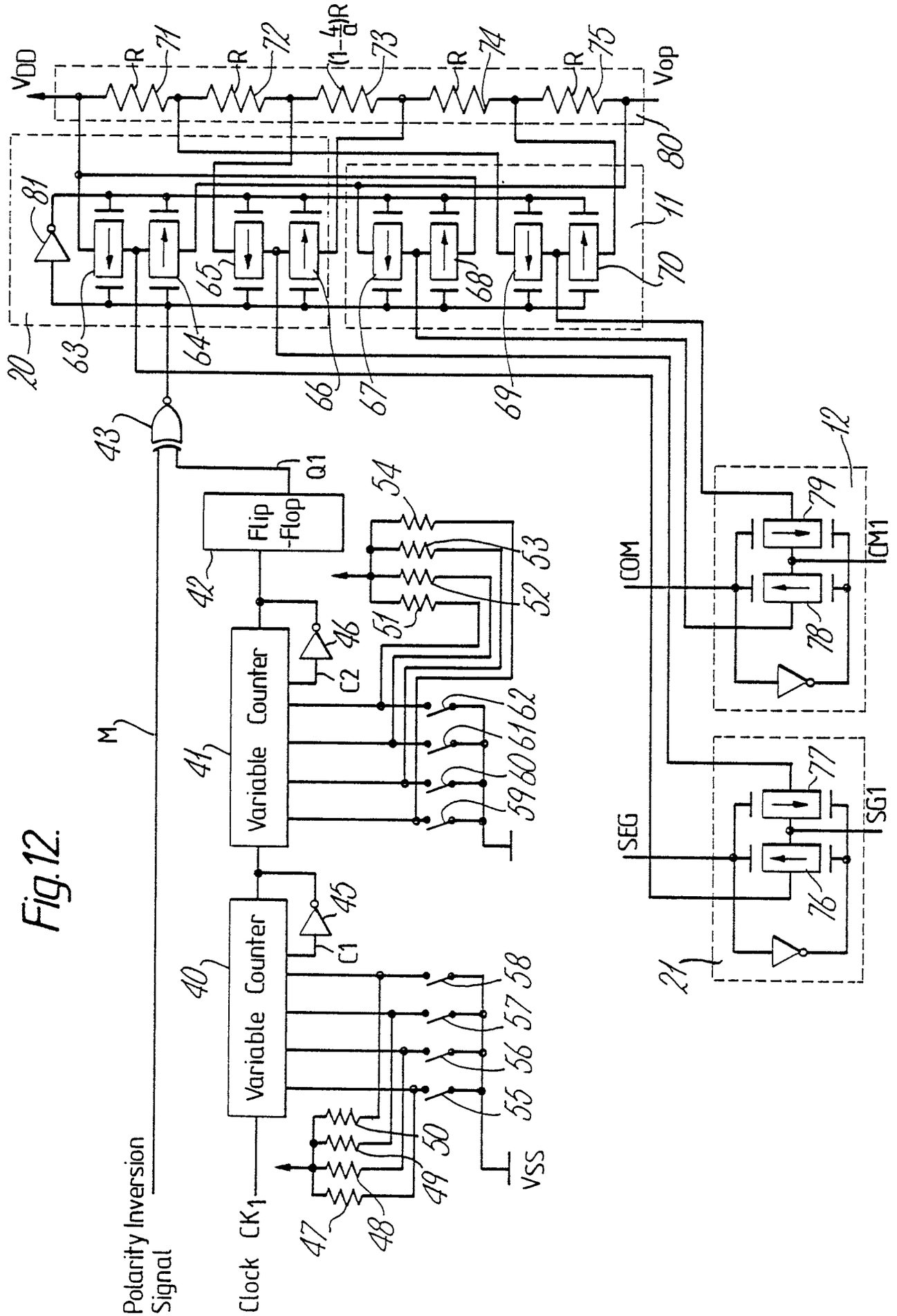

VDD
R
71
R
72
(1-1/n)R
73
R
74
R
75
Vop
80
11
81
20
63
64
65
66
67
68
69
70
43
Q1
Flip
-Flop
42
54
53
52
51
46
C2
41
Variable Counter
M
59
60
61
62
45
C1
40
Variable Counter
58
57
56
55
50
49
47
48
Polarity Inversion
Signal
Clock CK1
VSS
12
79
COM
COM1
78
77
SEG
SG1
76
21

Fig.12

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 86 30 3037

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl 4)
X	EP-A-0 173 158 (HITACHI) * Figures 4-11; abstract; page 6, line 15 - end of document *	1-3,5-7	G 09 G 3/36
A	GB-A-2 075 738 (HITACHI) * Figures 6-8; page 3, line 41 - page 4, line 31 *	1,5,6	
X	EP-A-0 149 899 (SEIKO INSTRUMENTS & ELECTRONICS) * Figures 25-28; page 19, line 16 - end of document *	1,2,5-7	

TECHNICAL FIELDS SEARCHED (Int Cl 4)

G 09 G 3/36

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	22-12-1986	VAN ROOST L.L.A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503 03 82