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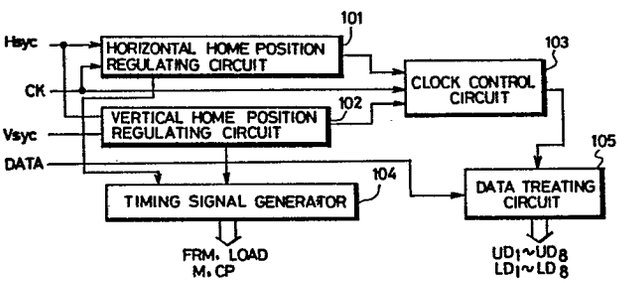
(54) Interface, for example for a liquid crystal display device.

(57) An interface for converting separate video signals into a display data signal and a timing signal for operating a thin display panel comprises a timing circuit (101, 102, 103) for taking a timing so as to introduce effective display data into a data treating circuit (105) according to a synchronizing signal (Hsyc), a data treating circuit (105) for generating desired data for a thin display panel using the display data, and a timing signal generating circuit (104) for generating timing signals necessary for operating a driver of the thin display panel.



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INTERFACE FOR A THIN DISPLAY

This invention relates to interface circuits for example for thin displays, e.g. liquid crystal displays, EL displays, plasma displays or LED displays. More particularly, although not so restricted, the present invention relates to a thin display device having an interface circuit which can be used as a compact and lightweight display device by utilizing interface signals of CRT displays that have gained a wide application particularly in personal computers and the like.

The present invention seeks to provide an interface circuit for a thin display, which has interface functions capable of giving display data to the thin display by using the real-time processing of inputted display data without storing them in a frame buffer memory (RAM) through the use of either a display data synchronizing signal of the CRT display or separate video signals having their composite signals separated.

The liquid crystal display has recently been practised as the display terminal of a personal computer or a word processor by a large-sized dot matrix panel because it is characterized by its thinness, low voltage and low power consumption. At present, a liquid crystal

interface circuit capable of being connected directly with a CRT control circuit is developed so that it may be used as the display terminal of a portable personal computer.

However, the interface circuit of the thin display according to the prior art is designed so that the thin panel is driven even during th blanking period of the CRT display. As a result, the display data is sequentially read out after a frame buffer memory has been prepared to once write the display data therein.

Since, moreover, the interface circuit of the prior art is especially for a monochromatic display, it is short of the quantity of display information in the case of a graphic display or the like. Specifically, the attraction of the display is insufficient as compared with that of the CRT display because one or two of the thin display data of red, green and blue are utilized and displayed simply in the ON-OFF manner on the simple matrix. On the other hand, however, the interface circuit for the multi-colored thin display is not developed yet irrespective of both the establishment of the coloring filters on the surface of the transparent electrodes of a thin panel and the development of a new liquid crystal panel having a storing function such as a panel having built therein an

active element or a nonlinear element such as a TFT (i.e. Thin Film Transistor), metal-insulating film-metal (MIM) or metal-semiinsulator (MSI disclosed in our EP-A-202092A2) or a smectic liquid crystal.

As has been described above, the interface circuit for the thin display according to the prior art is required to prepare the frame buffer memory as an external circuit to write in and read out the data under the administration of the interface circuit. This requirement raises the price of and complicates the circuitry so that the circuit is hard to be assembled into a small-sized display terminal. Moreover, three sets of interface circuits especially for the monochromatic display have to be prepared for constructing the interface circuit for the color thin display so that the price and the structural complexity are increased three times if they are expressed simply.

According to one aspect of the present invention there is provided an interface for converting separate video signals into a display data signal and a timing signal for operating a thin display panel characterised by comprising: timing means for taking a timing so as to introduce effective display data into data treating means according to a synchronizing signal; data treating means for generating desired data for a thin display

panel using said display data; and timing signal generating means for generating timing signals necessary for operating driver means of the thin display panel.

The thin display panel may have a X-Y dot matrix display electrode construction. In one embodiment the X-electrode comprises an uneven-numbered electrode group and an even-numbered electrode group, each of the groups being led out from opposite sides of the panel to each other.

Preferably the data treating means give 8 bits of desired data to the driver.

The timing means may comprise an horizontal home position regulating circuit for controlling a timing so as to introduce horizontal effective display data into the data treating means, a vertical home position regulating circuit for controlling a timing so as to introduce vertical effective display data into the data treating means and a clock control circuit for generating a pulse when both of the horizontal and vertical display data are effective. In one embodiment at least one of the horizontal and vertical home position regulating circuit comprises a counter for counting a reference signal, external input means for arbitrarily setting the timing with the display data, and a coincidence detecting circuit for detecting a

coincidence between the output of said counter and a set value of said external input means so that the display position is adjusted by said external input means. Additionally or alternatively at least one of the horizontal and vertical home position regulating circuit comprises delay time setting means for setting desired delay time, synchronizing means for synchronizing the output of the delay time setting means to clock signal, a counter for counting the clock signal according to the output of the synchronizing means, and initializing means for initializing the synchronizing means according to the output of the counter.

According to another aspect of the present invention there is provided an interface for either monochromatic or multicolor thin displays characterised by comprising: timing means for taking a timing so as to introduce effective display data into data treating means according to a synchronizing signal; data treating means for generating desired data for a thin display panel according to either monochromatic display data or multicolor display data; and timing signal generating means for generating timing signals necessary for operating driver means of the thin display panel.

The data treating means may comprise a data changing circuit for changing serial data of the display

data into parallel data and storing the data temporarily, a first switching circuit for giving monochromatic data to the driver means, a second switching circuit for giving multicolor data to the driver and a color selecting circuit for selecting one of the switching circuits.

In an embodiment, the data treating means comprises a color display data processing circuit unit including an S/P converter circuit for converting R, G and B color display serial data in parallel, color mixing and blending means for converting the output of said S/P converter circuit into mixed color data and a first group of switching circuits for switching said mixed color data, and a monochromatic display data processing circuit unit including a second group of switching circuits for switching the output of said S/P converter circuit of at least one of said R, G and B display data.

The data treating means may have display mode switching means for selectively switching ON and OFF the outputs of said color display data processing circuit unit and said monochromatic display data processing circuit unit.

The data treating means may have display data reversing means for reversing said color display data.

According to a further aspect of the present invention there is provided an interface for converting separate multicolor video signals into a display data signal and a timing signal for operating a multicolor thin display panel characterised by comprising: timing means for taking a timing so as to introduce effective display data into data treating means according to a synchronizing signal; data treating means for generating desired data for a thin display panel according to multicolor display data; and timing signal generating means for generating timing signals necessary for operating driver means of the thin display panel.

According to a yet further aspect of the present invention there is provided an interface for converting separate monochromatic video signals into a display data signal and a timing signal for operating a monochromatic thin display panel characterised by comprising timing means for taking a timing so as to introduce effective display data into data treating means according to a synchronizing signal; data treating means for generating desired data for a thin display panel according to monochromatic display data; and timing signal generating means for generating timing signals necessary for operating driver means of the thin display panel.

Preferably the data treating means has no RAMS.

The data treating means may comprise a data changing circuit for changing serial data of the display data into parallel data and storing the data temporarily, and a switching circuit for giving monochromatic or multicolor data to the driver means.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of one embodiment of an interface according to the present invention;

Figure 2 is a block diagram of a second embodiment of an interface according to the present invention applicable to both the monochromatic and multicolor displays;

Figure 3 is a block diagram of a third embodiment of an interface according to the present invention applicable to a color display;

Figure 4 is a block diagram of a fourth embodiment of an interface according to the present invention applicable to a monochromatic liquid crystal display;

Figure 5 is a circuit diagram of a fifth embodiment of an interface according to the present invention;

Figure 6 is a timing chart explaining the operation of the interface of Figure 5;

Figure 7 shows one embodiment of an electrode construction of a color liquid crystal display panel for use with an interface according to the present invention;

Figure 8(A) shows an embodiment of a system for the monochromatic display, and Figure 8(B) shows an embodiment of a system for the color display;

Figure 9 shows a sixth embodiment of an interface according to the present invention for a multicolor display;

Figure 10 is a timing chart explaining the operation of the interface of Figure 9;

Figure 11 is a circuit diagram showing a system of a color liquid crystal display with an interface according to the present invention;

Figure 12 is a circuit diagram showing a sixth embodiment of an interface according to the present invention having a parallel bit selecting function to switch parallel display data into 4-bit or 8-bit data;

Figure 13 is a timing chart explaining the operation of the interface of Figure 12;

Figure 14 is a circuit diagram showing a seventh embodiment of an interface according to the present invention which can handle the various color dot arrangements (e.g. stripe, mosaic, inverse mosaic or

triangle arrangements) of a color panel;

Figure 15 shows various arrangement types of the color dots;

Figure 16 shows one embodiment of a color arrangement selecting circuit of an interface according to the present invention;

Figure 17 is a block diagram of an eighth embodiment of an interface according to the present invention for a multicolor flat type display;

Figure 18 is a block diagram of a ninth embodiment of an interface according to the present invention where difficulty in connection is eliminated by separating an X-axis driver into two systems for upper and lower electrodes;

Figure 19 is a timing chart explaining the operation of the interface of Figure 18;

Figure 20 shows the construction of a color graphic liquid crystal display using an interface according to the present embodiment;

Figure 21 is a block diagram showing a tenth embodiment of an interface according to the present invention for a color liquid crystal display;

Figure 22 is a block diagram of an eleventh embodiment of an interface according to the present invention for monochromatic display.

Figure 23 is a block diagram of a twelfth embodiment of an interface according to the present invention which can be admitted even at a low transfer speed by transferring data on a 8-bit parallel signal;

Figure 24 is a timing chart explaining the operation of the interface of Figure 23;

Figure 25 is a block diagram showing a system of a liquid crystal display according to a further embodiment of the present invention;

Figure 26 is a diagram showing electrode construction of a liquid crystal panel using an interface according to the present embodiment;

Figure 27 is a block diagram of a thirteenth embodiment of an interface according to the present invention;

Figure 28 is a block diagram showing a fourteenth embodiment of an interface according to the present invention;

Figure 29 is a block diagram showing the horizontal and vertical home position regulating circuits of an interface according to the present invention;

Figure 30 is a block diagram of a fifteenth embodiment of an interface according to the present invention;

Figure 31 is a timing chart explaining the operation of the interface of Figure 30;

Figure 32 is a block diagram showing a sixteenth embodiment of an interface according to the present invention;

Figure 33 is a timing chart explaining the operation of the interface of Figure 32;

Figure 34 is a chart showing the timings of output signals of the interface of Figure 32;

Figure 35 is a block diagram of a seventeenth embodiment of an interface according to the present invention;

Figure 36 is a timing chart explaining the operation of the interface of Figure 35.

Figure 1 is a block diagram of an interface according to the present invention. In Fig. 1, reference letters Hsyc denote a horizontal synchronizing signal; letters CK a dot clock signal; letters Vsyc a vertical synchronizing signal; letters DATA a display data signal. A horizontal home position regulating circuit 101 is used to regulate a stand-by time for regulating a blanking period continuing from the instant of reception of the horizontal synchronizing signal till reception of effective display data thereby to shift the horizontal home position to a left end. A

vertical home position regulating circuit 102 is used to regulate a stand-by position for regulating a blanking period continuing from the instant of reception of the vertical synchronizing signal till reception of the effective display data thereby to shift the vertical home position to the highest one. Reference numeral 103 denotes a clock control circuit for regulating generation of a clock signal to allow a clock for generating a timing signal for change and display of the display data after the horizontal and vertical blanking periods thereby to control the number of effective display data per one line. Numeral 105

denotes a data treating circuit which is constructed of: a data changing circuit for either changing the serial data of the display data signal, Data, into a parallel signal or rearranging color display data of red, green and blue colors into mixed color display data of three primaries; a data regulating circuit that functions to regularly change the order of the color display data (i.e., red, green and blue color data) for each horizontal scanning into a mosaic pattern or a stripe pattern and to effect positive and negative displays; a monochromatic display data switching circuit for switching and outputting the output of the aforementioned data changing circuit in a time sharing manner; a switching circuit for switching the color display data in a time sharing manner; and a mono/multi color selecting circuit for selecting the switching circuits of mono/multi color display data and the display timing signals. Numeral 104 denotes a timing signal generator for outputting to a driver the timing signals such as a frame signal FRM, i.e., data for starting the scanning, a shift clock CP for shifting the display data or a latch signal LOAD for latching the display data shifted.

As has been described above, the mono/multi color display data are inputted to the data treating circuit

105 and changed and treated so that they may be received by a driver and are then outputted to and displayed in the driver together with the timing signal of the timing signal generator 104.

Fig. 2 is a block diagram showing the whole construction of one embodiment of an interface circuit applicable to both the mono and multi color displays. In Fig. 2, reference letters Hsyc denote the horizontal scanning signal; letters CK the dot clock signal; letters Vsyc the vertical scanning signal; and letters RD, GD and BD color video signals of red, green and blue colors.

A horizontal home position regulating circuit 201 is used to regulate a stand-by time for regulating a blanking period continuing from reception of the horizontal synchronizing signal Hsyc till reception of effective display data so that the horizontal home position may be shifted to the left end. A vertical home position regulating circuit 202 is used to regulate a blanking period continuing from reception of the vertical synchronizing signal Vsyc till reception of effective display data so that the vertical home position may be shifted to the highest position. Numeral 203 denotes an AND circuit for regulating generation of the clock signal to allow a clock for

generating timing signal for the data change and display in and after the horizontal and vertical blanking periods. Numeral 204 denotes a counter for dividing the frequency of the clock signal of the AND circuit 203 to monitor the number of the effective display data of one line and dot clock stopping means for counting the number of dot clocks to reset the horizontal home position regulating circuit 201. Numeral 205 denotes a data changing circuit for changing the serial data of the display data RD, GD and BD into parallel data or for rearranging the display data RD, GD and BD into mixed color display data. The data changing circuit 205 stores the data temporarily. Numeral 206 denotes a data regulating circuit which has functions to change the aforementioned display data RD, GD and BD into mosaic or stripe pattern for each horizontal scanning regularly in their order and to effect the positive and negative displays. Numeral 207 denotes a timing signal generator for outputting a timing signal such as the frame signal FRM, a control drive signal M, the shift clock CP or the latch signal LOAD to the driver so as to effect a liquid crystal display. Numerals 208 and 209 denote switching circuits for switching the output of the data changing circuit 205 in a time sharing manner. Especially the switching circuit 208 switches and outputs the color display data to the driver. The

switching circuit 209 switches the monochromatic display data. Numeral 210 denotes a mono/multi color selecting circuit for selecting the time sharing timing of the aforementioned switching circuits 208 and 209, the timing of the shift clock CP and the mono/multi color display data in dependence whether the liquid crystal display is for color or monochromatic display. The aforementioned switching circuit 208 or 209 is switch in a time sharing manner to output display data UD_1 to UD_8 for upper electrodes and display data LD_1 to LD_8 for lower electrodes to the driver.

Fig. 3 is a block diagram showing the construction of an interface which can be applied to the color display. Fig. 3 has a construction similar to the whole one of Fig. 2 excepting the mono/multi color selecting circuit 210 and the switching circuit 209. Moreover, the individual blocks have functions similar to those of Fig. 2, and the color video signals RD, GD and BD have their data changed by a data changing circuit 305 and subjected to a color mixing treatment and are switched in a time sharing manner by a switching circuit 308 to output the upper electrode display data UD_1 to UD_8 and the lower electrode display data UD_1 to UD_8 to the driver. Fig. 4 is a block diagram showing

the construction of an interface which can be applied to the monochromatic liquid crystal display. Fig. 4 has a construction similar to the color interface construction of Fig. 3 excepting a data control circuit 306. Moreover, the individual blocks have functions similar to those of Fig. 3, but a data changing circuit 405 has no means for mixing the colors of the display data. The display data inputted in series are changed into parallel data by the data changing circuit 405. In the case of a 4-bit output, the parallel data are then switched in a time sharing manner to output the display data UD_1 to UD_4 and UD_5 to UD_8 in parallel. In the case of an 8-bit output, on the other hand, the time sharing is not conducted, but the display data UD_1 to UD_8 are outputted in parallel. The timing signal generator 407 likewise generates timing signals for feeding the driver with the frame signal FRM, the control drive signal M, the shift clock CP and the latch signal LOAD necessary for the liquid crystal display to output them together with the display data to the driver so that the liquid crystal display may be effected by the driver.

The embodiment shown in FIG. 5 relates to an interface circuit which can select a display mode from monochromatic and multi colored displays.

Fig. 5 is a circuit diagram showing one embodiment of the present invention, and Fig. 6 is a timing chart for supplementarily explaining the operations of the circuit of Fig. 5.

In Fig. 5: reference letters Hsyc denote a horizontal synchronizing signal; letters Vsyc a vertical synchronizing signal; letters CK a dot clock signal; and letters RD, GD and BD the respective display data of red, green and blue colors. These signals Hsyc, Vsyc, CK, RD, GD and BD are equivalent to interface signals to be fed to a CRT display. Reference numeral 501 denotes an X-axis display position adjusting circuit for counting the number of the dot clocks CK to adjust the display position in the X-axis direction. Numeral 504 denotes a Y=axis display position adjusting circuit for counting the number of the horizontal synchronizing signals Hsyc to adjust the display position in the Y-axis direction. Numeral 503 denotes an AND circuit which is made receptive of both the outputs of the aforementioned X-axis and Y-axis display position adjusting circuits 501 and 504 and the dot clocks CK. Numeral 506 denotes a 1/8 frequency divider circuit for dividing the frequency of a clock signal

P_1, i.e., the output of the aforementioned AND circuit 503 into one eighth. Numeral 507 denotes a frequency divider circuit for further dividing the frequency of the output P_2 of the 1/8 frequency divider circuit 506 to generate a reset signal P_3 for resetting the aforementioned X-axis display position adjusting circuit 501. Numerals 510, 511 and 512 denote shift register circuits for shifting the display data of red, green and blue colors. Numerals 513, 514 and 515 denote latch circuits for temporarily latching the display data of the shift registers 510, 511 and 512. Numerals 541 to 546 denote switching circuits for switching the display data of the latch circuits 513 to 515 in a time sharing manner to output the display data to the X-electrode driver circuit (which will be shortly referred to as the "X driver") of the liquid crystal display. Numeral 528 denotes a shift register for switching the aforementioned switching circuits 541 to 546 in a time sharing manner.

Numerals 554, 555 and 556 denote Exclusive OR gates for inverting the display data of red, green and blue colors when a switch SW_1 is in ON state.

Reference numerals 524 and 525 denote D-type flip-flop circuits (which will also be shortly referred to as the "D-type F/F circuit") which is made receptive of the aforementioned clock signal P_2 to generate a latch signal P_4. Numeral 521 denotes a set-reset flip-flop

circuit for setting operations in response to the generation of the aforementioned latch signal P_4. Numerals 516 and 517 denote a D-type flip-flop circuit and a NOR circuit for generating a set pulse signal P_9 when the output T_2 of the aforementioned Y-axis display position adjusting circuit 504 rises to an "H" level. Numeral 518 denotes a flip-flop circuit for generating a set output in response to the aforementioned set pulse signal P_9. Numerals 547 and 548 denote D-type flip-flop circuits for delaying the output of the aforementioned flip-flop circuit 518. The output FRM of the aforementioned D-type flip-flop circuit 548 is a frame signal. Numeral 520 denotes a flip-flop circuit for dividing the frequency of the aforementioned frame signal into one half. The output of the flip-flop circuit 520 is an alternate drive signal M for alternately driving a liquid crystal. On the other hand, reference letters LK denote a latch signal which is latched from display data transferred to the X-axis driver circuit by a latch circuit built in the X-axis driver circuit. Numeral 531 notes a 1/4 frequency divider circuit for dividing the frequency of a clock signal P_{10} into one quarter. Numeral 533 denotes a flip-flop circuit for dividing the frequency of the output P_{13} of the aforementioned frequency divider circuit 531 into one half. Numerals 539 and 540 denote

switching circuits for switching the display data of the aforementioned latch circuit 515. Numerals 535, 536 and 537 denote AND circuits and an OR circuit, which construct together a selecting gate circuit for selecting the shift clocks SK of a 4-bit parallel shift register built in the X-electrode driver circuit in the case of monochromatic or color display.

Next, the operations of one embodiment of the present invention will be described in the following.

The X-axis display position adjusting circuit 501 starts to count the number of the dot clocks CK when it receives the horizontal synchronizing signal Hsyc. When this counted value coincides with the set value of the blanking period of the display data, the output T_1 of the aforementioned X-axis display position adjusting circuit 501 rises to the "H" level. The setting of this blanking period can be adjusted at a unit of one dot by external setting means such as a digital switch. The Y-axis display position adjusting circuit 504 starts to count the number of the horizontal synchronizing signals Hsyc when it receives the vertical synchronizing signal Vsyc. When this counted value coincides with the set value of the blanking period of the display data in the Y-axis direction, the output T_2 of the aforementioned Y-axis display position adjusting circuit 504 rises to

the "H" level. The setting of this blanking period can be similarly adjusted at a unit of one dot by external setting means such as a digital switch. When both the outputs T_1 and T_2 of the aforementioned X-axis and Y-axis position adjusting circuits rise to the "H" level, a display start (or home position) is taken so that the clock signal P_1 is outputted from the AND circuit 503. The clock signal P_1 is inputted to the 1/8 frequency divider circuit 506 and the shift registers 510, 511 and 512. The display data RD, GD and BD are shifted for each clock by the shift registers 510, 511 and 512 so that the aforementioned clock signal P_1 may be the shift clock. The output P_2 of the 1/8 frequency divider circuit 506 causes the D-type flip-flop circuit 524 and the NOR circuit 525 to generate the latch signal P_4, each time eight clock signals P_1 are inputted, and to latch the parallel display data of the aforementioned shift registers 510, 511 and 512 in the latch circuits 513, 514 and 515 thereby to conduct the S/P conversions. The latch signal P_4 is inverted by an inverter 526 to set the flip-flop circuit 521 so that an AND circuit 522 starts to output the clock signal P_{10}. This clock signal P_{10} has its frequency divided by a 1/2 frequency divider circuit 527 and is inputted as the shift clock of the shift register 528. The shift register 528 uses

the output of a NOR circuit 529 as the shift data so that it operates as a quaternary ring counter to generate switching control signals P_5, P_6 and P_7. As a result, the switching circuits 541, 542 and 543, and 544, 545 and 546 are turned on in a time sharing manner to output display data (UD_0 to UD_3) and (LD_0 to LD_3) in parallel. The clock signal P_{10} has its frequency divided into one half by a flip-flop circuit 523 to output a clock signal P_8.

Furthermore, the aforementioned flip-flop 523 is reset by the signal which was inverted from the shift data of the shift register 528 by an inverter 530 so that it outputs three clocks of the clock signal P_8 in response to eight clocks of the clock signal P_{10} to generate the shift clocks SK through the AND circuit 536 and the OR circuit 537. The outputs of the latch circuits 515, 514 and 513 are inputted in the following manner to the switching circuits 541 to 546 to prepare the mixed R, G and B (i.e., red, green and blue) color display data. The switching circuits 541 to 546 are constructed of 4-bit parallel transmission gates and connected in the manner enumerated in the following table if their inputs are the 8th bits R_1, G_1 and B_1 to R_8, G_8 and B_8 from the 1st bits of the latch circuits 515, 514 and 513.

Names \ Bits	1st Bit	2nd Bit	3rd Bit	4th Bit
Switching Circuit 541	R_1	B_1	G_2	R_3
Switching Circuit 542	G_1	R_2	B_2	G_3
Switching Circuit 543	B_3	G_4	R_5	B_5
Switching Circuit 544	R_4	B_4	G_5	R_6
Switching Circuit 545	G_6	R_7	B_7	G_8
Switching Circuit 546	B_6	G_7	R_8	B_8

As described above, the switching circuits 541, 543 and 545, and 542, 544 and 546 are grouped into the upper display data UD_0 to UD_3 and the lower display data LD_0 to LD_3, and the color display data RD, GD and BD are inputted alternately and separately from the 1st bits. As a result, the display data UD_0 to UD_3 generate the outputs (R_1, B_1, G_2 and R_3) (B_3, G_4 - - - and so on) whereas the display data LD_0 to LD_3 generate the outputs (G_1, R_2, B_2 and G_3) and (R_3, B_4 - - - and so on).

Next, the timing signals to the liquid crystal display will be described in the following.

The output T_2 of the Y-axis display position adjusting circuit 504 is inverted by an inverter 505, when it rises to the "H" level, so that the set pulse P_9 is generated by the D-type flip-flop circuit 516 and the NOR circuit 517 to set the flip-flop circuit 518.

Then, the number of the clock signals P_2 the aforementioned 1/8 frequency divider circuit 506 is counted (up to 700, for example) by the frequency divider circuit 507 until the display data in the X-axis direction are inputted. After this, the reset signal P_3 is generated by a D-type flip-flop circuit 509 and a NOR circuit 508 to reset the X-axis display position adjusting circuit 501, the 1/8 frequency divider circuit 506, the frequency divider circuit 507 and the flip-flop circuit 518. This reset signal p_3 is used as both a latch signal LK for a latch circuit built in the aforementioned X-electrode driver circuit (i.e., the X driver) and a shift clock YSCL for a shift register built in the Y-electrode driver circuit (i.e., the Y driver). The output of the aforementioned flip-flop circuit 518 is delayed by the D-type flip-flop circuits 547 and 548 to output a frame signal FRM or data for starting the scanning of the Y-electrode driver circuit (i.e., the Y driver). The aforementioned frame signal FRM has its frequency divided by the 1/2 frequency divider circuit 520 to generate the AC drive signal M, which is outputted to the X-electrode and Y-electrode driver circuits, to reverse the polarity of the drive voltage.

The description thus far made is directed to the case of the color display. Next, the case of the monochromatic display will be described in the following.

The clock signal P_{10} is inputted to the 1/4 frequency divider circuit 531 to output the 1/4 divided frequency output P_{13}, which further has its frequency divided into one half by the 1/2 frequency divider circuit 533 to output the switching control signals P_{14} and P_{15} of the switching circuits 539 and 540. The reversed output of the divided frequency output P_{13} of the aforementioned 1/4 frequency divider circuit 531 is fed through the AND circuit 535 and the OR circuit 537 to output the monochromatic shift clocks SK of the aforementioned X-electrode driver circuit (i.e., the X driver). Exclusive OR circuits 547, 548 and 549 are polarity switching circuits for reversing or restoring the polarity of the aforementioned display data RD, GD and BD so that the polarity of these data RD, GD and BD can be reversed, when a switch SW_1 is turned on, and otherwise restored to switch the displays NEGA/Posi. On the other hand, a switch SW_2 is used to select the color and monochromatic dipslays. When this switch SW_2 is turned off, the reversed output of the output P_{13} of the aforementioned 1/4 frequency divider circuit 531 is fed through the selecting gate circuit 535 and the OR circuit 537 to generate the shift clocks SK for the monochromatic display and at the same time to activate the outputs of the aforementioned switching circuits 539

and 540 thereby to raise the outputs of the switching circuits 541 to 546 to high impedances. When the switch SW_2 is turned on, on the contrary, the clock signal P_8 of the aforementioned flip-flop circuit 523 is fed through the AND circuit 536 and the OR circuit 537 to generate the shift clocks SK for the color display and at the same time to activate the outputs of the switching circuits 541 to 546 thereby to switch the outputs of the switching circuits 539 and 540 to high impedances.

As has been described hereinbefore, the display modes can be switched between the color and monochromatic displays in accordance with the voltage level of a selecting terminal S_2. The displays NEGA/Posi can also be selected by setting the voltage level of a selecting terminal S_1.

Fig. 6(A) is a timing chart showing the outputs T_1 and T_2 of the X-axis and Y-axis display position adjusting circuits. Fig. 6(B) shows the timing of the clock signals P_1 and P_3; Fig. 6(C) shows the timing of the switching control signals P_5, P_6 and P_7 and the display data UD_0 to UD_3 and LD_0 to LD_3; Fig. 6(D) shows the timing of the monochromatic display data LD_0 to LD_3; and Fig. 6(E) shows the timing the shift clocks CK, the latch clocks LK, the frame signal FRM and the AC drive signal M, i.e., the timing signals

to be fed to the driver circuits of the liquid crystal display.

Fig. 7 shows one embodiment of the electrode construction of a color liquid crystal panel in the case of the color display according to the present invention. The color array order of the electrodes should not be limited to that of the present invention. Fig. 8 shows system constructions of the embodiment of the present invention. Fig. 8(A) shows an example of the system construction for the monochromatic display, and Fig. 8(B) shows an example of the system construction for the color display. In view of Fig. 8, the present invention could be understood more deeply.

As has been described hereinbefore, according to the present invention, conversions into the display data and timing signals of the liquid crystal display can be made on real time by using the interface signals of the CRT display. There can be attained the following outstanding effects. (1) Since no frame buffer memory is required, the small-sized inexpensive liquid crystal display terminal can be manufactured by integrating the gate array. (2) The interface circuit for the color display nonexisting in the prior art can be provided to increase the attraction of the liquid

crystal display. (3) The display modes can be selected between the monochromatic and color displays by the single interface circuit. (4) Since the same driver circuit as that of the prior art can be used, it is unnecessary to develop the driver circuit especially for the color display.

Moreover, the present invention is especially effective for a new liquid crystal panel of strong dielectricity making use of the storability of an element even for the blanking period, such as an active matrix having built therein a non-linear resistance element, e.g., MSI or MIM, an active matrix or a TFT panel having a switching transistor built therein, a smectic liquid crystal panel.

FIG. 9 shows an embodiment of an interface circuit according to the invention which can be applied to a thin display capable of conducting the color display by making use the interface signal of the color CRT.

Fig. 10 is a timing chart for supplementing the explanation of the operations of the circuit of Fig. 9.

In Fig. 9: reference letters Hsyc denote a horizontal synchronizing signal; letters Vsyc a vertical synchronizing signal; letters CK dot clock signals; and letters RD, GD and BD display data in red, green and blue colors, respectively.

These signals Hsyc, Vsyc, CK, RD, GD and BD are similar to interface signals to the CRT display. Reference numeral 901 denotes an X-axis display position adjusting circuit for counting the number of the dot clocks CK to adjust the display region (or position) in the X-axis direction. Numeral 907 denotes a Y-axis display position adjusting circuit for counting the number of the horizontal synchronizing signals Hsyc to adjust the display region (or position) in the Y-axis direction. Numerals 904 and 905 denote 1/8 and 1/80 counter circuits for counting effective dot clocks ϕ_2.

Numerals 911, 912 and 913 denote S/P converter circuits for converting the serial display data RD, GD and BD in the red, green and blue colors into parallel display data. Numerals 914, 915 and 916 denote latch circuits for temporarily storing the parallel display data outputs of the aforementioned S/P converter circuits 911, 912 and 913. Numerals 917 to 922 denote switching circuits for switching the parallel display data of the aforementioned latch circuits 914 to 916 in a time sharing manner to output parallel display data UD_1 to UD_4 and LD_1 to LD_4 to liquid crystal driver circuits. Numeral 923 denotes a 4-bit shift register circuit for switching the aforementioned switching circuits 917 to 922 in a time sharing manner. Letters SK denote a shift clock signal for shifting the parallel display data UD_1 to UD_4 and LD_1 to LD_4 of the shift register circuit built in the X-axis driver circuit. Letters LK denote a latch signal for latching the parallel display data UD_1 to UD_4 and LD_1 to LD_4 in the latch circuits built in the X-axis driver circuit. Letters FRM denote scanning start data for starting the scan in the Y-axis direction. Letter M denotes an alternating drive signal for driving the color liquid crystal panel by flowing an AC current.

Next, the operations of the present invention

will be described in the following. When the horizontal synchronizing signal Hsyc is inputted to the X-axis display position adjusting circuit 901, the output X_T of this circuit 901 is reset at "L" to rise to "H" after a lapse of a predetermined time, as shown in the timing chart (A) in Fig. 10. This time width LW1 can change the display start position in the X-axis display direction by arbitrarily adjusting the counted value of the dot clocks CK of the built-in variable counter. Moreover, the horizontal synchronizing signal Hsyc sets an R-S flip-flop 906 so that the output T_1 of this flip-flop 906 rises to the value "H". As a result, the output ϕ_1 of an AND circuit 902 generates the dot clocks for the X-axis effective display period at the timing shown in Fig. 10(A). The Y-axis display position adjusting circuit 907 is also made to have a similar construction and has its output Y_T reset at the value "L", when it receives the vertical synchronizing signal Vsyc, and caused to rise to the value "H" after a lapse of predetermined time period, as shown in the timing chart (B) in Fig. 10. This time width LW2 can adjust the display start position in the Y-axis direction by arbitrarily adjusting the counted value of the horizontal synchronizing signals Hsyc of the built-in variable counter. Moreover, the vertical synchronizing signal

Vsyc sets an R-S flip-flop 909 so that the output T_2 of this flip-flop 909 takes the value "H". As a result, an AND circuit 908 outputs the horizontal synchronizing signals Hsyc of the Y-axis effective display period at the timing shown in Fig. 10(B). While the output T_2 of the R-S flip-flop 909 is at the value "H", the AND circuit 903 generates the dot clocks ϕ_2 of the effective display period. These dot clocks ϕ_2 are inputted as the shift clocks of the S/P converter circuits 911, 912 and 913 constructed of 8-bit shift registers. As a result, the serial data of the display data RD, GD and BD for the effective display periods of the red, green and blue colors are converted into parallel data and are outputted to the latch circuits 914, 915 and 916. The aforementioned dot clocks ϕ_2 of the effective display period have their frequency divided by a factor of eight by the 1/8 counter to generate a carry signal ϕ_3. This carry signal ϕ_3 is a latch signal for the aforementioned latch circuits 914, 915 and 916. The carry signal ϕ_3 is also inputted to the 1/80 counter 905 so that it is divided by a factor of eighty to generate a carry signal ϕ_4 thereby to reset the aforementioned R-S flip-flop 906. As a result, the output T_1 of this flip-flop 906 is reset at the value "L" to interrupt the generation of the dot clocks ϕ_1.

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During the aforementioned effective display period, the outputs of the latch circuits 14, 15 and 16 are inputted to the switching circuits 17 to 22. These switching circuits 17 to 22 are constructed into a 4-bit parallel transmission gate. If the input of this transmission gate falls at the eighth bit of R_1, G_1 and B_1 to R_8, G_8 and B_8 from the 1st bit of the latch circuits 14, 15 and 16, the input signals of the switching circuits 17 to 22 are rearranged in the following table:

	1st bit	2nd bit	3rd bit	4th bit
Switching Circuit 17	R_1	B_1	G_2	R_3
Switching Circuit 19	B_3	G_4	R_5	B_5
Switching Circuit 21	G_6	R_7	B_7	G_8
Switching Circuit 18	G_1	R_2	B_2	G_3
Switching Circuit 20	R_4	B_4	G_5	R_6
Switching Circuit 22	B_6	G_7	R_8	B_8

As seen from the above table, the switching circuits are grouped into the circuits 17, 19 and 21 and the circuits 18, 20 and 22, and the display data RD, GD and BD are inputted alternately and separately from

the 1st bit. The switching signals of the aforementioned switching circuits q17 to q22 are generated by the 4-bit shift register q23. A 1/4 counter q24 quarters the clock ϕ_{10}, which is prepared by dividing the frequency of the dot clock ϕ_2 into halves by a 1/2 counter q31, to generate a carry signal ϕ_8, as shown in Fig. 10(C). This carry signal ϕ_8 is inputted to the shift register q23 to generate outputs Q_1 to Q_4. These outputs Q_1 to Q_4 generate the output "H" in a time sharing manner, but the outputs Q_2 to Q_4 are utilized as the switching signals of the switching circuits q17 to q22. The output Q_1 is reserved as an output data pause period. As a result, the switching circuits q17 to q22 are switched in a time sharing manner, i.e., q17 and q18, q19 and q20, and q21 and q22 to simultaneously output the parallel display data UD_1 to UD_4 and LD_1 to LD_4. The output SK of an AND circuit q27 between the inverted output of the output Q_1 of the shift register q23 and the shift clock ϕ_7 of the shift register q23 outputs the 4-bit parallel data UD_1 to UD_4 and LD_1 to LD_4 as the shift clocks of the (4-bit parallel) shift registers built in the X-axis electrode driver circuit. The timing chart in Fig. 10(D) shows the timing of interface signals to the X-axis and Y-axis electrode driver circuits. The shift clocks SK are inputted to a 1/480 counter q28

so that the carry signal LK having a 1/480 frequency becomes a latch signal for latching the output of the 4-bit parallel shift register built in the aforementioned X-axis electrode driver circuit. An R-S flip-flop circuit 929 is set by the signal Vsyc and reset by the latch signal LK to output the Y-axis electrode scanning start signal FRM having the timing shown in Fig. 10(D). A 1/2 counter 930 generates the signal having one half frequency of the aforementioned signal FRM to invert for each frame the polarity of the drive voltage to be applied to the liquid crystal.

Fig. 11 is a circuit diagram showing the system construction of the color liquid crystal display according to one embodiment of the present invention. Reference numeral 1160 denotes the aforementioned interface circuit; numeral 1150 a Y-axis electrode driver circuit; numeral 1140 an X-axis electrode driver circuit having the X-electrode of a color liquid crystal display panel 1144 led out upward; numeral 1149 an X-axis electrode driver circuit having the X-electrode led out downward. The X-axis electrode driver circuits 1140 and 1149 are constructed of 4-bit parallel shift registers 1141 and 1146, latch circuits 1142 and 1147, and liquid crystal driver units 1143 and 1148. The parallel display data UD_1 to UD_4 and LD_1 to LD_4 are inputted simultaneously to the

4-bit parallel shift registers 141 and 146, shifted by the shift clocks SK and latched by the latch clocks LK. The outputs thus latched by the latch circuits 142 and 147 conduct the drives in accordance with the display data corresponding to the filter electrodes colored by the liquid crystal drivers 143 and 145, respectively.

As has been described hereinbefore, according to the embodiment, the color displays of the liquid crystal or the else can be easily conducted in real time by using the interface signal of the CRT display but not the memory circuit such as the RAM. Thus, the present invention can provide an attractive display which can have its display information increased and be made light, thin and small so that it can be used as the flat display terminal. Since the IC of the driver circuit to be used can be similar to that of the monochromatic one of the prior art, another outstanding effect is that any driver circuit especially for the color display need not be developed.

Fig. 12 is a circuit diagram showing one embodiment of an interface circuit having a parallel bit selecting function to switch parallel display data into 4-bit or

8-bit data. Fig. 13 is a timing chart for supplementing the description of the operations of Fig. 12.

The circuit shown in Fig. 12 has a construction similar to that of Fig. 5 excepting a portion, and the common components conduct similar operations. Reference numerals 1210, 1211 and 1212 denote S/P changing circuits which are individually composed of shift registers for shifting red, green and blue display data and latch circuits for temporarily latching the outputs of the shift registers.

Numeral 1221 denotes a set/reset flip-flop circuit for setting in response to the aforementioned first pulse signal P_2. Numerals 1257 and 1258 denote switching circuits for the display data of the upper and lower drivers, respectively, for outputting the display data in 4-bit parallel in a time sharing manner. Numerals 1260 and 1259 denote switching circuits for the display data of the upper and lower drivers, respectively, for outputting the display data in 8-bit parallel in a time sharing manner. Reference letters SW_2 denotes a selecting switch for selecting whether the aforementioned 4-bit or 8-bit parallel output is to be outputted to the driver.

The first output P_2 of a 1/8 divider 1206 sets the flip-flop circuit 1221. As a result, an AND circuit

1222 starts the output of a clock signal P_{10}.

When the selecting switch SW_2 is OFF, the gate is ON by the switching circuit 1251. As a result, the frequency is divided by a flip-flop circuit 1227 of the 1/2 divider and is inputted as the clock of a quaternary ring counter 1228. This quaternary ring counter 1228 uses the output of a NOR circuit 1229 as its data. The quaternary ring counter 1228 generates switching control signals P_5, P_6 and P_7 in a time sharing manner and switches on the switching circuits 1257, 1259 and 1260 in a time sharing manner to output the display data UD_1 to UD_4, LD_1 to LD_4, UD_5 to UD_8 and LD_5 to LD_8 in parallel. Moreover, the clock signal P_{10} has its frequency divided into two halves by a flip-flop circuit 1223 so that a shift clock signal SK of the parallel data is outputted. The flip-flop circuit 1223 is reset by the signal, which is reversed data from the quaternary ring counter 1228 by an inverter 1230, to output three clocks of the shift clock signal SK of the parallel data in response to the input of eight clocks of the clock signal P_{10}. The output P_2 of the 1/8 divider 1206 is gated on by a switching circuit 1253 into the latch signals of latch circuits built in the S/P changing circuits 1210, 1211 and 1212 to latch the shifted data every eight shots of the clock signal P_1.

The outputs of the aforementioned S/P changing circuits 1210, 1211 and 1212 are inputted alternately bit by bit into the switching circuits 1257 and 1258 so that they may be the mixed color display data of R, G and B (i.e., red, green and blue colors). The switching circuit 1257 outputs the upper display data UD_1 to UD_4 grouped, and the switching circuit 1258 outputs the lower display data LD_1 to LD_4 grouped.

The color display data RD, GD and BD are inputted alternately from the individual first bits to the switching circuits 1257 and 1258. As a result, the display data are outputted in a time sharing manner in response to the outputs P_5, P_6 and P_7 of the aforementioned quaternary ring counter 1228 so that the switching circuit 1257 generates the outputs of (R_1, B_1, G_2 and R_3) and (B_3, G_4, ---, and so on) --- and so on. On the other hand, the switching circuit 1258 generates the outputs (G_1, R_2, B_2 and G_3) and (R_4, B_4 ---, and so on) to the display data LD_1 to LD_4 at the same timing as that of the switching circuit 1257. (Note: the numeral indicates what bit the data falls at.)

In the system described above, the display data are transferred in the 4-bit parallel to the upper driver and the lower driver.

Next, the following description is directed to the

case in which the switch SW_2 is ON. In the 8-bit parallel output mode at this time, the switching circuits 1259 and 1260 are selected and activated to output the upper display data UD_1 to UD_8 and the lower display data LD_1 to LD_8 in a time sharing manner. The output P_2 of the 1/8 divider 1206 has its frequency divided into two halves by a flip-flop circuit 1252 and is inputted as a latch signal via the switching circuits 1253 to the S/P changing circuits 1210, 1211 and 1212. As a result, these S/P changing circuits 1210, 1211 and 1212 latch the display data of 16 bits. On the other hand, the output P_{10} of the AND circuit 1222 has its frequency divided into two halves by the flip-flop circuit 1250 and further similarly divided through the switching circuit 1251 by the flip-flop circuit 1227 to operate the quaternary ring counter 1228 so that the shift clock SK of the display data is outputted from the flip-flop circuit 1223. The switching circuits 1259 and 1260 receive the 16-bit display data of the aforementioned S/P changing circuits 1210, 1211 and 1212 alternately for each one bit. The switching circuit 1260 outputs the upper display data UD_1 to UD_8 grouped, and the switching circuit 1259 outputs the lower display data LD_1 to LD_8 grouped. The color display data RD, GD and BD of the S/P changing circuits

1210, 1211 and 1212 are likewise inputted to the switching circuits 1260 and 1259 alternately from the first bit. As a result, the display data are outputted in a time sharing manner by the outputs P_5, P_6 and P_7 of the aforementioned quaternary ring counter 1228 so that the switching circuit 1260 generates outputs (R_1, B_1, G_2, R_3, B_3, G_4, R_5 and B_5), (G_6, R_7, B_7, G_8, ---, and so on), ---, and so on. On the other hand, the switching circuit 1259 generates the outputs (G_1, R_2, B_2, B_3, R_4, B_4, G_5 and R_6), (B_6, G_7, R_8, ---, and so on), ---, and so on to the display data at the same timing as that of the circuit 1260. (Note: the numeral indicates what bit the data falls at.)

As has been described above, the 8-bit parallel mode can be selected by turning on the switch SW_2, and the 4-bit parallel mode can be selected by turning off the switch SW_2. The display data is inverted to effect an NEGA display by turning on a switch SW_1, and the Posi display can be effected by turning off the switch SW_1.

In the timing chart of Fig. 13, (A) shows the timing of the outputs T_1 and T_2 of the horizontal and vertical home position regulating circuits. (B) shows the timing of clock signals P_1 and P_3; (C) the timing of the timing signals to the drivers of the liquid

crystal display such as the switching signals P_5, P_6 and P_7 and the display data UD_0 to UD_3 and LD_0 to LD_3; and (D) the timing of the shift clock CP, the latch clock LK, the frame signal FRM and the control drive signal M.

As has been described hereinbefore, according to the present embodiment, the parallel display data bits can be easily selected to the 4-bit or 8-bit so that the 4-bit or 8-bit parallel driver can be selected within the allowable range of the transfer speed to enhance the applicability remarkably.

As a result, the 4-bit driver cannot be used in the prior art, but two of them can be used if they are in parallel to have an 8-bit construction. Since the driver having the same construction as that of the prior art can be used as it is, there is no necessity for developing a driver especially for color display.

Although the present invention has been described only to the change from the 4-bit to 8-bit, it can be applied to another change from the 8-bit to 16-bit but should not be limited thereto.

The present invention can naturally be applied to elements other than the liquid crystal ones.

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Fig. 14 is a circuit diagram showing one embodiment of the interface circuit which can handle the various color dot arrangements (e.g., stripe, mosaic, inverse mosaic or triangle arrangements) of a color panel.

The circuit shown in FIG. 14 has a construction similar to that of FIG. 5 excepting a portion, and the common components have similar operations.

Reference numeral 1450 denotes a color arrangement selecting circuit for causing the arrangements of the red, green and blue color dots to correspond to those of the color dots of the stripe (of Fig. 15(A)), the mosaic (Fig. 15(B)) and the inverse mosaic (Fig. 15(C)).

In Fig. 15 showing the arrangement types of the color dots: (A) shows the stripe type (e.g., the parallel array of R, G and B); (B) shows the mosaic type (e.g., downward to the right of R, G and B); (C) shows the inverse mosaic type (e.g., downward to the left of R, G and B).

Fig. 16 shows one embodiment of the color arrangement selecting circuit according to the present invention.

Reference numerals 1664, 1665 and 1666 denote switching circuits which are switched in the order of connection to output the display data RD, GD and BD to display data output terminals D_1, D_2 and D_3. Numerals 1651, 1652 and 1653 denote D-type flip-flops (i.e., D-type F/F circuits) and a NOR circuit for generating a ternary ring counter. Numerals 1655 to 1658 denote transmission gate circuits for changing the outputs of the D-type flip-flop circuits of the aforementioned ternary ring counter by a selecting terminal S_4. A selecting terminal S_3 is used in case the arrangement is fixed at the stripe type. The selecting terminal S_4 is used to select the mosaic type or the inverse mosaic type. Next, the operations of Fig. 16 will be described in the following.

In the case of the stripe type, i.e., in the case of the electrode construction of the color liquid crystal panel shown in Fig. 7 or 15(A), the selecting terminal S_3 is set at a voltage level "H". As a result, the D-type flip-flop circuits 1651 and 1652 of the ternary ring counter are reset. As a result, both the switching circuits 1665 and 1666 are turned off. The output of a NOR circuit 1654 takes an "L" level so that the switching circuit 1664 is turned on to output the display data RD, GD and BD to the

D_1, D_2 and D_3.

Next, the dot color arrangement of the mosaic type of Fig. 15(B) will be described in the following. The selecting terminal S_3 is set at the "L" level, and the selecting terminal S_4 is set at the "H" level. As a result, the ternary ring counter is reset by the vertical synchronizing signal Vsyc and then performs its ternary ring counting operation when it receives the horizontal synchronizing signal Hsyc as its clock input. Then, the transmission gates 1655 and 1657 are turned on. As a result, the switching circuits 1664, 1665 and 1666 are turned on consecutively and cyclically each time they receive the horizontal synchronizing signal Hsyc, so that the output terminals D_1, D_2 and D_3 have their order changed, as follows, for each one line display to output the display data:

BD, GD and BD - - - 1st Line;

BD, RD and GD - - - 2nd Line; and

GD, BD and RD - - - 3rd Line.

Next, let the case of the inverse mosaic type shown in Fig. 15(C) be considered in the following. Both the selecting terminals S_3 and S_4 are set at the "L" level. Then, the transmission gates 1656 and 1658 are turned on. As a result, the output terminals D_1, D_2 and D_3 output the display data for each line

display, as follows:

RD, GD and BD - - - 1st Line;

GD, BD and RD - - - 2nd Line; and

BD, RD and GD - - - 3rd Line.

These display data are inputted for S/P changing as the input data of the individual shift registers and are changed into parallel data, as has been described above. These parallel data are then switched in a time sharing manner by the grouped switching circuits and are driven by the X-axis drivers.

As has been described hereinbefore, according to the present embodiment, an optimum system can be selected at any time by the selecting terminals even for the panel having the various color dot arrays such as the stripe type, the mosaic type and the inverse mosaic type of the color display panel so that the present embodiment can be applied to side purposes.

Fig. 17 is a circuit diagram showing another embodiment of the interface for a color flat type display. In Fig. 17, a horizontal home position regulating circuit 1701 is made receptive of the horizontal synchronizing signal Hsyc and has a predetermined delay time for taking timing with the color display data. A vertical home position regulating

circuit 1702 is made receptive of the vertical synchronizing signal Vsyc and has a predetermined delay time from the timing of the signal Vsyc to take timing with the display data. A variable counter 1703 counts the number of the clock signals CK and accordingly the number of the horizontal dot clocks. A flip-flop circuit 1704 divides the frequency of the output clock signal CK of an AND circuit 1717. Switching circuits 1732 and 1733 are switching circuits for selecting the color video signals DR, DG and DB in a time sharing manner to transfer data to a latch circuit 1734 or 1735. A latch circuit 1736 further latches the video data, which are latched in a time sharing manner, to output them in parallel.

Next, the operations will be described in the following.

When the horizontal synchronizing signal Hsyc is inputted to a monostable multivibrator 1709 of the horizontal home position regulating circuit 1701, the output of the monostable multivibrator 1709 falls to the "O" level with a delay time which is determined by the time constant of a capacitor 1714 and a variable resistor 1715. Since a flip-flop circuit 1710 is set by the signal Hsyc, the output of a NOR circuit 1712 rises to the "1" level. The vertical home position

regulating circuit 1702 also has a similar construction and outputs the "1" level to the AND circuit 1717 with a delay time after the vertical synchronizing signal Vsyc. As a result, after the outputs of the horizontal home position regulating circuit 1701 and the vertical home position regulating circuit 1702 coincide to the "1" level, the AND circuit 1717 outputs the clock signals CK. The number of these clock signals CK is counted by the variable counter 1703.

In case the counted value of the variable counter 1703 is set at 640, a carry signal CL_1 is generated in response to the 640th clock signal CK. Since the carry signal CL_1 sets the output of the flip-flop circuit 1710 at the "1" level, the AND circuit 1717 interrupts the output of the clock signals CK. On the other hand, the red, green and blue video signals DR, DG and DB are inputted to D-type flip-flop circuits 1729, 1730 and 1731 and are outputted with a delay of the half period of the aforementioned dot clock signals CK. The outputs of the flip-flop circuits 1729, 1730 and 1731 are inputted to the switching circuits 1732 and 1733 and are selectively switched until they are latched by the latch circuit 1734 or 1735. The control signals of these switching circuits 1732 and 1733 are switched alternately in response

to each input of the clock signals by the output of the flip-flop circuit 1704 which is made receptive of the clock signals CK of the AND circuit 1717. The latch signals of the aforementioned latch circuits 1734 and 1735 are generated by AND circuits 1726 and 1725. The output CL_2 of the AND circuit 1725 is delayed by the delay circuit 1727 and is inputted as the latch pulse of the latch circuit 1736. The latch circuit 1736 latches the video signals of the aforementioned latch circuits 1734 and 1735 simultaneously to output the video signals R_1, G_1, B_1, R_2, G_2 and B_2 simultaneously to the driver of the color liquid crystal display.

Moreover, the output CL_2 of the AND circuit 1725 is delayed by a delay circuit 1728 constructed of the D-type flip-flop and is outputted as a shift clock signal SC for the video signals R_1 to B_2 of the liquid crystal display driver.

The carry signal CL_1 of the aforementioned variable counter 1703 is delayed by a delay circuit 1706 constructed of the D-type flip-flop circuit to generate the output LD as the data latch signal for one line to the liquid crystal driver.

When the vertical synchronizing signal Vsyc is inputted, this signal acting as the data for starting

the drive of the first scanning line is inputted to a NOR circuit 1722 so that the output of a NOR circuit 1721 is set at "1". And, the latch signal LD of the aforementioned liquid crystal driver is delayed a half period of the clock signal CK by a delay circuit 1707 constructed of the D-type flip-flop circuit and is inputted to the NOR circuit 1721 so that it resets the output of the NOR circuit 1721 at "0". The output signal FRM of this NOR circuit 1721 is outputted as the data (i.e, the frame signal) for starting the scanning at the common side of the liquid crystal driver to the liquid crystal driver. Moreover, the output FRM of the aforementioned NOR circuit 1721 has its frequency divided by a flip-flop circuit 1711 to invert the polarity of the liquid crystal drive voltage for each frame thereby to output the drive control signal M for the control drive.

According to the present invention, it is possible to construct a novel color interface circuit which can have its circuitry simplified at a low cost by the use of the interface signal of a CRT display and which is compatible with the CRT display.

Figs. 18 to 20 show another example in which the difficulty in connection is to be eliminated by separating an X-axis driver into two systems

for upper and lower electrodes. A D-type flip-flop (which will be shortly referred to as a "D-type FF") 1806 and a NOR circuit 1812 are circuits for generating a data hold signal HP for holding the data to a segment driver. A D-type FF circuit 1801, a NOR circuit 1813 and an FF circuit 1814 are circuits for generating the frame signal FRM. An FF circuit 1815 is a circuit for generating a drive signal polarity inversion control signal DF for alternately driving a liquid crystal. An FF circuit 1807 is a circuit for dividing the frequency of an effective horizontal dot signal ϕ_2. A D-type FF circuits 1808 and a NOR circuit 1810 are circuits for generating a shift clock USK for transferring data UST to the shift register of the upper segment driver. A D-type FF circuit 1809 and a NOR circuit 1811 are circuits for generating a shift clock LSK for transferring data LST to the shift register of the lower segment driver. A D-type FF circuit 1923 and a NOR circuit 1824 are circuits for generating a set signal ϕ_5 to the set/reset circuits of FF circuits 1825 and 1826. Delay circuits 1927 and 1828 are circuits for delaying the aforementioned data shift clocks USK and LSK to generate a reset signal to the FF circuits 1925 and 1826. Transmission gates 1816 and 1819, 1817 and 1820, and 1818 and 1821

are switching circuits for sharing the red, green and blue video signals between the red, green and blue UR, UG and UB of the upper segment driver and the red, green and blue LR, LG and LB of the lower segment driver. The present embodiment has the components recited above.

Next, the operations of Fig. 18 will be described in the following. Fig. 19 is a timing chart of Fig. 18. In Fig. 18, a vertical home position regulating circuit 1802 is a circuit for setting the effective display period in the Y-axis direction and has built therein a counter circuit for counting the vertical flyback period after it receives the vertical synchronizing signal Vsyc and a counter circuit for counting the number of the horizontal synchronizing signals for the effective display region period. The horizontal synchronizing signal Hsyc is inputted as the clock input to the vertical home position regulating circuit 1802. The output T_1 of this vertical home position regulating circuit 1802 is an output signal at the "H" level for the period of the effective display region in the Y-axis direction, as shown in Fig. 19. As a result, the output ϕ_1 of an AND circuit 1803 inputs the horizontal synchronizing signal Hsyc for the period of the effective display period in

the Y-axis direction to a horizontal home position regulating circuit 1804. This horizontal home position regulating circuit 1804 has the same construction as that of the vertical home position regulating circuit 1802 and has built therein a counter circuit for counting the horizontal flyback period after it receives the horizontal synchronizing signal Hsyc and a counter circuit for counting the number of the dot clocks CK. These dot clocks CK are inputted as the clock input. The output T_2 of the horizontal home position regulating circuit 1804 is an output signal at the "H" level for the period of the effective display region in the X-axis direction, as shown in Fig. 19. As a result, an AND circuit 1805 outputs the dot clock signal ϕ_2 in the effective display region. The red, green and blue video signals RD, GD and BD are shared selectively between upper video signals UR, UG and UB and lower video signal data LR, LG and LB by switch circuits, which are constructed of transmission gates 1816 and 1819, 1817 and 1820, and 1818 and 1821, and are outputted to the upper and lower segment drivers. The selected controls of the aforementioned transmission gates 1816 to 1821 are shared by an output signal ϕ_6 which has its frequency divided into one half by the dot clock signal ϕ_2.

The D-type FF circuit 1808 and the NOR circuit 1810 generate a shift clock USR, which is to be used as the shift clock of the shift register built in the upper segment driver, in response to the fall of the Q output of the FF circuit 1807. In response to the fall of the $\overline{Q}$ output of the D-type FF circuit 1807, a shift clock LSK is generated to provide a shift clock for the shift register built in the lower segment driver.

A D-type FF circuit 1823 and a NOR circuit 1824 generate a set pulse ϕ_5 for setting the shift data in response to the fall of ϕ_1 to set FF circuits 1825 and 1826 at the "H" level. Since these FF circuits 1825 and 1826 are reset by the first shots of the shift clock USK of the upper segment driver and the shift clock LSK of the lower segment driver, the outputs LSK and LST of the aforementioned FF circuits 1825 and 1826 provide the data of the shift registers of the upper and lower segment drivers. The D-type FF circuit 1801 and the NOR circuit 1813 generate a set pulse signal ϕ_3 at the fall of the output T_1 of the aforementioned horizontal home position regulating circuit 1802 to set the FF circuit 1814. The D-type FF circuit 1806 and the NOR circuit 1812 generate the data hold pulse HP at the fall of the aforementioned

horizontal home position regulating circuit T_2 to hold the data of the upper and lower segment drivers. Moreover, the data is also delayed by a delay circuit 1830 and is applied as the reset signal of the FF circuit 1814 to reset the FF circuit 1814. Therefore, the output FRM of the FF circuit 1814 provides the scan starting data for the shift registers of the common driver as the frame signal for starting the scanning. The FF circuit 1815 divides the frequency of the aforementioned FRM signal to input the polarity inversion signal DF for inverting the polarity of the drive voltage to the upper and lower segment drivers and the common driver for each frame thereby to switch the polarity.

Fig. 20 shows the whole construction of a color graphic liquid crystal display using the interface of the present embodiment. In Fig. 20: reference 2042 denotes an upper segment driver; numeral 2043 a lower segment driver; numeral 2041 a common driver; and numeral 2060 a color liquid crystal display panel. The upper and lower segment drivers 1042 and 2043 are constructed of shift registers 2044 and 2052, switching circuits 2045, 2046, 2050 and 2051, waveform polarity converting circuits 2048 and 2053, and data hold circuits 2047 and 2049. The horizontal

electrodes R_1, G_1 and B_1 to R_4, G_4 and B_4 of the color liquid crystal panel 2060 are connected with the upper and lower segment drivers and are driven vertically. The shift data UST and LST of the shift registers 2044 and 2052 are shifted by the shift clocks USK and LSK. The outputs Q_1 to Q_4 of the shift registers 2044 and 2052 are controlled sequentially by the switching circuits 2045 and 2050 to sample and hold the data. After this, in response to the data hold signal HP, the data hold circuit 2047 holds the analog voltage of one horizontal scanning line to drive the S electrodes R_1, G_1 and B_1 to R_4, G_4 and B_4. The common driver 2041 is fed with the frame signal FRM as the frame starting data to conduct the linear sequential scannings in response to the aforementioned hold panel signal HP. The waveform polarity converting circuits 2048 and 2053 controls to convert the polarity of the analog voltage in accordance with the polarity of the polarity converting signal DF to effect the control drive.

According to the present embodiment, the color video signals are shared and transferred to the upper and lower sides so that the pitch interval between the color panel X-axis electrodes and the driver can be enlarged to facilitate the connection therebetween.

Moreover, the transfer clock frequency of the data can be reduced to one half so that the IC price can be dropped. Still moreover, the driver is laid out at the upper and lower sides so that the pattern design and mounting of the periphery of the driver can be facilitated.

Fig. 21 is a block diagram showing a further embodiment of the interface for the color liquid crystal display. In Fig. 21, shift registers 2112, 2113 and 2114 are circuits for shifting the output signals of latch circuits 2109, 2110 and 2111 for each one bit in response to shift clock signals ϕ_4, ϕ_5 and ϕ_6. AND circuits 2115, 2116 and 2117 are selecting gate circuits for selectively extracting the output signals of the aforementioned shift registers 2112, 2113 and 2114. A shift register 2119 is a circuit for shifting the output signals of the aforementioned selecting gate circuits. A latch circuit 2120 is a circuit for temporarily storing the output of the aforementioned shift register 2119 to output the mixed color display data in parallel. A frame signal generator 2123 is a circuit for generating a frame signal. A shift clock generator 2124 is a circuit for generating shift clocks for sequentially transferring the mixed color display data inputted to an

X-axis driver 2127. A latch clock generator 2125 is a circuit for generating a latch signal for latching the data inputted to the X-axis driver 2127 and a Y-axis driver 2129. A control signal generator 2126 is a circuit for switching the polarity of the drive signals of the X-axis driver 2127 and the Y-axis driver 2129 so as to drive a color liquid crystal panel 2128 in a controlled manner. The color liquid crystal panel 2128 is a panel having red, green and blue filters attached to its transparent electrodes. The X-axis driver 2127 and the Y-axis driver 2129 are circuits for driving the X-electrodes and Y-electrodes of the color liquid crystal panel 2128, respectively. A frequency multiplier 2130 is a circuit which uses a PLL circuit for oscillating at a frequency three times as high as that of the clock signal ϕ_2.

Next, the operation of the present embodiment will be described in the following.

The latch signal ϕ_1 is a carry signal which is prepared by dividing the aforementioned clock signal ϕ_2 by the 1/8 divider 2105. The output signals of the latch circuits 2109, 2110 and 2111 are the signals ϕ_3 which are inverted from the latch signal ϕ_1 by the inverter 2121, and are transferred in parallel to the shift registers 2112, 2113 and 2114. The

individual color display data transferred to the aforementioned shift registers 2112, 2113 and 2114 are shifted for each one bit in response to the shift clocks ϕ_4, ϕ_5 and ϕ_6 and are inputted to the AND circuits 2115, 2116 and 2117, respectively. A ring counter 2122 is made receptive of the output of the frequency multiplier 2130, which uses the PLL circuit oscillating with a frequency three times as high as that of the aforementioned clock signal ϕ_2, to output the clock signals ϕ_4, ϕ_5 and ϕ_6 in time series to provide the shift clock signals for the aforementioned shift registers 2112, 2113 and 2114.

As a result, the OR circuit 2118 outputs the color display data of the red, green, blue, red, - - -, and so on sequentially and selectively from the shift registers 2112, 2113 and 2114. The output signal of the aforementioned OR circuit 2118 is inputted to the shift register 2119 and is shifted and stored for each one clock signal because the clock signal ϕ_2 is used as the shift clock signal. The latch circuit 2120 latches the output signal of the aforementioned shift register 2119 in parallel in response to the aforementioned latch signal ϕ_1 to output the mixed color display data to the X-axis driver 2127. The shift clock generator 2124 generates

the shift clock signal by the counter, which is operative to divide the frequency of the clock signal ϕ_6 into 1/8, because the color display data of the aforementioned latch circuit 2120 is shifted to the 8-bit mixed color display data parallel to the shift register of the X-axis driver 2127. The latch clock generator 125 is constructed of a counter for dividing the frequency of the carry signal of the aforementioned shift clock generator 124 into 1/80 and outputs the latch signal to the latch circuit built in the X-axis driver 2127 when the mixed color display data shifted to the shift register of the X-axis driver 2127 takes 640 x 3 dots. On the other hand, the frame signal generator 2123 feeds the frame signal to the shift register of the Y-axis driver 2129 when it receives the vertical synchronizing signal Vsyc. That frame signal generator 2123 is constructed of a one-shot multivibrator, and its frame signal is a data signal for the Y-axis driver 2129. Moreover, the latch signal of the aforementioned latch clock generator 2125 is inputted as the shift clock signal of the data to the Y-axis driver 2127 to shift the data. The X-axis driver 2127 and the Y-axis driver 2129 have built therein the drivers for driving the X- and Y-electrodes of the color liquid crystal panel

2128 so that they generate selection signals, when the data are at "1", and non-selection signals, when the data are at "0", for their driving operations.

Fig. 23 is a circuit diagram showing a further embodiment of the interface which can be admitted even at a low transfer speed by transferring data on a 8-bit parallel signal, and Fig. 24 is a timing chart for supplementarily explaining the operations of the circuit of Fig. 23.

In Fig. 23: reference numeral 2310 denotes a variable counter for setting the counted value of the output ϕ_5 of an AND circuit 2308 at 200 or 400; numerals 2317 and 2318 buffers for classifying the 8-bit output data of a latch circuit 2314 into odd and even bits to amplify the display data UD_1 to UD_4 and LD_1 to LD_4 in the upper and lower extraction electrode drivers of the X-electrodes of the liquid crystal display; and letters shift clock signals for shifting the parallel display data UD_1 to UD_4 and LD_1 to LD_4 to the 4-bit parallel shift register circuits built in the X-axis driver. Letters LK denote a latch signal for latching the parallel display data UD_1 to UD_4 and LD_1 to LD_4 in the latch circuit built in the X-axis driver. Letters FRM denote scanning starting data for starting the scanning of the Y-axis

FIG. 22 shows an embodiment of an interface for monochromatic display. In FIG. 22, a 4-bit shift register 2205 is a circuit for converting a video signal VD coming in series into a parallel signal. A quartering counter 2204 is a circuit for generating a latch circuit for latching the display data of said 4-bit shift register 2205. A video signal VD is inputted to the 4-bit shift register 2205 for shiftclocking the output of the AND circuit 2217. As a result, the data is shifted and fetched each time a clock signal is inputted. On the other hand, the quartering counter 2204 is a frequency divider circuit made receptive of the clock signals of the AND circuit 2217 for generating a carry signal CL_2 in response to the fourth clock signal. This carry signal CL_2 latches the data of the aforementioned 4-bit shift register 2205. The 4-bit video data D_0 to D_3 thus latched are outputted from the 4-bit shift register 2205. The carry signal CL_2 of the aforementioned quartering counter 2204 is delayed by a D-type flip-flop circuit 2208 and is outputted as a shift clock signal SC for a data shift register of a liquid crystal driver circuit. The circuit shown in FIG. 22 has a construction similar to that of FIG. 17 except a portion.

Fig. 23 is a circuit diagram showing a further embodiment of the interface which can be admitted even at a low transfer speed by transferring data on a 8-bit parallel signal, and Fig. 24 is a timing chart for supplementarily explaining the operations of the circuit of Fig. 23.

In Fig. 23: reference numeral 2310 denotes a variable counter for setting the counted value of the output ϕ_5 of an AND circuit 2308 at 200 or 400; numerals 2317 and 2318 buffers for classifying the 8-bit output data of a latch circuit 2314 into odd and even bits to amplify the display data UD_1 to UD_4 and LD_1 to LD_4 in the upper and lower extraction electrode drivers of the X-electrodes of the liquid crystal display; and letters shift clock signals for shifting the parallel display data UD_1 to UD_4 and LD_1 to LD_4 to the 4-bit parallel shift register circuits built in the X-axis driver. Letters LK denote a latch signal for latching the parallel display data UD_1 to UD_4 and LD_1 to LD_4 in the latch circuit built in the X-axis driver. Letters FRM denote scanning starting data for starting the scanning of the Y-axis

electrodes of the liquid crystal display panel. Letter M denotes a control drive signal for driving the liquid crystal panel in a controlled manner.

Next, the operations of the embodiment of the present invention will be described in the following.

The horizontal synchronizing signal Hsyc sets an R-S flip-flop 2306 so that the output T_1 of this flip-flop takes the "H" level. As a result, the output ϕ_1 of an AND circuit 2302 generates dot clocks for an X-axis effective display period at the timing shown in Fig. 24(A). A vertical home position regulating circuit 2307 also has a similar construction and has its output Y_T reset at "L", as shown in Fig. 24(B), when the vertical synchronizing signal Vsyc is inputted, to rise to the "H" level after lapse of a predetermined time period. This period Lw_2 is enabled to regulate the display starting position in the Y-axis direction by arbitrarily regulating the value of the built-in variable counter.

Moreover, the vertical synchronizing signal Vsyc sets an R-S flip-flop 2309 so that the output T_2 of this flip-flop 2309 takes the "H" level. As a result, the AND circuit 2308 generates the output ϕ_5 of the Y-axis effective display period at the timing shown in Fig. 24(B). The variable counter

2310 outputs the carry signal ϕ_6 at the counted value 200, when a switch 2334 is ON, and at the counted value 400 when the switch is OFF. While the output T_2 of the R-S flip-flop 2309 is at the "H" level, an AND circuit 2303 generates the dot clock ϕ_2 of the effective display period. This dot clock ϕ_2 is inputted as the shift clock of an S/P changing circuit 2311 constructed of an 8-bit shift register.

As a result, the serial data of the display data D are changed to parallel data, which are outputted to the latch circuit 2314. The dot clock of the aforementioned effective display period has its frequency divided into 1/8 by the 1/8 counter to generate the carry signal ϕ_3. This carry signal ϕ_3 becomes the latch signal of the aforementioned latch circuit 2314. The carry signal ϕ_3 is further inputted to a 1/80 counter 2305 to have its frequency divided into 1/80 so that the carry signal ϕ_4 is generated to reset the aforementioned R-S flip-flop 2306. As a result, the output T_1 is reset at the "L" level to interrupt the generation of the dot clock ϕ_1.

For the aforementioned effective display period, the output of the latch circuit 2314 is fed to the X-axis driver from the buffers 2317 and 2318. The odd bit output of the latch circuit 2314 is inputted

to the buffer 2317 to output the display data UD_1 to UD_4, whereas the even bit output is inputted to the buffer 2318 to output the display data LD_1 to LD_4. The timing chart (D) of Fig. 24 shows the timing of the interface signals to the X-axis and Y-axis drivers.

The shift clock SK is inputted to a 1/80 counter 2328 so that the carry singal LK having its frequency divided into 1/80 becomes a latch signal for latching the output of the 4-bit parallel shift register built in the aforementioned X-axis driver. An R-S flip-flop 2329 is a circuit to be set by the signal Vsyc and reset by the latch signal LK to output the signal FRM for starting the scanning of the Y-axis electrodes at timing shown in Fig. 24(D).

A 1/2 divider 2330 generates the signal M, which is prepared by dividing the frequency of the aforementioned FRM signal into 1/2, to invert for each frame the polarity of the drive voltage to be impressed upon the liquid crystal.

Fig. 25 is a block diagram showing the system construction of the liquid crystal display according to a further embodiment of the present invention. X-axis drivers 2540 and 2545 are constructed of 4-bit parallel shift registers 2541 and 2546, latch

circuits 2542 and 2547, and liquid crystal drivers 2543 and 2548. The parallel display data UD_1 to UD_4 and LD_1 to LD_4 are inputted simultaneously to the 4-bit parallel shift registers 2541 and 2546, shifted in response to the shift clocks SK and latched by the latch circuits 2542 and 2547 in response to the latch clocks LK. The outputs thus latched by the latch circuits 2542 and 2547 effect the drives in accordance with the display data corresponding to the filter electrodes colored by the liquid crystal drivers 2548 and 2545, respectively.

Fig. 26 is a diagram showing the electrode construction of the liquid crystal panel using the present embodiment. In Fig. 26, the odd number X-axis electrodes X_1, X_3, X_5, - - -, and so on are used as the upper lead electrodes, and the even number electrodes X_2, X_4, - - -, and so on are used as the lower lead electrodes, and these upper and lower lead electrodes are driven by different X-axis drivers.

As has been described above, according to the present embodiment, the display data can be transferred in 8-bit parallel to the upper and lower electrodes so that the speed of the transfer shift clock signal can be retarded two times. Since, moreover, the pitch interval of the X-axis electrodes of the liquid crystal panel can be enlarged two times, the connection between the liquid crystal panel and the X-axis drive

output can be facilitated.

Fig. 27 is a circuit diagram showing one embodiment of the present invention. In Fig. 27, reference numeral 2701 denotes an X-axis display position adjusting circuit, and numeral 2702 denotes a Y-axis display position adjusting circuit. The X-axis display position adjusting circuit 2701 is constructed of external setting means 2721 such as a digital switch, a counter circuit 2722 for counting the number of clock signals CK, a group of exclusive OR circuits constructing together a coincidence detecting circuit; a group of NOR circuits 2724, a group of NAND circuits 2725, and a NOR circuit 2729. The Y-axis display position adjusting circuit 2702 is constructed, like the aforementioned X-axis display position adjusting circuit, of a counter circuit for counting the number of reference signals, external input means, and a coincidence detecting circuit for detecting a coincidence.

Next, the operations of Fig. 27 of the present invention will be described in the following. When a horizontal synchronizing signal Hsyc is inputted to the X-axis display position adjusting circuit 2701, a flip-flop circuit (or an F/F circuit) 2720 has its output set at an "H" level so that a clock signal CK is outputted from an AND circuit 2750 and

inputted to the counter circuit2722. The output of the counter circuit2722 and the output of the external setting means2721 are inputted to the grouped exclusive OR circuits2723, the outputs of which are outputted through the grouped NOR circuits2724 and the grouped NAND circuits2725 to the NOR circuit2729. As a result, the set value of the aforementioned external setting means2721 such as the digital switch and the counted value of the aforementioned counter circuit2722 coincide with each other, the output R_1 of the NOR circuit2729 rises to the "H" level to reset the aforementioned flip-flop circuit2720. As a result, the output Q of the flip-flop circuit 2720 is dropped to an "L" level. Since a flip-flop circuit2730 is reset, the output of a NOR circuit2731 takes the "H" level. Then, this "H" signal is inputted to the data input of a D-type flip-flop circuit2732 to output a signal T_1 from the output terminal Q to an AND circuit2703. On the other hand, the Y-axis display position adjusting circuit2702 has a construction similar to that of the X-axis display adjusting circuit2701 to count the number of the horizontal synchronizing signals Hsyc in response to the input of a vertical synchronizing signal Vsyc. When the counted value coincides with the

set value of the external input means, the counter circuit is reset in response to the coincidence detection signal to generate an output T_2 thereby to input the "H" signal to the AND circuit 2703. Just at this time, the display start (or the home position) is taken to output the shift clock SP and a clock signal P_2. This clock signal P_2 has its frequency divided into one eighth by a 1/8 frequency divider circuit2734 to generate latch pulses LP by a D-type flip-flop circuit2739 and a NOR circuit2740 so that the output of a shift register 3205 (which should be referred to in Fig.32) is latched in a latch circuit3209 (which should also be referred to in Fig.32) to execute the serial/parallel conversions of the display data. The output of the 1/8 frequency divider circuit2734 is further inputted to a frequency divider circuit2735 to count the number (e.g., 672) of effective display dots in the X-axis direction. In response to the output of the frequency divider circuit2735, reset pulses P_1 are generated by a D-type flip-flop circuit2736 and a NOR circuit2737 to reset the flip-flop circuit2730, the 1/8 frequency divider cirucit2734 and the frequency divider circuit2735. On the other hand, the shift clock SP is inputted as a shift clock to the

aforementioned shift register (which should also be referred to in Fig.32). Moreover, the shift clock SP has its frequency divided into one sixteenth by a 1/16 frequency divider circuit2742 to generate a set signal for a flip-flop circuit2745 by a D-type flip-flop circuit2741 and a NOR circuit 2743. When the flip-flop circuit2745 is set, an AND circuit2746 generates the clock signal P_5 to input it to a 1/4 frequency divider circuit2747. The output CP of this 1/4 frequency divider circuit2747 is turned as the shift clock signals of display data D_0 to D_3 (which should also be referred to in Fig.32) into the shift clock of a 4-bit parallel shift register built in a liquid crystal driver circuit IC.

The output of the 1/4 frequency divider circuit2747 further has its frequency divided by a flip-flop circuit2748 to generate switching signals GP_1 and GP_2 so that the 8-bit output of the aforementioned latch circuit3209(which should also be referred to in Fig.32) is switched for each 4 bits in parallel to output the 4-bit parallel display data D_0 to D_3. Fig.33 is a timing chart showing the timings of the individual parts of the circuit according to the embodiment of the present invention

shown in Fig.27. In Fig.33, the output Q_1 is set at the "H" level in response to the horizontal synchronizing signal Hsyc by the flip-flop circuit 2720 (which should be referred to in Fig.27) and is reset by the output R_1 of the NOR circuit 2729 of the coincidence detecting circuit so that the output Q of the D-type flip-flop circuit 2732 then generates the signal T_1. As a result, the clock signal P_2 can have its frequency divided by the frequency divider circuit 2735 to set and reset the flip-flip circuit 2730 and the frequency divider circuit 2735 in response to the reset signal P_1. As will also be understood, moreover, after the latch signal LP has been generated, the shift clock CP of the 4-bit parallel data and the switching signals GP_1 and GP_2 of the 4-bit parallel data D_0 to D_3 are generated.

Fig.32 is a diagram showing the overall construction of the interface of the present embodiment.

In Fig.32: the letters Hsyc denote the horizontal synchronizing signals; the letters Vsyc the vertical synchronizing signals; the letters CK the dot clock signals; and the letter D the display data. These signals Hsyc, Vsyc, CK and D are similar to the interface signals of the CRT display. Reference

numeral 3201 denotes an X-axis display position adjusting circuit for counting the number of the dot clock signals CK to adjusting the display start (or the home position) in the X-axis direction. Numeral 3202 denotes a Y-axis display position adjusting circuit for counting the number of the horizontal synchronizing signals Hsyc to adjust the display start (or the home position) in the Y-axis direction. Numeral 3203 denotes an AND circuit for generating the dot clocks CK when the outputs of the X-axis and Y-axis display position adjusting circuits coincide with each other. Numeral 3204 denotes means constructed of a frequency divider circuit or the like for counting the number of horizontal dots to reset the aforementioned X-axis display position adjusting circuit. Numeral 3205 denotes a shift register for shifting the serial data D. Numeral 3209 denotes a latch circuit for latching the output of the shift register 3205. Numeral 3206 denotes a frequency divider circuit for dividing the frequency of the shift clock SP to generate in the latch circuit 3209 the latch signal, the GP_1 and GP_2 for switching circuits 3207 and 3208, and the data shift clock CP. Numeral 3210 denotes a timing signal generator circuit for generating the interface signal for a

liquid crystal driver circuit such as a LOAD for latching the AC drive signal M, the frame starting signal FRM and the display data transferred to the driver. The numerals 3207 and 3208 denote switching circuits for alternately turning on and off every 4 bits of the 8th bits of the latch output of the latch circuit 3209 to output the display data in 4 bits.

Next, the operations of Fig. 32 will be described in the following.

When the horizontal synchronizing signal Hsyc is inputted to the X-axis display position adjusting circuit 3201, the number of the clock signals CK is counted by the counter circuit built therein. When the counted number coincides with the set count value, moreover, the X-axis display position adjusting circuit 3201 outputs the signal T_1. When the vertical synchronizing signal Vsyc is likewise inputted to the Y-axis display position adjusting circuit, the number of the horizontal synchronizing signals Hsyc is counted by the counter circuit built therein. When the counted number coincides with the set count value, moreover, the Y-axis display position adjusting circuit 3202 outputs the signal T_2.

Since the AND circuit 3203 has received the

aforementioned signals T_1 and T_2 and clocks CK, it generates the clock signal P_2 and the shift clock signal SP when both the signals T_1 and T_2 take the "H" level. The first clock signal when both the two signals T_1 and T_2 rise to the "H" level provides the display start (or the home position). When the clock signal P_2 is inputted to the frequency divider circuit 3204 so that the data of one line in the X-axis display direction are transferred, the reset signal P_1 is generated to reset the X-axis display position adjusting circuit 3201 to interrupt the input of the clock signal P_2.

On the other hand, the aforementioned shift clock signal SP is inputted as the shift clock of the shift register 3205 to shift the display data D. Moreover, the shift clock signal SP is inputted to the frequency divider circuit 3206 to generate the 1/8 frequency dividing signal so that the output of the aforementioned shift register 3205 is latched in the latch circuit 3209. The 8th bit data of the latch circuit 3209 are inputted at the unit of 4 bits to the switching circuit 3207 and the switching circuit 3208 to generate the parallel display data D_0 to D_3 of 4 bits which were switched by the switching signals GP_1 and GP_2 (i.e., the inverted signal of the signal

GP_1) of the aforementioned frequency divider circuit 3206. Moreover, this frequency divider circuit 3206 generates the shift clock signal CP so as to shift the aforementioned display data D_0 to D_3 to the shift register built in the driver. The timing signal generator circuit 3210 generates the driver latch signal LOAD, the frame signal FRM and the AC drive signal M to cause the liquid crystal driver circuit (or the driver) to generate those interface signals.

Incidentally, the embodiment thus far described is limited to the case in which the outputs of the display data are the 4 bits D_0 to D_3. The present invention should not be limited thereto but can be applied to the cases of 8 bits and 16 bits. Moreover, the reset means 3204 should not be limited to the frequency divider circuit but may reset the X-axis display position adjusting circuit 3201, when the data of one line in the X-axis direction are transferred, to interrupt the input of the signal P_2.

Fig. 34 is a chart showing the timings of the output signals of the overall construction of Fig. 32.

Incidentally, in the foregoing embodiment, the

display data D are subjected to the serial/parallel conversions to drop the transfer speed to the driver so as to divide the frequency of the shift clock CP into one quarter. However, the serial data themselves can be transferred to the driver.

The interface circuit of the present invention can be used in a variety of plane displays such as a liquid crystal panel (which should be referred to in Japanese Patent Laid-Open Nos. 94086/1986 and 174509/1986, for example) using a nonlinear resistive film such as silicon oxide or nitride film, a liquid crystal panel using a nonlinear element such as MIM or TFT, a smectic liquid crystal panel, a simple matrix TN plasma display, or an EL display. If the interface circuit is used in an unstorable display panel such as the simple matrix TN liquid crystal panel, the display element is not driven during the blanking period to reduce the substantial duty ratio, thus raising a problem that the contrast will drop. This problem is suitably eliminated in case the interface circuit is used in the storable display panel such as the aforementioned MSI, TFT and smectic liquid crystal panel.

FIG. 28 shows another embodiment of the invention.

In response to a 1/8 divider 2834 of Fig. 28, as has been described above, a latch signal LP is generated by a D-type flip-flop circuit 2839 and a NOR circuit 2840. On the other hand, the output of the 1/8 divider 34 has its frequency divided by a divider 2835. The first output P_6 of this divider 2835 is the 1/16 signal of the clock signal P_2. That divided signal P_6 is used to generate a set pulse P_4 by a D-type flip-flop 2845. As a result, an AND circuit 2846 generates the clock signal P_5. And, a 1/4 divider 2847 divides the frequency of the clock signal P_5 into 1/4 to generate the shift clock signal CP. As has been described above, the shift clock signal CP becomes the shift clock of the 4-bit parallel shift register, which is built in a liquid crystal driver IC, as the shift clock signal of the 4-bit display data D_0 to D_3. A flip-flop circuit 2848 divides the frequency of the shift clock signal CP to generate switching signals GP_1 and GP_2.

Fig. 29 is a circuit diagram showing a further embodiment of the horizontal and vertical home position regulating circuits. In Fig. 29, the horizontal home

position regulating circuit is constructed of: delay time setting means composed of a monostable multivibrator 2940 so as to determine the delay time by the time constant of a capacitor 2956 and a variable resistor 2957; synchronizing means using a D-type flip-flop 2944 for synchronization with the clock signal CK in response to the output of an AND circuit 2942; counting means using a variable counter 2946 enabled to count the number of the clock signal outputs of an AND circuit 2945 to set the counted number in a variable manner; and initializing means using a flip-flop circuit 2947 for initialization in response to the carry signal of the aforementioned variable counter. Likewise, the vertical home position regulating circuit is constructed of: delay time setting means using a monostable multivibrator 2948; synchronizing means using a D-type flip-flop 2952; counting means using a scanning number counter 2954 enabled to set the counted value in a variable manner; and initializing means using a D-type flip-flop for initialization with the carry output of the aforementioned scanning number counter.

Next, the operations of the horizontal home position regulating circuit will be described in the following. In response to the horizontal syn-

chronizing signal Hsyc, the flip-flop 2947 is reset so that the output Q_1 takes the "0" level. The output P of the monostable multivibrator is raised to the "1" level and fell to the "0" level after lapse of a predetermined time period. This holding time period of the "1" level is determined by the time constant C x R of the capacitor 2956 and the variable resistor 2957. As a result, after the predetermined time period, the output of a NOR circuit 2941 takes the "1" level and is inputted via the AND circuit 2942 to the D-type flip-flop 2944. As a result, the output Q_2 of the D-type flip-flop circuit 2944 is synchronized by the clock CK and outputted to the AND circuit 2945. As a result, the fine changes of the predetermined time period due to the fluctuations of the time constant CR and the voltage are always times to a constant value by that synchronizing means. The clock signal CK having passed through the AND circuit 2945 is inputted to the variable counter 2946. In the case of the display horizontal dot number 640, the carry signal is generated by the 640th clock signal CK, if the counted value is set at 640, and is inputted to the clock signal of the flip-flop circuit 2947. As a result, the output Q_1 of the flip-flop circuit 2947 takes the "1" level to

fell the output of the NOR circuit 2941 to the "0" level. As a result, the output Q_2 of the D-type flip-flop takes the "0" level so that the generation of the clock CK is interrupted by the AND circuit 2945. As described above, the predetermined time period can be made arbitrarily variable by using the output P of the monostable multivibrator 2940 so that the display position in the horizontal (or X-axis) direction can be easily regulated.

The vertical home position regulating circuit can likewise be regulated easily. If the vertical synchronizing signal Vsyc is inputted, a flip-flop circuit 2955 is reset so that the output Q_3 takes the "0" level. The output R of the monostable multivibrator is made to rise to the "1" level and is made to fall to the "0" level after lapse of a predetermined time period. The hold time of this "1" level can likewise be varied by adjusting a variable resistor 2959. After the predetermined time, the output of a NOR circuit 2949 takes the "1" level and is inputted through an AND circuit 2950 to a D-type flip-flop 2952. As a result, the output Q_4 of the D-type flip-flop circuit 2952 is synchronized with the horizontal synchronizing signal Hsyc and outputted to an AND circuit 2953. The horizontal synchronizing

signal Hsyc having passed through the AND circuit 2953 is inputted to the variable counter 2954. In case the number of the vertical scanning lines for the display is 400, the carry signal is generated in response to the 400th horizontal synchronizing signal Hsyc, if the counted value is set at 400, and is inputted to the clock signal of the flip-flop circuit 2955. As a result, the output Q_3 of the flip-flop circuit 55 takes the "1" level to drop the output of the NOR circuit 2949 to the "0" level. As a result, the output Q_4 of the D-type flip-flop takes the "0" level so that the generation of the horizontal synchronizing signal Hsync is interrupted by the AND circuit 2953. Like the horizontal home position regulating circuit, moreover, the display position in the vertical (or Y-axis) direction can be easily regulated by regulating the variable resistor 2948 of the monostable multivibrator 2948. And, the output H_{DC} of an AND circuit 2960 is a horizontal dot clock in the effective display area so that an image can be displayed in the liquid crystal display by making use of the clock H_{DC} and the display data.

Fig. 30 is a circuit diagram showing a further embodiment of the present invention. Fig. 31 is a timing chart of Fig. 30. Reference numeral 3013 denotes

a 1/8 a divider for dividing the frequency of the dot clock P_1 to feed a latch signal to a latch circuit 3008. Numeral 3018 denotes a 1/4 divider for generating a latch signal and then counting the number of the dot clocks P_1 to feed the shift clock CP to a 4-bit parallel shift register built in the driver. Numeral 3019 denotes a flip-flop circuit for dividing the frequency of the output of the 1/4 divider into 1/2. Numerals 3009 and 3010 denote switching circuits for switching the 8-bit parallel signal of the aforementioned latch circuit 3008 for every four bits to output the display data D_0 to D_3. A D-type flip-flop circuit 3012 and a NOR circuit 3014 are set pulse generators for generating the set signal P_2 when the output of the vertical home position regulating circuit 3002 takes the "H" level. A flip-flop circuit 3015 is a circuit for setting in response to the set signal P_2 and resetting in response to the reset signal R_1 to generate the frame data P_3. Numeral 3016 denotes a D-type flip-flop circuit for clocking the reset signal R_1 by using the frame data P_3 as its data. A flip-flop circuit 3017 divides the frequency of the output of the D-type flip-flop circuit 3016.

The present embodiment has the construction thus far described. Here, the output M of the flip-flop

circuit 3017 is a control signal for inverting the polarity of the waveform of the drive signal for each frame. The output FRM of the D-type flip-flop circuit 3016 is both a frame signal for starting to scan the first common electrode of the Y-axis driver. The LOAD signal is a latch circuit for latching the display data D_0 to D_3 in the built-in latch circuit, after those of the display data, which correspond to the X-axis electrodes, are shifted by the shift clock CP to the 4-bit parallel shift register built in the X-axis driver, and a shift clock of the shift register, which is built in the Y-axis driver, to scan a next Y-electrode. Next, the operations of the present embodiment will be described in the following.

A flip-flop circuit 3005 and a NOR circuit 3006 generate the reset signal R_1 and reset a horizontal home position regulating circuit 3001 to drop the output signal T_1 to the "L" level. The display data D are transferred to a shift register 3007 by using the dot clock P_1 as the shift clock input. In response to the latch signal having its frequency divided by the 1/8 divider 3013, the latch circuit 3008 converts the display data of the shift register 3007 to 8-bit parallel data. After the latch signal is outputted, the 1/4 divider 3018 divides the dot clock P_1 into

1/4 to output the shift clock CP for shifting the 4-bit parallel data D_0 to D_3 to the 4-bit parallel shift register built in the liquid crystal driver.

When the vertical home position regulating circuit 3002 generates the output signal T_2, the D-type flip-flop circuit 3012 and the NOR circuit 3014 generate the set pulse P_2 for setting the flip-flop circuit 3015.

This set signal P_2 sets the flip-flop circuit 3015 to raise the frame data signal P_3 to the "H" level. This frame data signal P_3 is fed as the data input of the D-type flip-flop circuit 3016. Next, when the aforementioned reset signal R_1 is generated, the flip-flop circuit 3015 is reset. Simultaneously with this, the D-type flip-flop circuit 3016 has its data shifted to raise the frame signal FRM to the "H" level. This frame signal FRM is dropped to the "L" level in response to the subsequent reset signal R_1. As a result, the aforementioned frame signal FRM has just the same pulse width as the period of the reset signal R_1 (i.e., the LOAD signal) and is fed as the data of the shift register built in the Y-axis driver. Moreover, absolutely the same reset signal (i.e., the LOAD signal) is inputted as the shift clock of that shift register so that the liquid

crystal can be driven by the scanning signals timed all over the common electrodes. Incidentally, the aforementioned vertical fly-back period can be arbitrarily set by the vertical home position regulating circuit 3002.

As has been described hereinbefore, according to the present embodiment, the frame signal is fed to the shift register of the Y-axis driver through the D-type flip-flop (or the shift register). As a result, the scanning time is common for the common electrodes from the first one to the last one. As a result, it is possible to solve the problem of the display quality of the prior art, in which the displays of the first and last common electrode lines are abnormally dense or thin, so that the displays cannot be misread by the observer.

FIG. 35 is a circuit diagram showing another embodiment of the invention. In FIG. 35, Hsyc inputted into a D-type flip-flop 3551 is synchronized by clock signal CK and outputted to a D-type flip-flop 3552. A NOR circuit 3555 generates a first pulse by the rise edge of Hsyc. The first pulse resets a D-type flip-flop 3557 of a horizontal home position regulating circuit 3501, so that a NOR circuit 3560 puts out clock CK. A counter 3561 counts up the clock CK. When counted value of the counter 3561 becomes equal to the setting value of an external setting means 3562, a coincidence circuit 3563 which comprises an exclusive OR and a NAND generates a coincidence signal. The signal reverses the output of the flip-flop 3557 and stops supply of the clock CK to the counter 3561. Therefore it is possible to regulate the horizontal blanking period. The vertical blanking period may be regulated by counting the pulse signal P15 of the first pulse generating means through a counter 3567 and using the output of a coincidence circuit 3569 similarly. The setting of the horizontal or vertical blanking period may be regulated by the dot in X or Y axis direction. When both of the outputs $\bar{Q}$ of the flip-flops 3557 and 3565 become "L", a display start (home position) is taken so that a NOR circuit 3559 generates clock signal P1. The clock P1 is inputted into a 1/8 divider 3506 and S/P changing circuits 3510, 3511 and 3512.

When the display data for 1 line are transferred, Hsyc fall down,Consequently, a second pulse generating means which comprises a D-type flip-flop 3553 and a NOR circuit

3554 generates pulse signal P16. The pulse P16 reverses the output Q of a flip-flop circuit 3558, so that the NOR circuit 3559 stops the generation of clock signal P1.

CLAIMS

1. An interface for converting separate video signals into a display data signal and a timing signal for operating a thin display panel characterised by comprising: timing means (101,102,103) for taking a timing so as to introduce effective display data into data treating means (105) according to a synchronizing signal (Hsyc); data treating means (105) for generating desired data for a thin display panel using said display data; and timing signal generating means (104) for generating timing signals necessary for operating driver means of the thin display panel.

2. An interface as claimed in claim 1 characterised in that the thin display panel has a X-Y dot matrix display electrode construction.

3. An interface as claimed in claim 2 characterised in that the X-electrode comprises an uneven-numbered electrode group and an even-numbered electrode group, each of the groups being led out from opposite sides of the panel to each other.

4. An interface as claimed in any preceding claim characterised in that the data treating means give 8 bits of desired data to the driver means.

5. An interface as claimed in any preceding claim

characterised in that the timing means comprise a horizontal home position regulating circuit (101) for controlling a timing so as to introduce horizontal effective display data into the data treating means (105), a vertical home position regulating circuit (102) for controlling a timing so as to introduce vertical effective display data into the data treating means and a clock control circuit (103) for generating a pulse when both of the horizontal and vertical display data are effective.

6. An interface as claimed in claim 5 characterised in that at least one of the horizontal and vertical home position regulating circuit (Figure 27) comprises a counter (2722) for counting a reference signal (CK) external input means (2721) for arbitrarily setting the timing with the display data, and a coincidence detecting circuit (2723-5) for detecting a coincidence between the output of said counter and a set value of said external input means so that the display position is adjusted by said external input means.

7. An interface as claimed in claim 5 or 6 characterised in that at least one of the horizontal and vertical home position regulating circuit (Figure 29) comprises delay time setting means (2940,2956-7) for setting desired delay time, synchronizing means (2944)

for synchronizing the output of the delay time setting means to clock signal (CK), a counter (2946) for counting the clock signal according to the output of the synchronizing means, and initializing means (2947) for initializing the synchronizing means according to the output of the counter (2946).

8. An interface for either monochromatic or multicolor thin displays characterised by comprising: timing means (101,102,103) for taking a timing so as to introduce effective display data into data treating means (105) according to a synchronizing signal (Hsyc); data treating means (105) for generating desired data for a thin display panel according to either monochromatic display data or multicolor display data; and timing signal generating means (104) for generating timing signals necessary for operating driver means of the thin display panel.

9. An interface as claimed in any preceding claim characterised in that the data treating means comprises a data changing circuit (205) for changing serial data of the display data into parallel data and storing the data temporarily, a first switching circuit (208) for giving monochromatic data to the driver means, a second switching circuit (209) for giving multicolor data to the driver and a color selecting circuit (210) for

selecting one of the switching circuits (208,209).

10. An interface as claimed in claim 8 or 9 characterised in that the data treating means (Figure 5) comprises a color display data processing circuit unit including an S/P converter circuit (510,511,512) for converting R, G and B color display serial data in parallel, color mixing and blending means (513,514,515) for converting the output of said S/P converter circuit into mixed color data and a first group of switching circuits (542-545) for switching said mixed color data, and a monochromatic display data processing circuit unit including a second group of switching circuits (539,540) for switching the output of said S/P converter circuit of at least one of said R, G and B display data.

11. An interface as claimed in claim 10 characterised in that the data treating means have display mode switching means (SW2) for selectively switching ON and OFF the outputs of said color display data processing circuit unit and said monochromatic display data processing circuit unit.

12. An interface as claimed in claim 10 or 11 characterised in that the data treating means have display data reversing means (SW1) for reversing said color display data.

13. An interface for converting separate multicolor

video signals into a display data signal and a timing signal for operating a multicolor thin display panel characterised by comprising: timing means (101,102,103) for taking a timing so as to introduce effective display data into data treating means (105) according to a synchronizing signal (Hsyc); data treating means (105) for generating desired data for a thin display panel according to multicolor display data; and timing signal generating means (104) for generating timing signals necessary for operating driver means of the thin display panel.

14. An interface as claimed in any of claims 8 to 13 characterised in that the thin display panel has a X-Y dot matrix display electrode construction, the X-electrode of which comprises an uneven-numbered electrode group and an even-numbered electrode group, each of the groups being led out from opposite sides of the panel to each other, and the data treating means generates separate desired data for the uneven-numbered electrode group and for the even-numbered electrode group.

15. An interface as claimed in claim 13 or 14 characterised in that the data treating means have a color arrangement selecting circuit for changing a color data according to the type of color dots arrangement of

the multicolor thin display panel.

16. An interface as claimed in any of claims 13 to 15 characterised in that the data treating means comprises first S/P converter circuits for converting, R, G and B color display serial data in parallel, shift registers for shifting the parallel R, G and B color display data, selecting gate circuits for selectively extracting the output of the shift registers and second S/P converter circuits for converting serial data of the selecting gate circuits in parallel.

17. An interface for converting separate monochromatic video signals into a display data signal and a timing signal for operating a monochromatic thin display panel characterised by comprising timing means (101,102,103) for taking a timing so as to introduce effective display data into data treating means (105) according to a synchronizing signal (Hsyc); data treating means (105) for generating desired data for a thin display panel according to monochromatic display data; and timing signal generating means (104) for generating timing signals necessary for operating driver means of the thin display panel.

18. An interface as claimed in any preceding claim characterised in that data treating means (105) has no RAMS.

19. An interface as claimed in any of claim 8 to 18 characterised in that the data treating means (Figure 2) comprises a data changing circuit (205) for changing serial data of the display data into parallel data and storing the data temporarily, and a switching circuit (210) for giving monochromatic or multicolor data to the driver means.

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FIG. 1

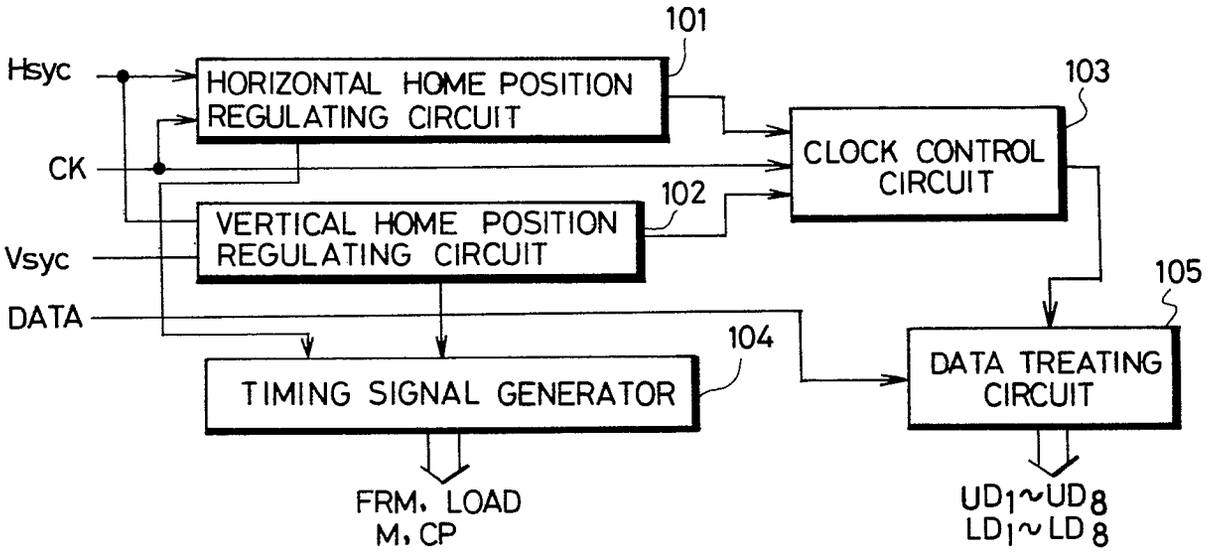


FIG. 2

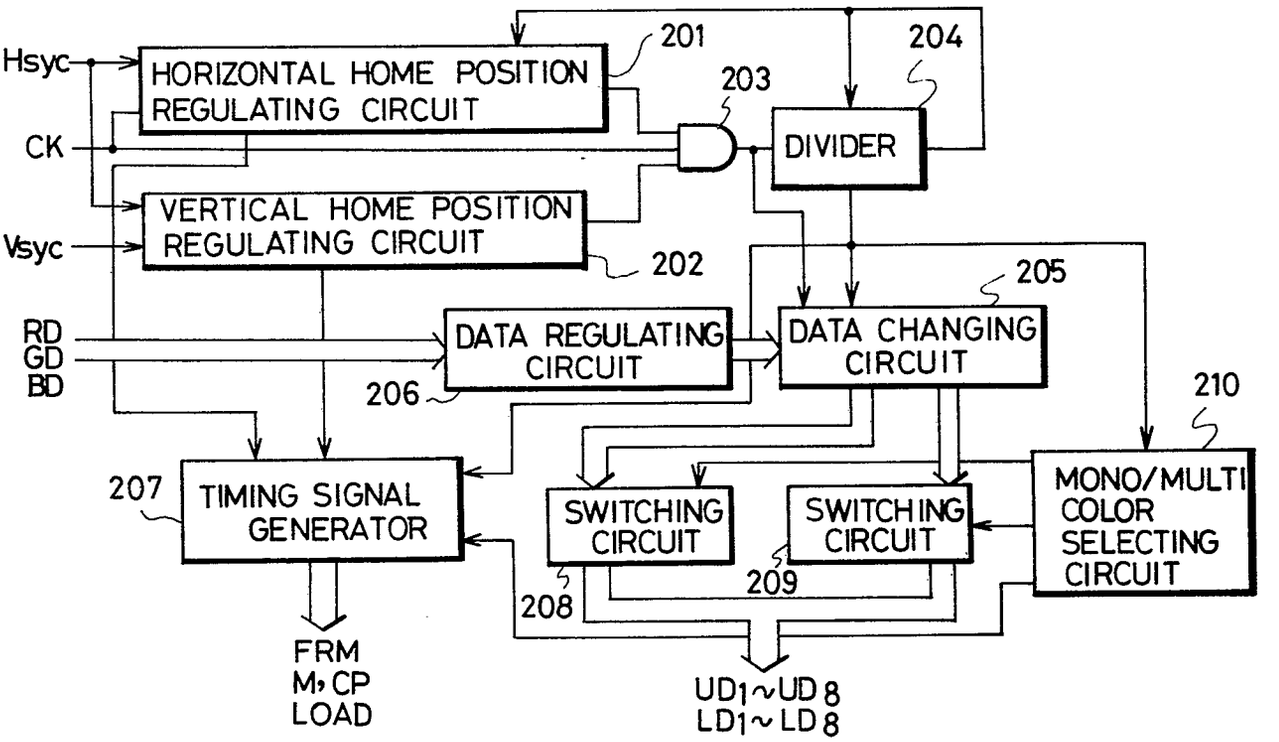


FIG. 3

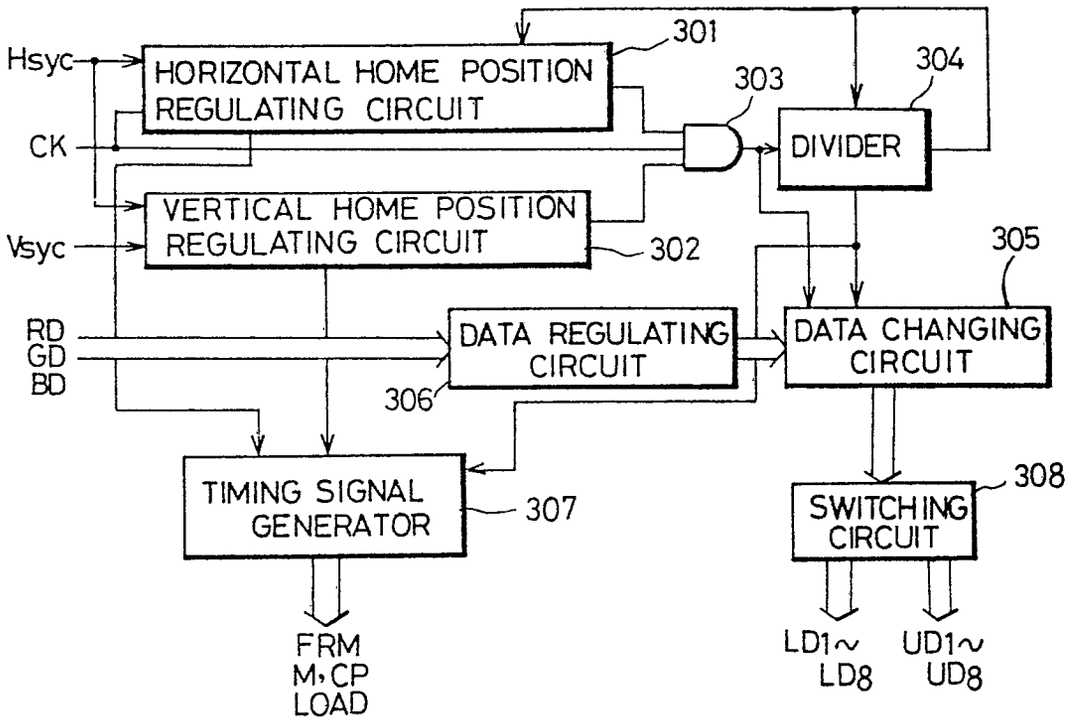
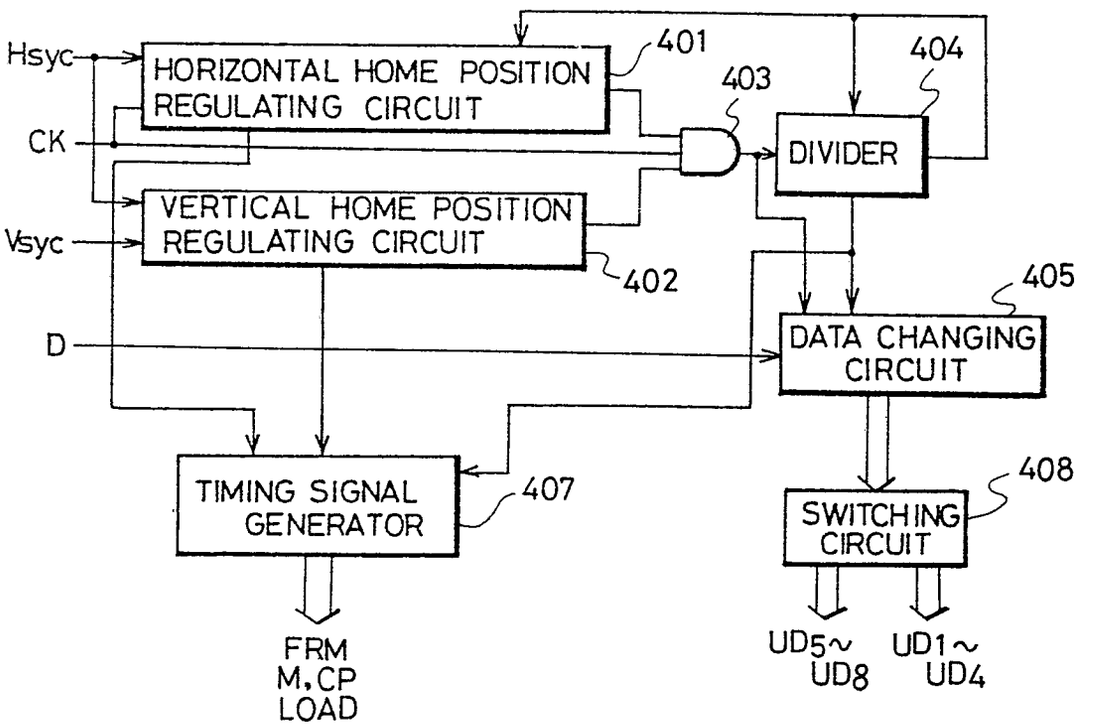

Hsyc
CK
Vsyc
RD
GD
BD
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME POSITION REGULATING CIRCUIT
DATA REGULATING CIRCUIT
DIVIDER
DATA CHANGING CIRCUIT
TIMING SIGNAL GENERATOR
SWITCHING CIRCUIT
301
302
303
304
305
306
307
308
FRM
M, CP
LOAD
LD1~
LD8
UD1~
UD8

FIG. 4


Hsyc
CK
Vsyc
D
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME POSITION REGULATING CIRCUIT
DIVIDER
DATA CHANGING CIRCUIT
TIMING SIGNAL GENERATOR
SWITCHING CIRCUIT
401
402
403
404
405
407
408
FRM
M, CP
LOAD
UD5~
UD8
UD1~
UD4

0 244 978

FIG. 5

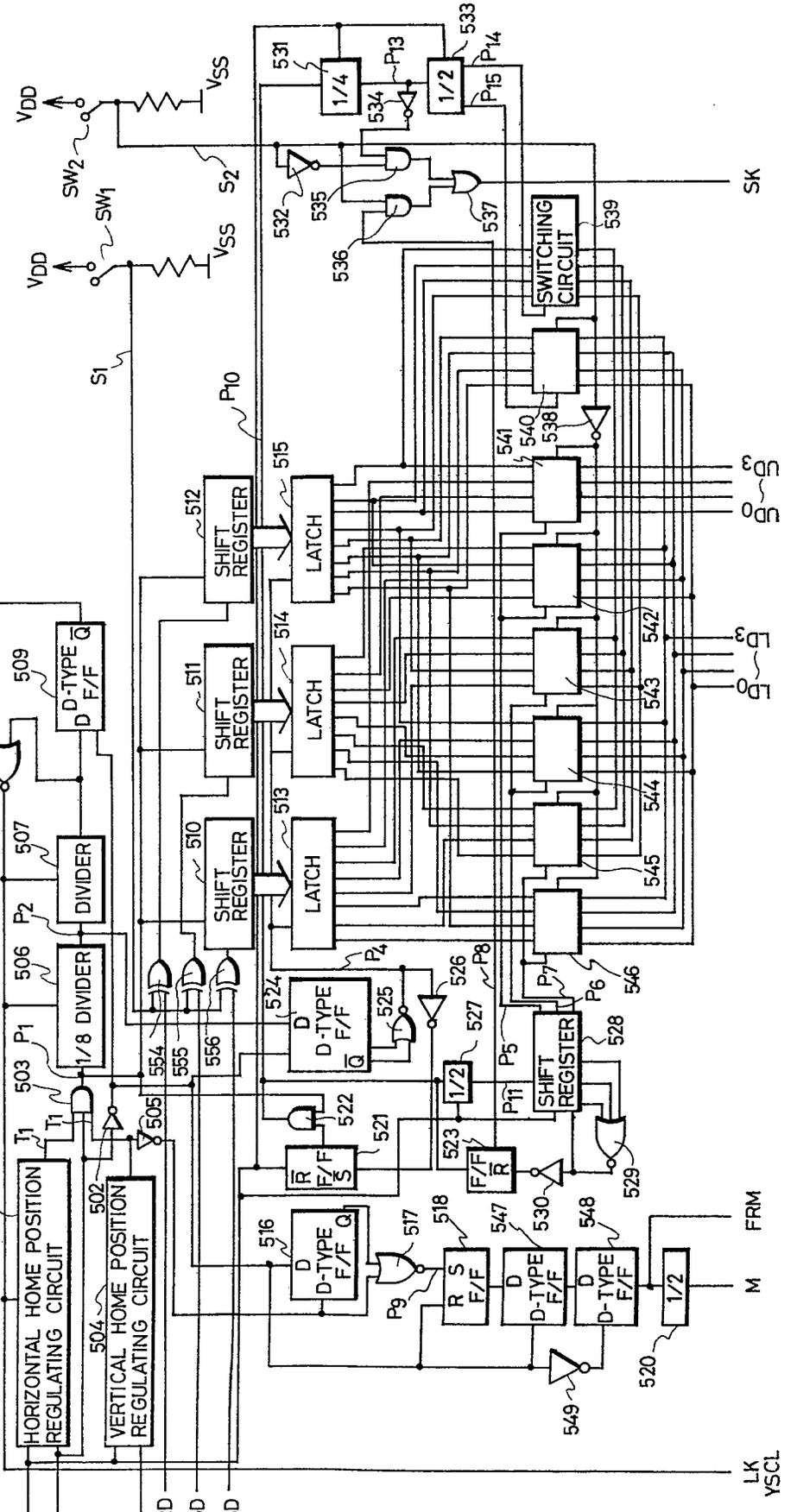


FIG. 6

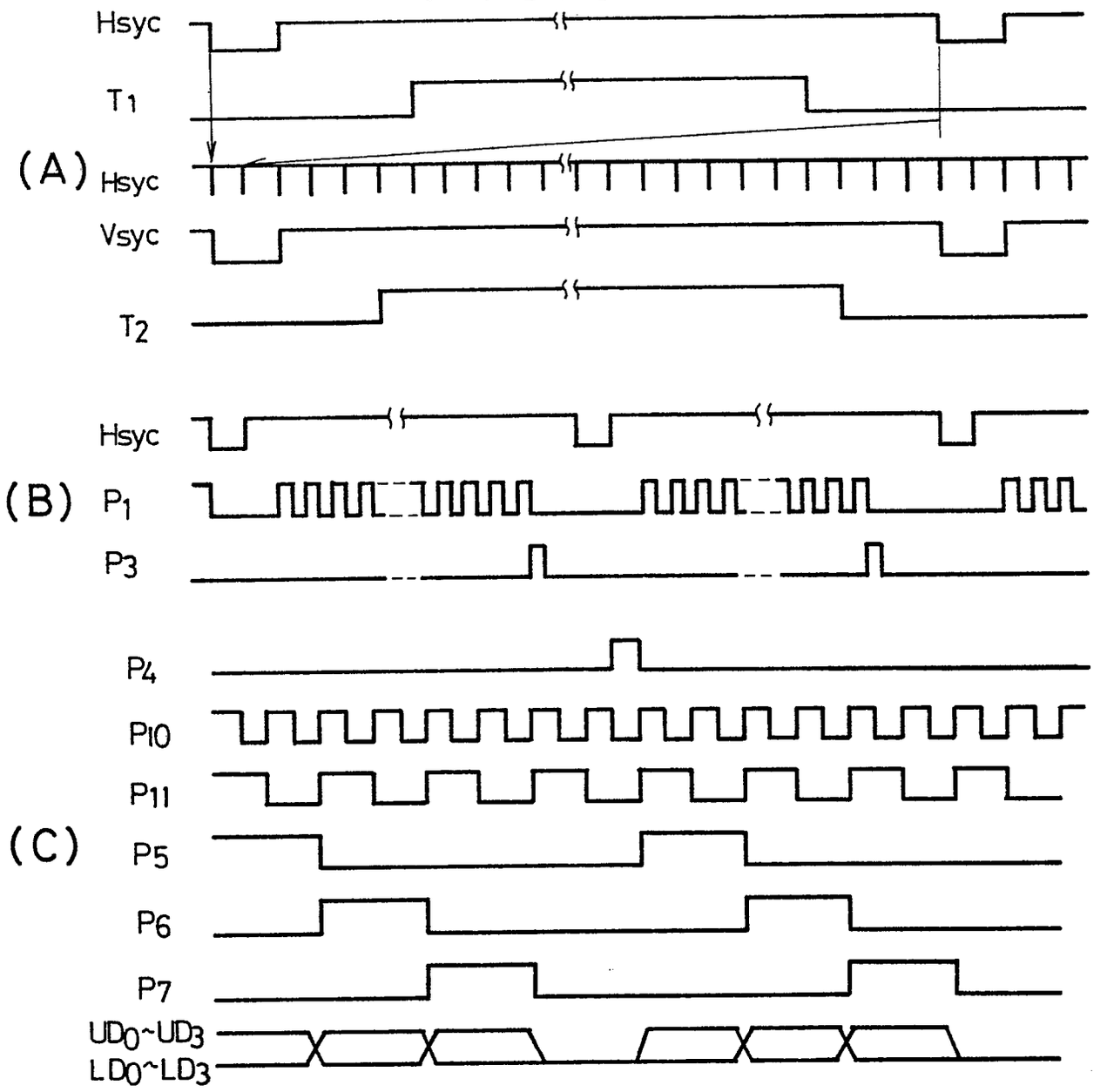
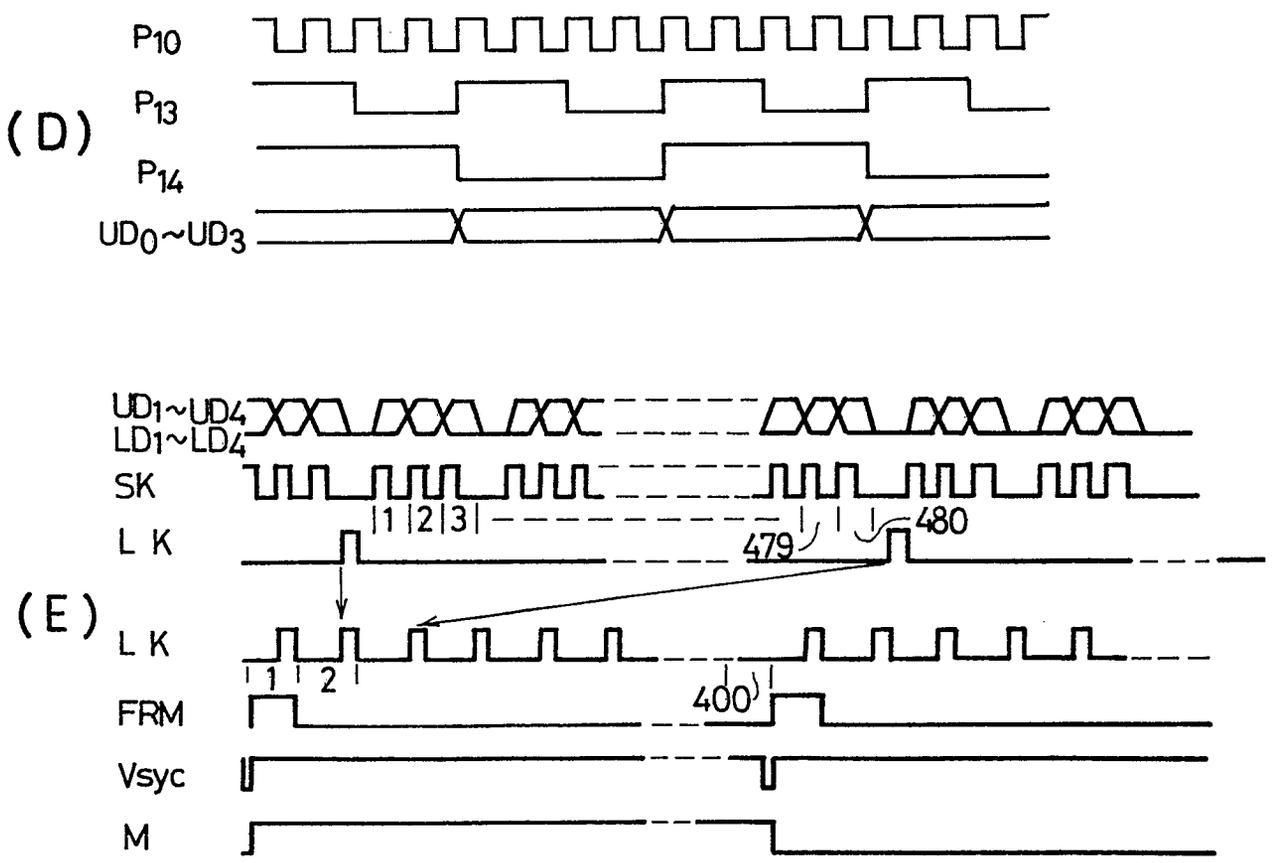

Hsyc
T1
(A)
Hsyc
Vsyc
T2
Hsyc
(B)
P1
P3
P4
P10
P11
(C)
P5
P6
P7
UD0~UD3
LD0~LD3

FIG. 6


(D)
P10
P13
P14
UD0~UD3
UD1~UD4
LD1~LD4
SK
L K
1 2 3
479
480
(E)
L K
1
2
400
FRM
Vsyc
M

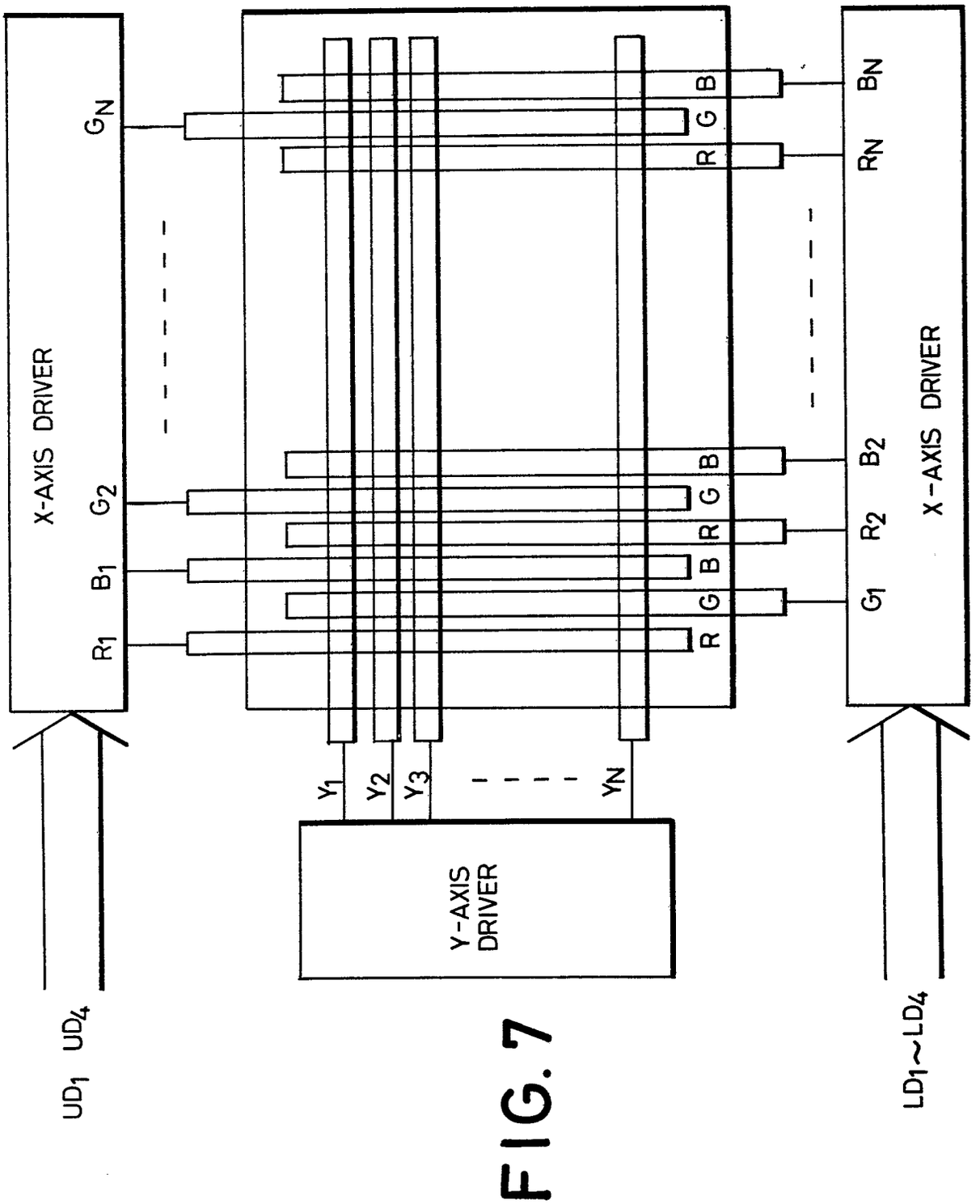

X-AXIS DRIVER
G_N
G_2
B_1
R_1
R G B
B_N
R_N
B_2
R_2
G_1
X-AXIS DRIVER
Y_1
Y_2
Y_3
Y_N
Y-AXIS DRIVER
UD_1 UD_4
LD_1~LD_4

FIG. 7

FIG.8A

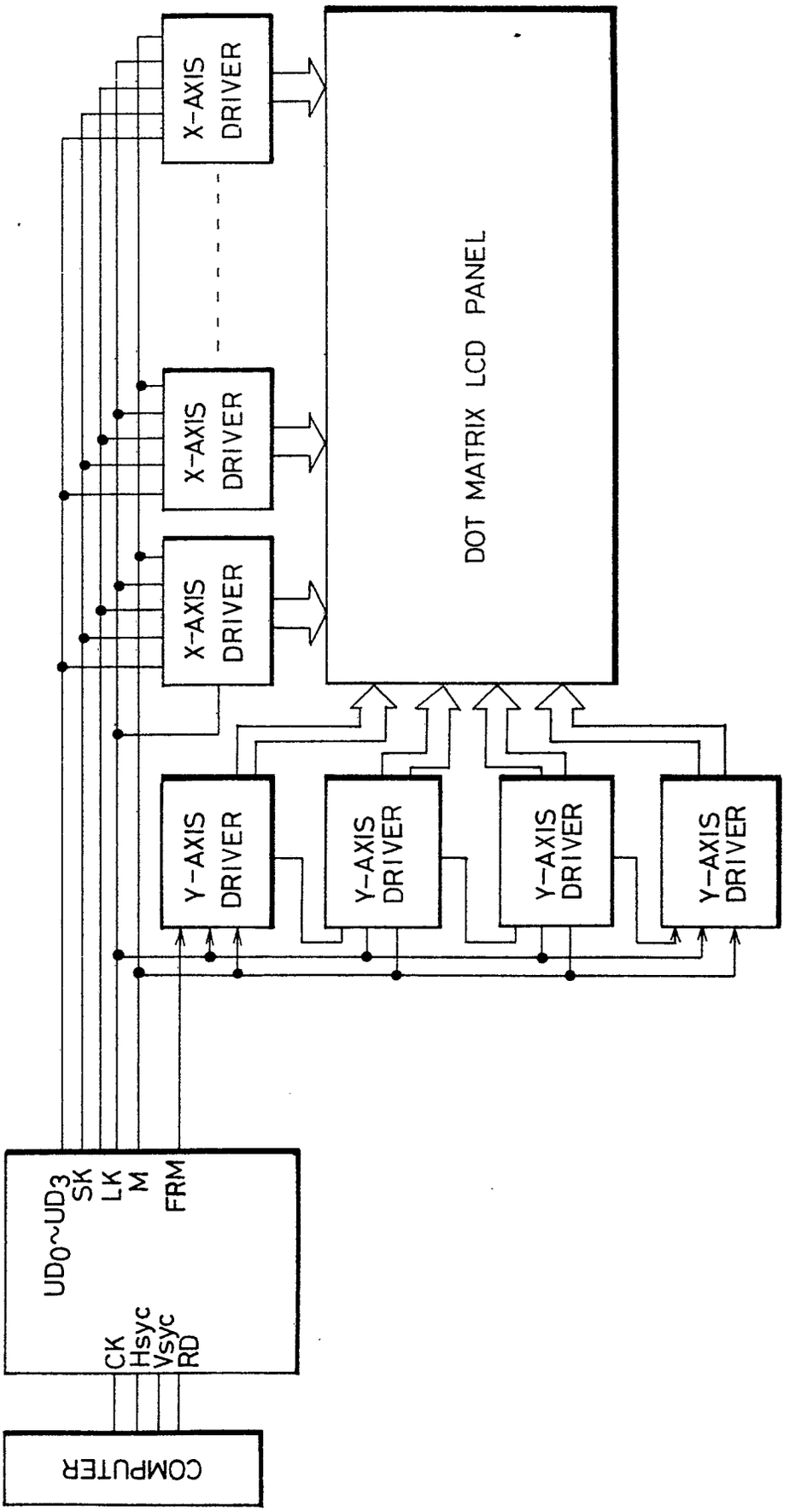

X-AXIS DRIVER
X-AXIS DRIVER
X-AXIS DRIVER
DOT MATRIX LCD PANEL
Y-AXIS DRIVER
Y-AXIS DRIVER
Y-AXIS DRIVER
Y-AXIS DRIVER
UD0~UD3
SK
LK
M
FRM
CK
Hsyc
Vsyc
RD
COMPUTER

FIG. 8 B

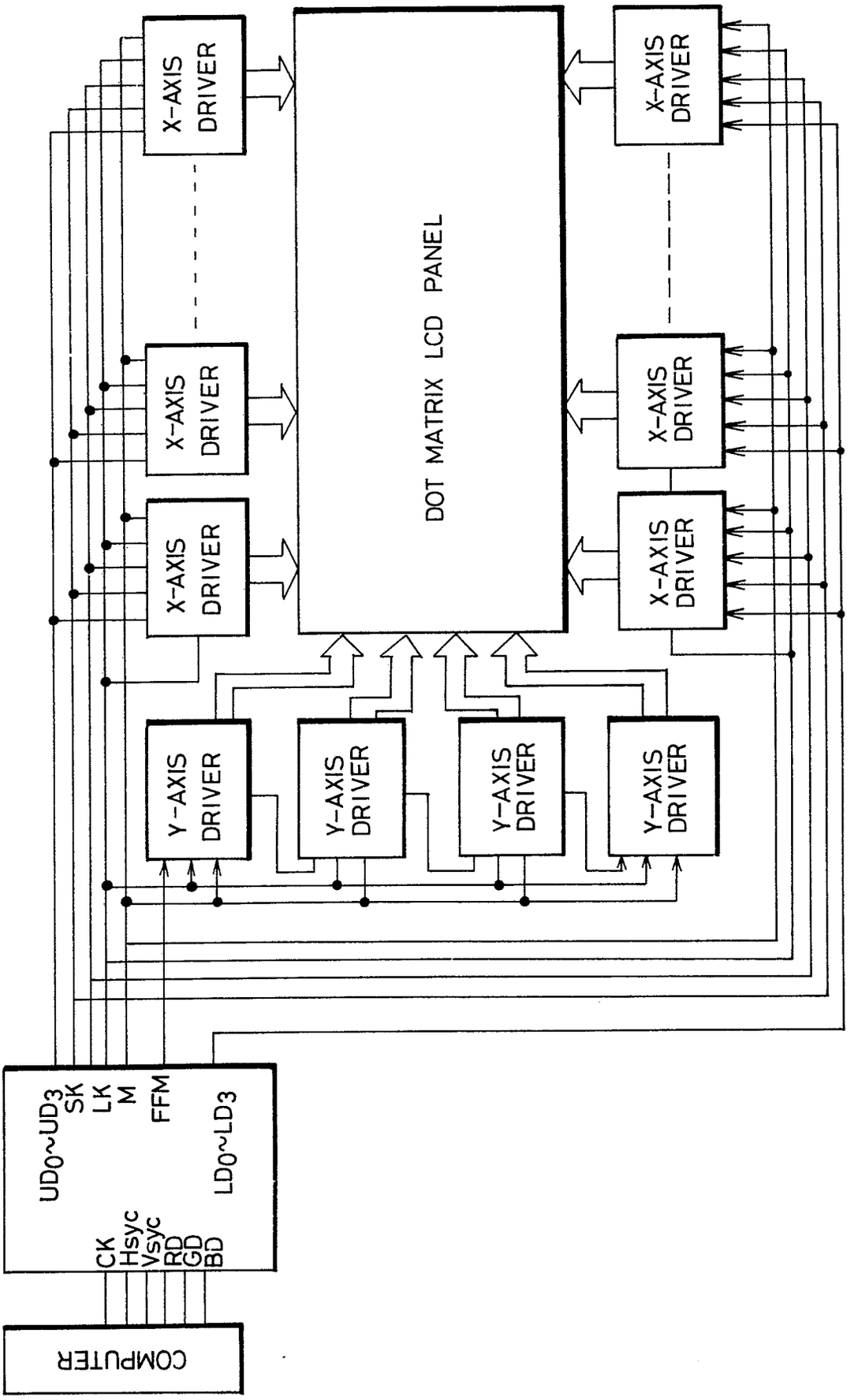

X-AXIS DRIVER
X-AXIS DRIVER
X-AXIS DRIVER
DOT MATRIX LCD PANEL
X-AXIS DRIVER
X-AXIS DRIVER
X-AXIS DRIVER
Y-AXIS DRIVER
Y-AXIS DRIVER
Y-AXIS DRIVER
Y-AXIS DRIVER
UD0~UD3
SK
LK
M
FFM
LD0~LD3
CK
Hsyc
Vsyc
RD
GD
BD
COMPUTER

FIG.9

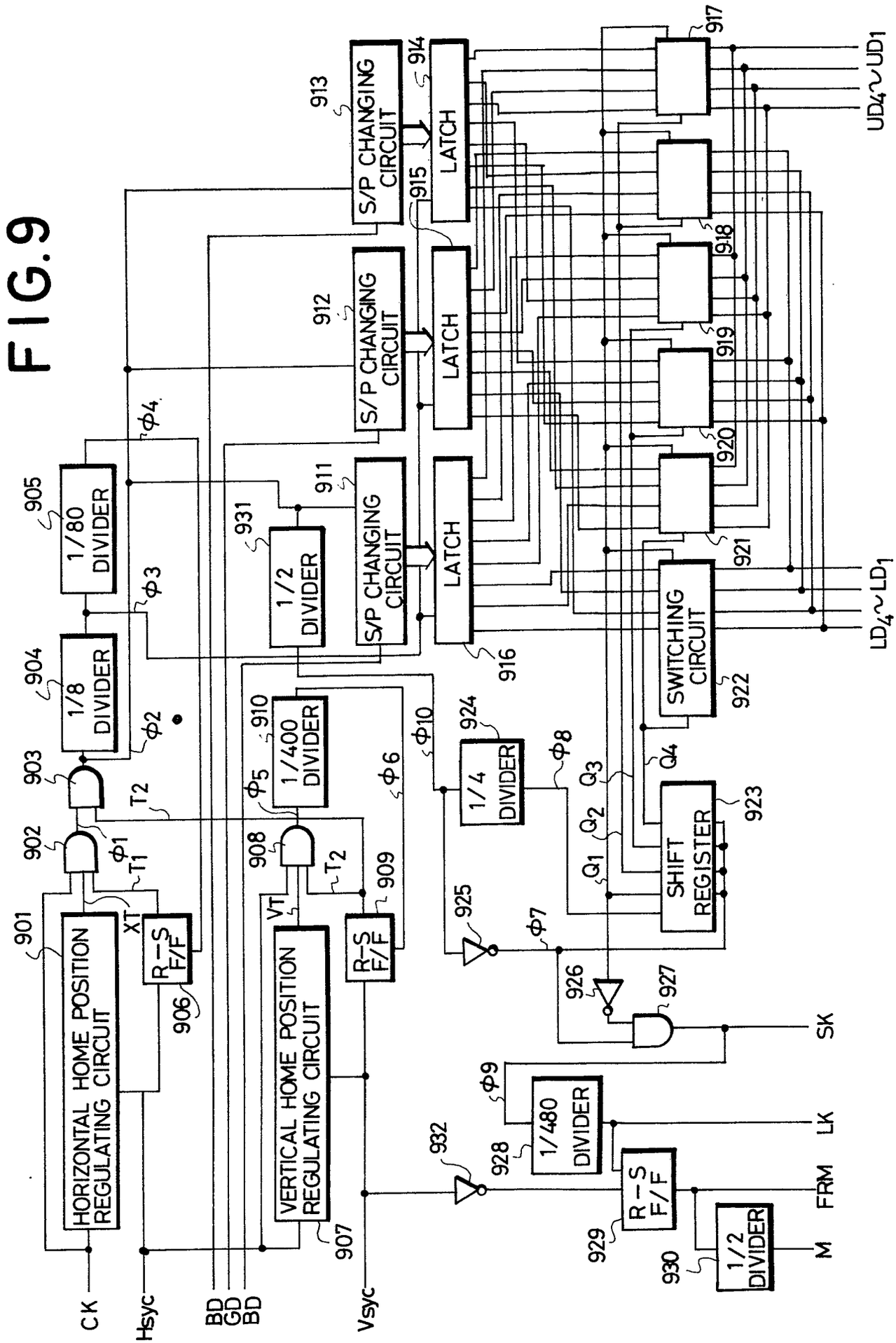

CK
Hsyc
BD
GD
BD
Vsyc
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME POSITION REGULATING CIRCUIT
R-S F/F
1/80 DIVIDER
1/8 DIVIDER
1/2 DIVIDER
1/400 DIVIDER
1/4 DIVIDER
1/480 DIVIDER
S/P CHANGING CIRCUIT
LATCH
SWITCHING CIRCUIT
SHIFT REGISTER
UD4~UD1
LD4~LD1
SK
LK
FRM
M

FIG.10

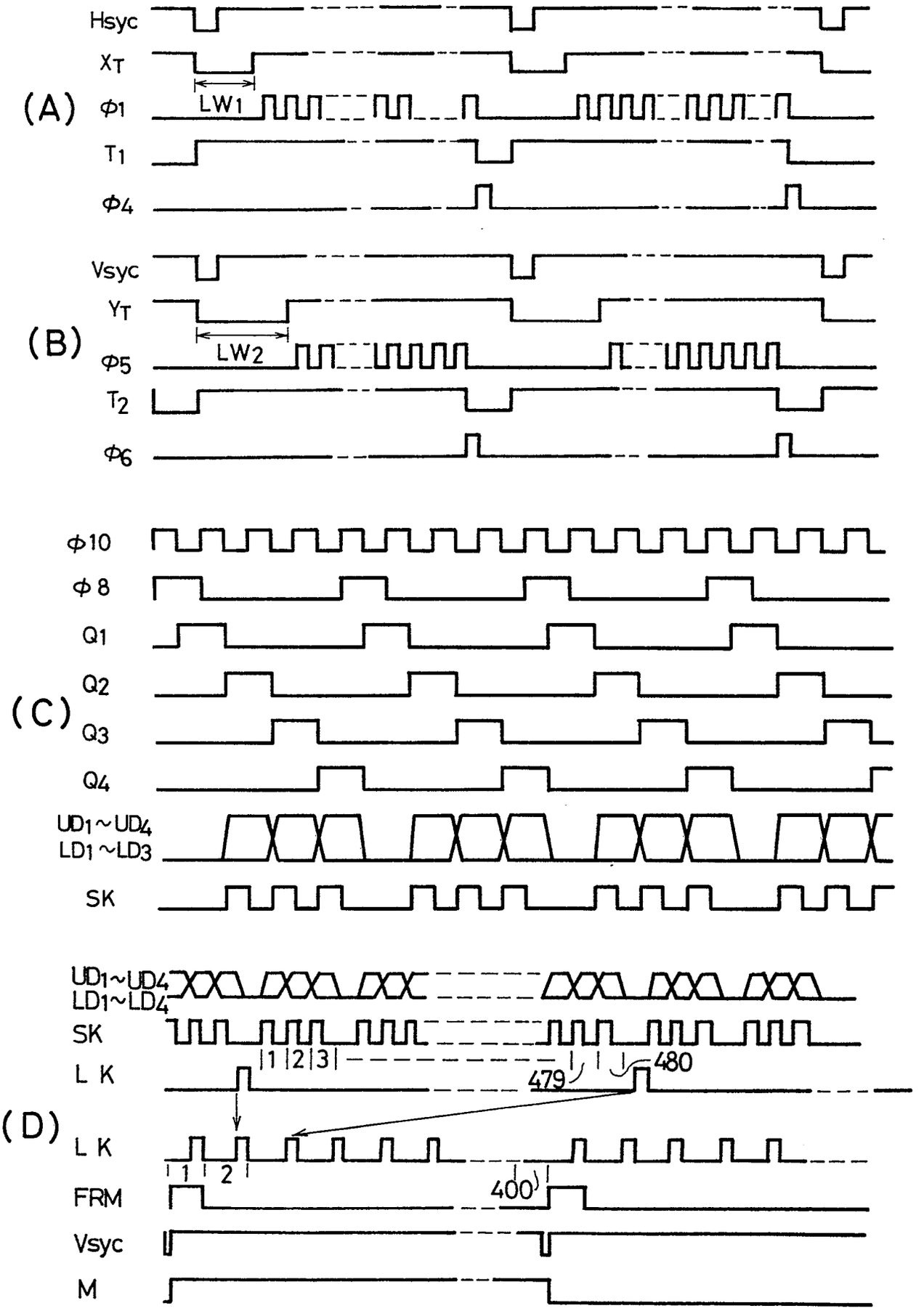

Hsyc
XT
(A)
LW1
Φ1
T1
Φ4
Vsyc
YT
(B)
LW2
Φ5
T2
Φ6
Φ10
Φ8
Q1
Q2
(C)
Q3
Q4
UD1~UD4
LD1~LD3
SK
UD1~UD4
LD1~LD4
SK
L K
1 2 3
479
480
(D)
L K
1
2
FRM
400
Vsyc
M

FIG. 11

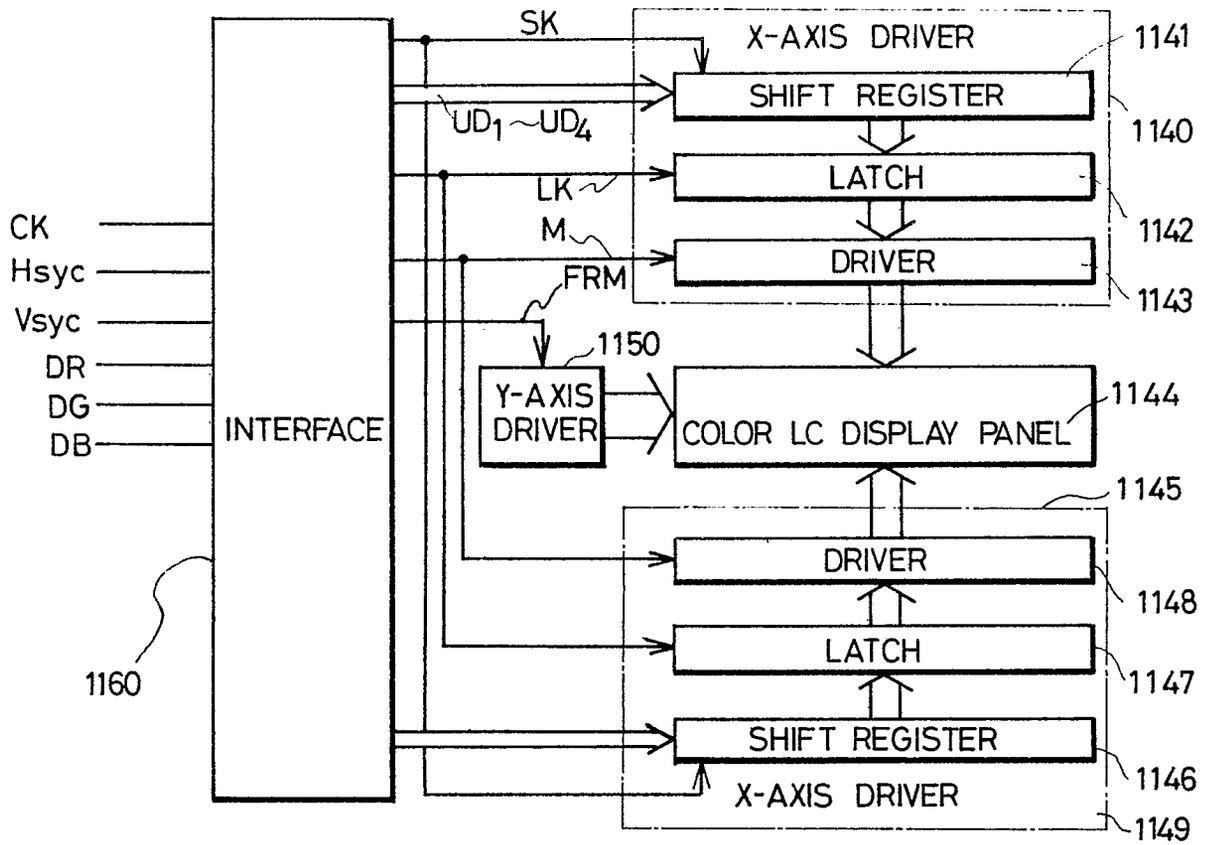

SK
X-AXIS DRIVER
1141
SHIFT REGISTER
1140
UD1~UD4
LATCH
LK
1142
M
DRIVER
FRM
1143
CK
Hsyc
Vsyc
DR
DG
DB
1150
Y-AXIS DRIVER
COLOR LC DISPLAY PANEL
1144
INTERFACE
1145
DRIVER
1148
LATCH
1147
1160
SHIFT REGISTER
1146
X-AXIS DRIVER
1149

FIG.12

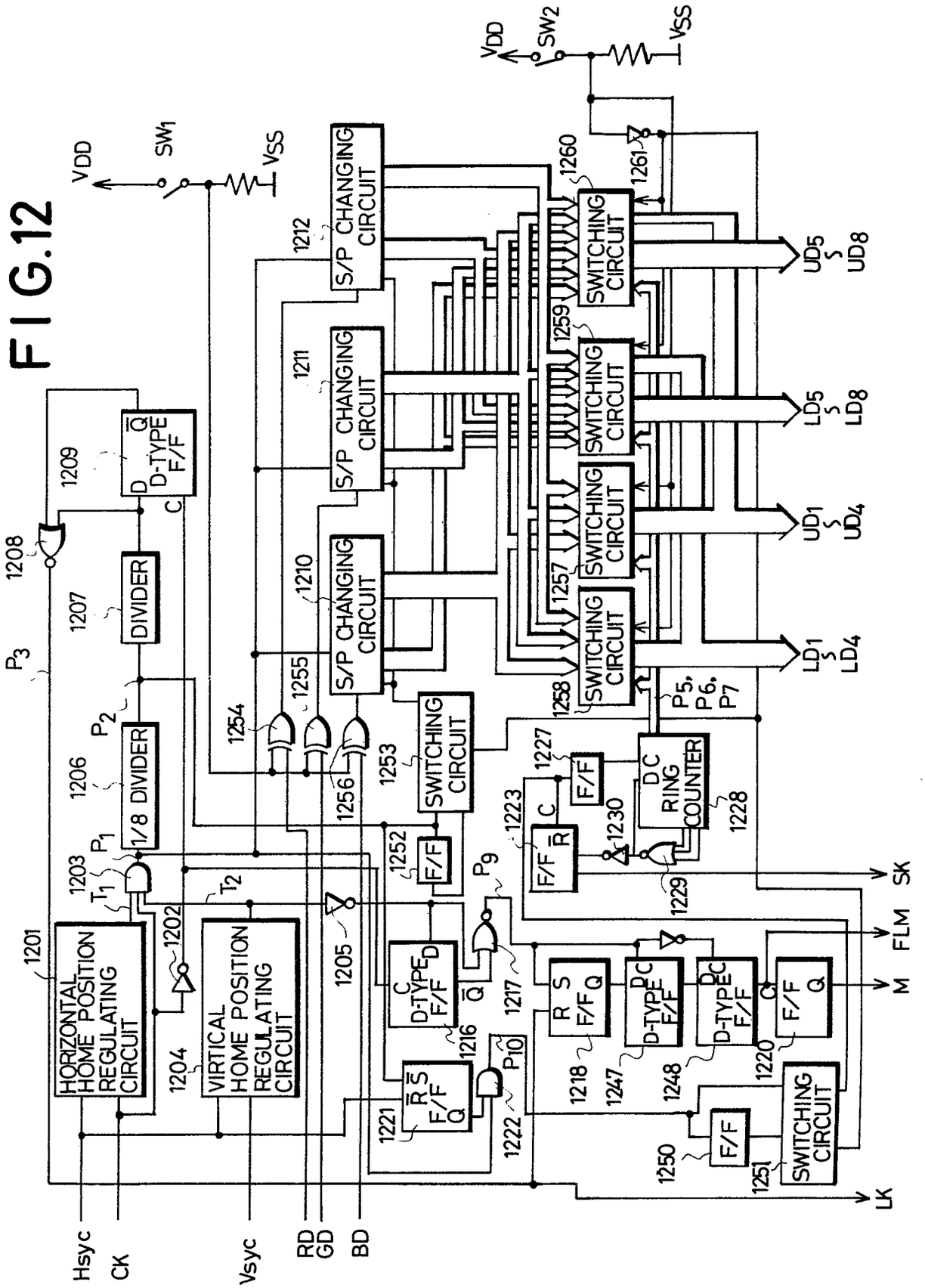
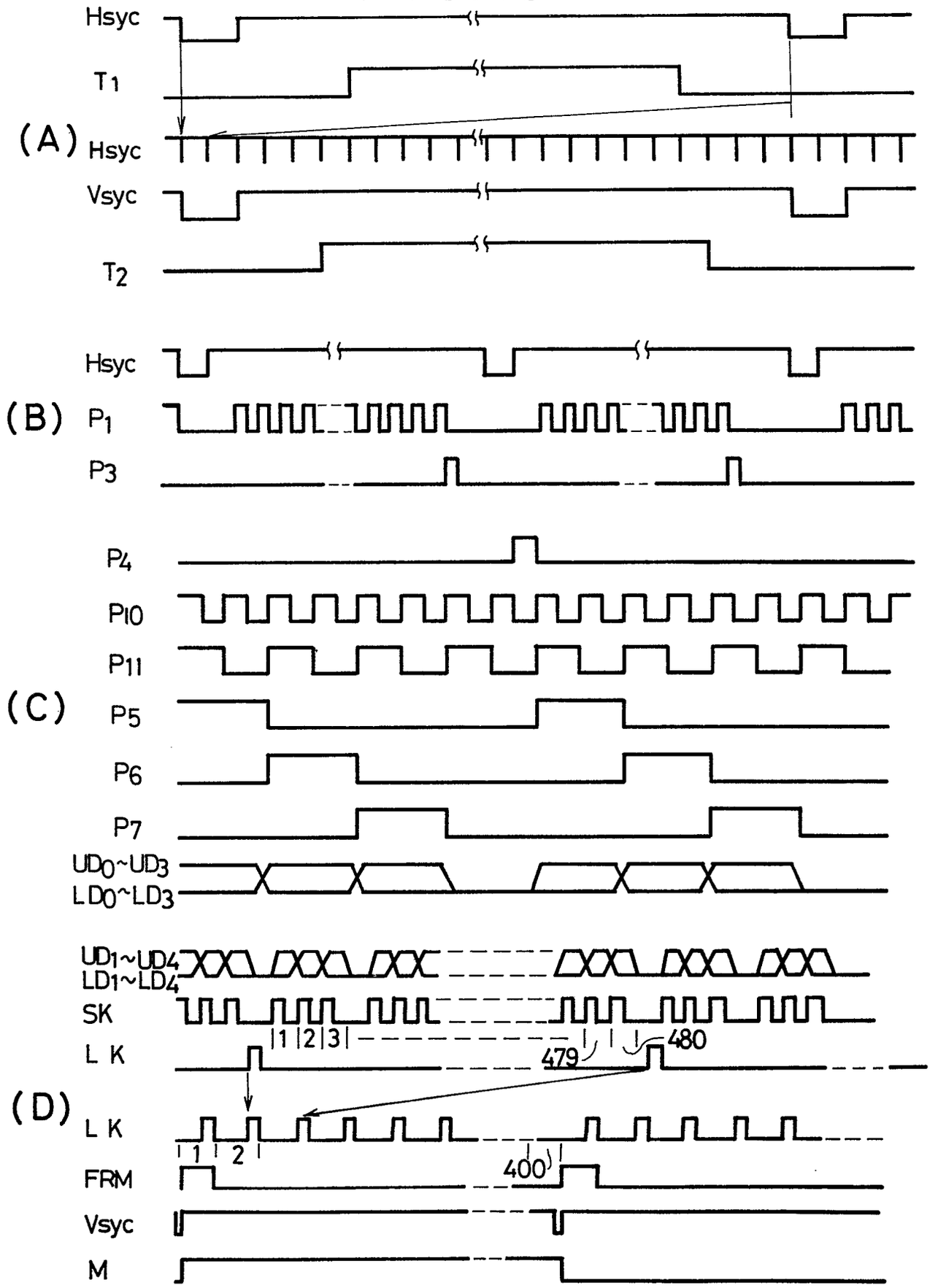
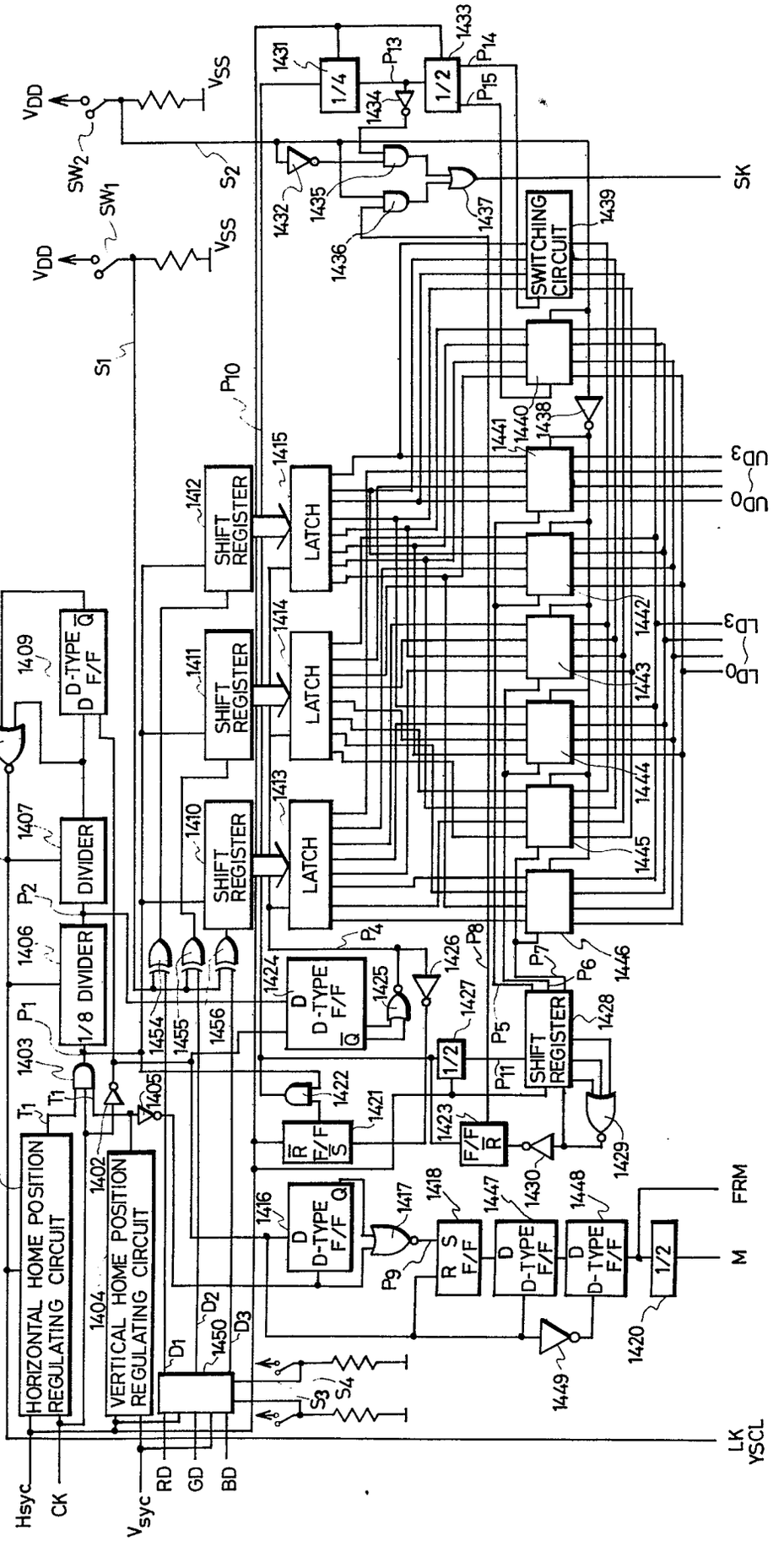

VDD
SW1
VSS
VDD
SW2
VSS
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VIRTICAL HOME POSITION REGULATING CIRCUIT
1/8 DIVIDER
DIVIDER
D-TYPE F/F
S/P CHANGING CIRCUIT
SWITCHING CIRCUIT
DC RING COUNTER
F/F
R S F/F
Hsyc
CK
Vsyc
RD
GD
BD
SK
FLM
LK
UD5 ~ UD8
LD5 ~ LD8
UD1 ~ UD4
LD1 ~ LD4

FIG. 13


Hsyc
T1
(A)
Hsyc
Vsyc
T2
Hsyc
(B)
P1
P3
P4
P10
P11
(C)
P5
P6
P7
UD0~UD3
LD0~LD3
UD1~UD4
LD1~LD4
SK
L K
1 2 3
479
480
(D)
L K
1
2
FRM
400
Vsyc
M

0 244 978

FIG. 14



0 244 978

FIG.15

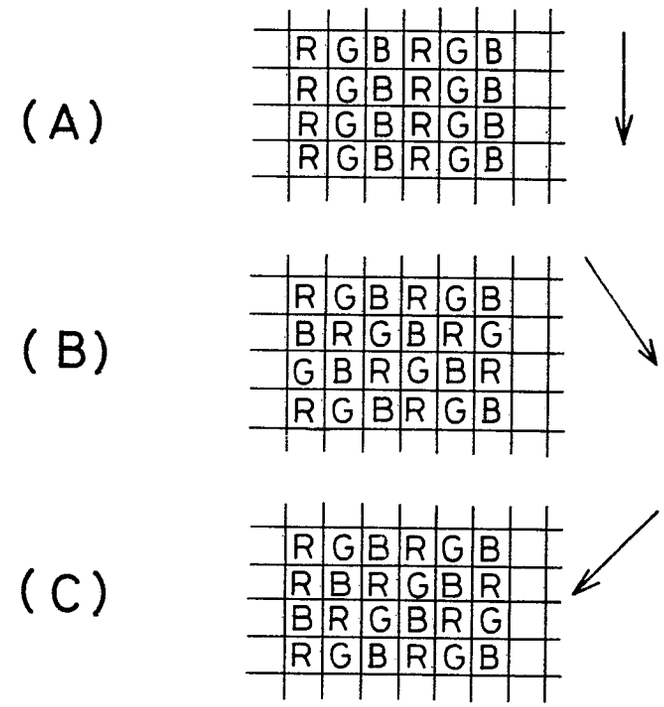


FIG.16

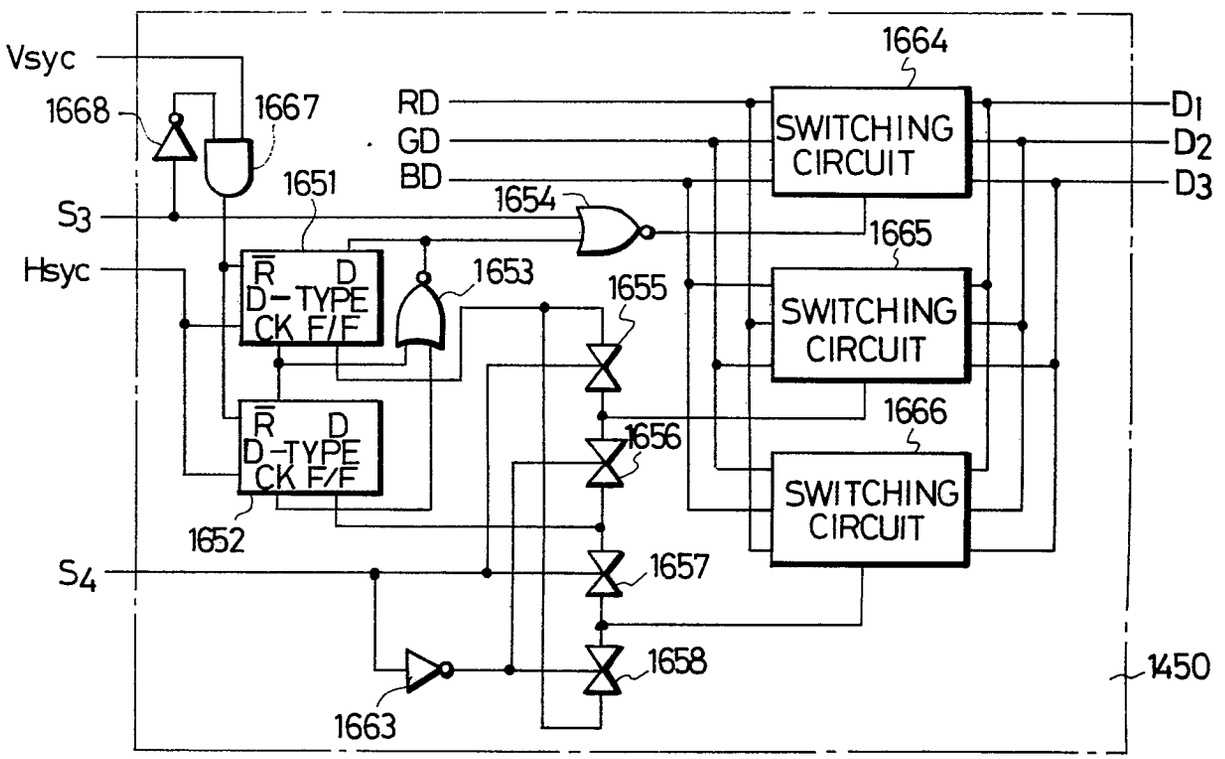
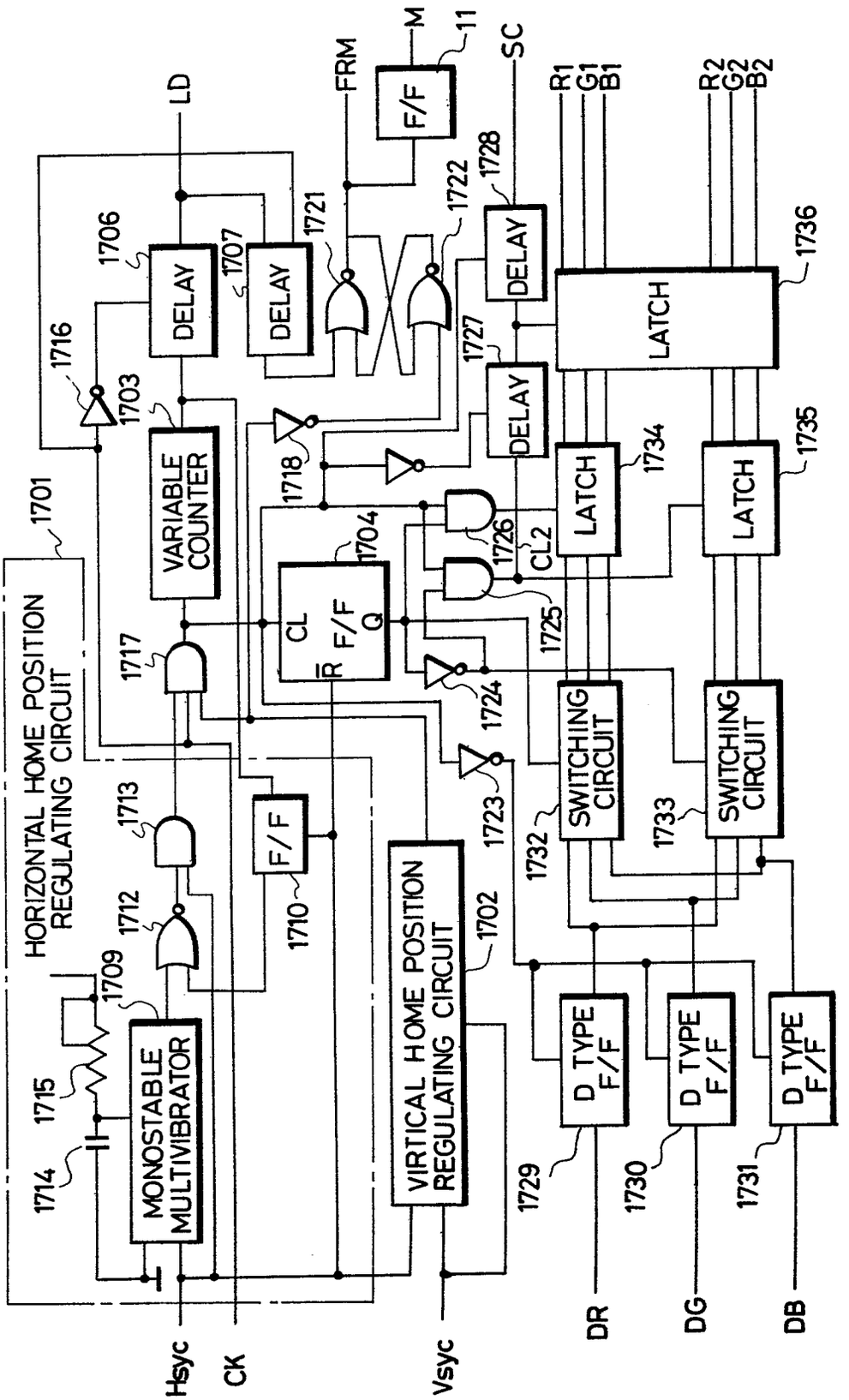


FIG.17


HORIZONTAL HOME POSITION REGULATING CIRCUIT
1701
VIRTICAL HOME POSITION REGULATING CIRCUIT
1702
VARIABLE COUNTER
1703
1704
CL
R
F/F
Q
MONOSTABLE MULTIVIBRATOR
1709
1710
F/F
1712
1713
1714
1715
1716
1717
1718
DELAY
1706
DELAY
1707
1721
1722
DELAY
1727
DELAY
1728
F/F
11
M
FRM
LD
SC
1723
1724
1725
1726
CL2
LATCH
1734
LATCH
1735
LATCH
1736
SWITCHING CIRCUIT
1732
SWITCHING CIRCUIT
1733
D TYPE F/F
1729
D TYPE F/F
1730
D TYPE F/F
1731
R1
G1
B1
R2
G2
B2
DR
DG
DB
Hsyc
CK
Vsyc

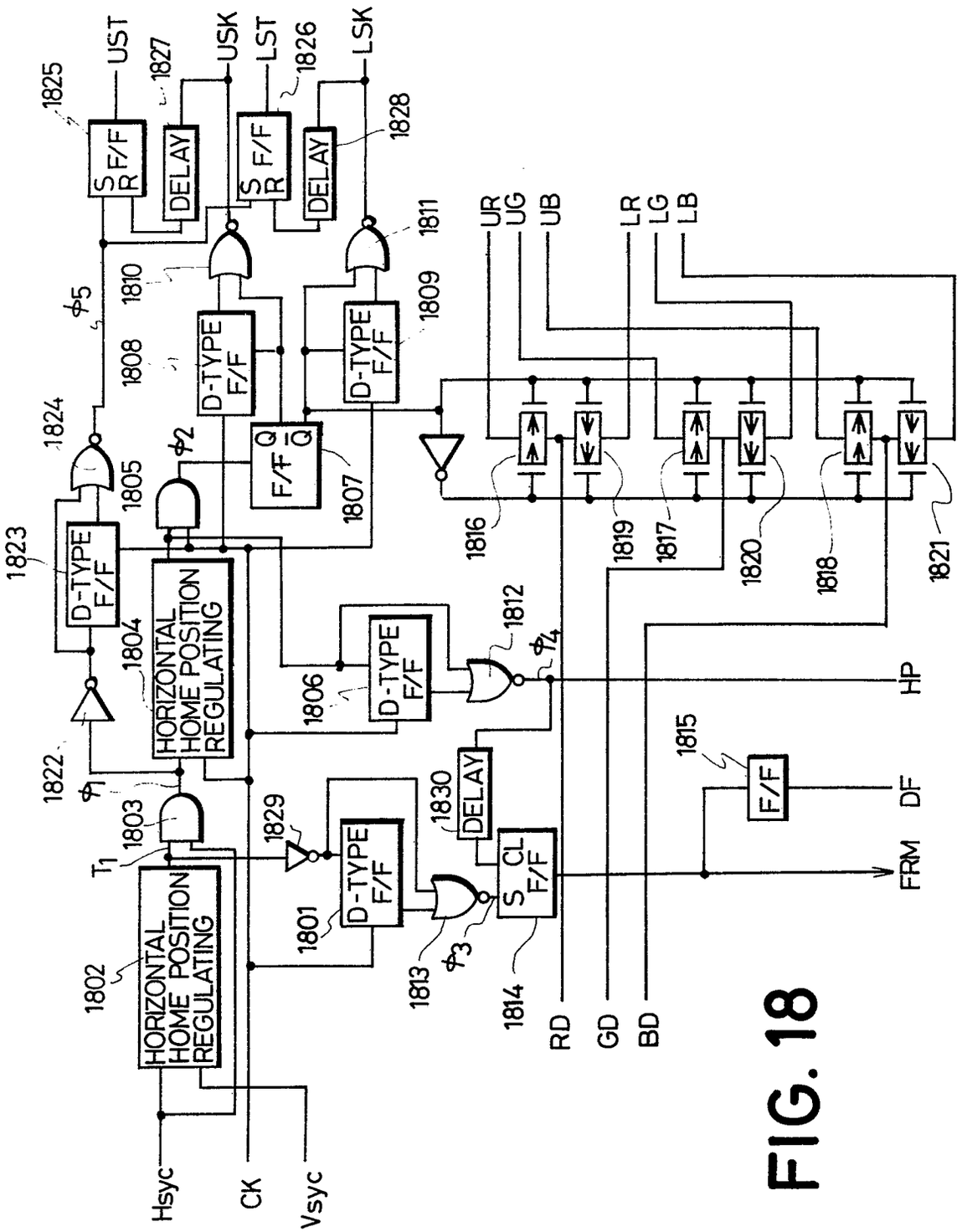

HORIZONTAL HOME POSITION REGULATING
HORIZONTAL HOME POSITION REGULATING
D-TYPE F/F
D-TYPE F/F
D-TYPE F/F
D-TYPE F/F
D-TYPE F/F
S R F/F
S R F/F
S CL F/F
F/F
DELAY
DELAY
DELAY
F/F
Q
Q
Hsyc
CK
Vsyc
UST
USK
LST
LSK
HP
DF
FRM
RD
GD
BD
UR
UG
UB
LR
LG
LB
T1
φ1
φ2
φ3
φ4
φ5
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830

FIG. 18

FIG.19

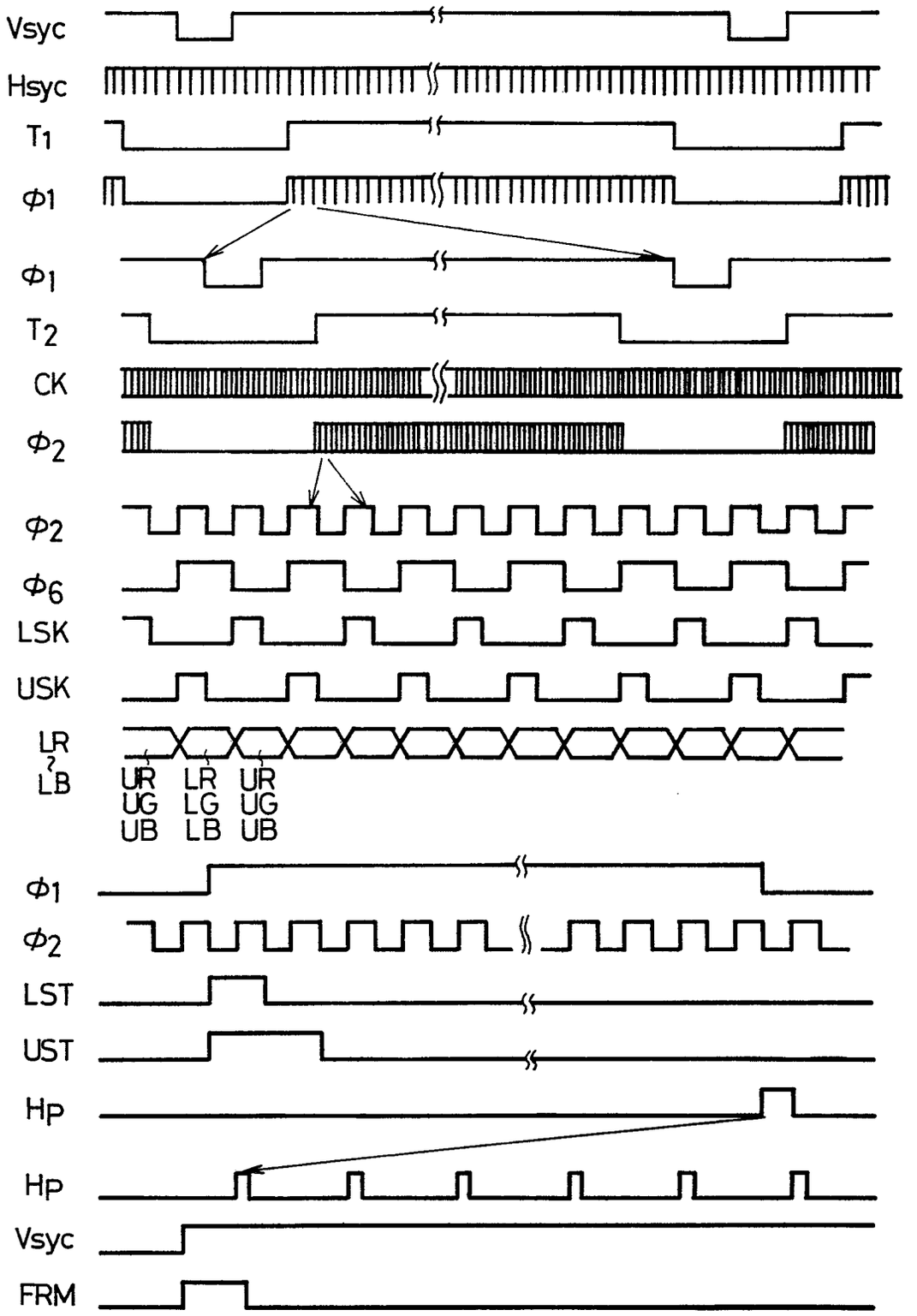

Vsyc
Hsyc
T1
Φ1
Φ1
T2
CK
Φ2
Φ2
Φ6
LSK
USK
LR
LB
UR LR UR
UG LG UG
UB LB UB
Φ1
Φ2
LST
UST
Hp
Hp
Vsyc
FRM

FIG. 20

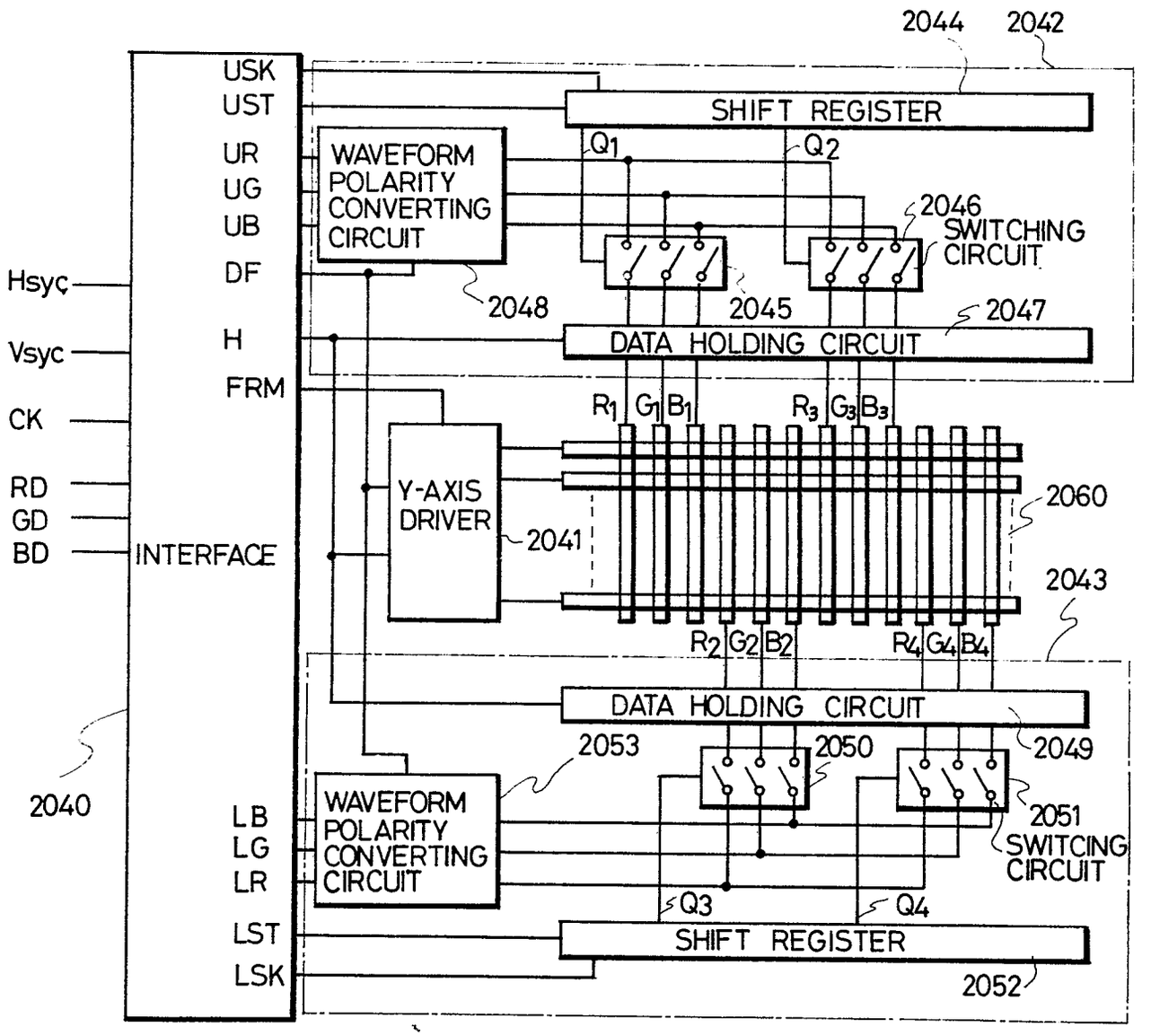

2044
2042
USK
UST
SHIFT REGISTER
UR
UG
UB
WAVEFORM POLARITY CONVERTING CIRCUIT
Q1
Q2
2046
SWITCHING CIRCUIT
Hsyc
DF
2048
2045
2047
Vsyc
H
DATA HOLDING CIRCUIT
FRM
R1 G1 B1
R3 G3 B3
CK
Y-AXIS DRIVER
2041
2060
RD
GD
BD
INTERFACE
2043
R2 G2 B2
R4 G4 B4
DATA HOLDING CIRCUIT
2049
2053
2050
2051
SWITCING CIRCUIT
2040
LB
LG
LR
WAVEFORM POLARITY CONVERTING CIRCUIT
Q3
Q4
LST
SHIFT REGISTER
LSK
2052

FIG.21

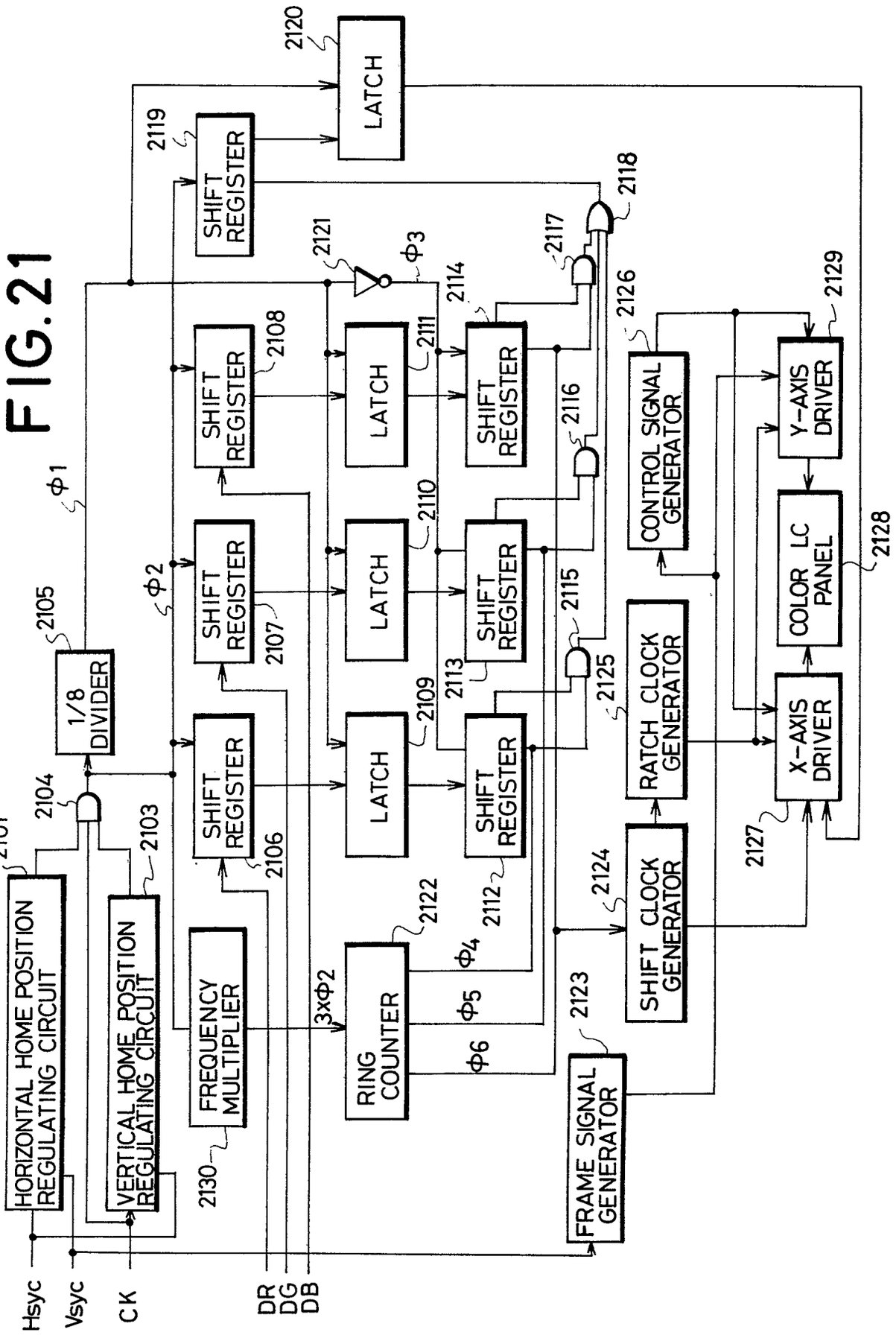

HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME POSITION REGULATING CIRCUIT
FREQUENCY MULTIPLIER
1/8 DIVIDER
SHIFT REGISTER
LATCH
RING COUNTER
FRAME SIGNAL GENERATOR
SHIFT CLOCK GENERATOR
RATCH CLOCK GENERATOR
CONTROL SIGNAL GENERATOR
X-AXIS DRIVER
Y-AXIS DRIVER
COLOR LC PANEL
Hsyc
Vsyc
CK
DR
DG
DB
Φ1
Φ2
Φ3
Φ4
Φ5
Φ6
3xΦ2
2101
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130

FIG. 22

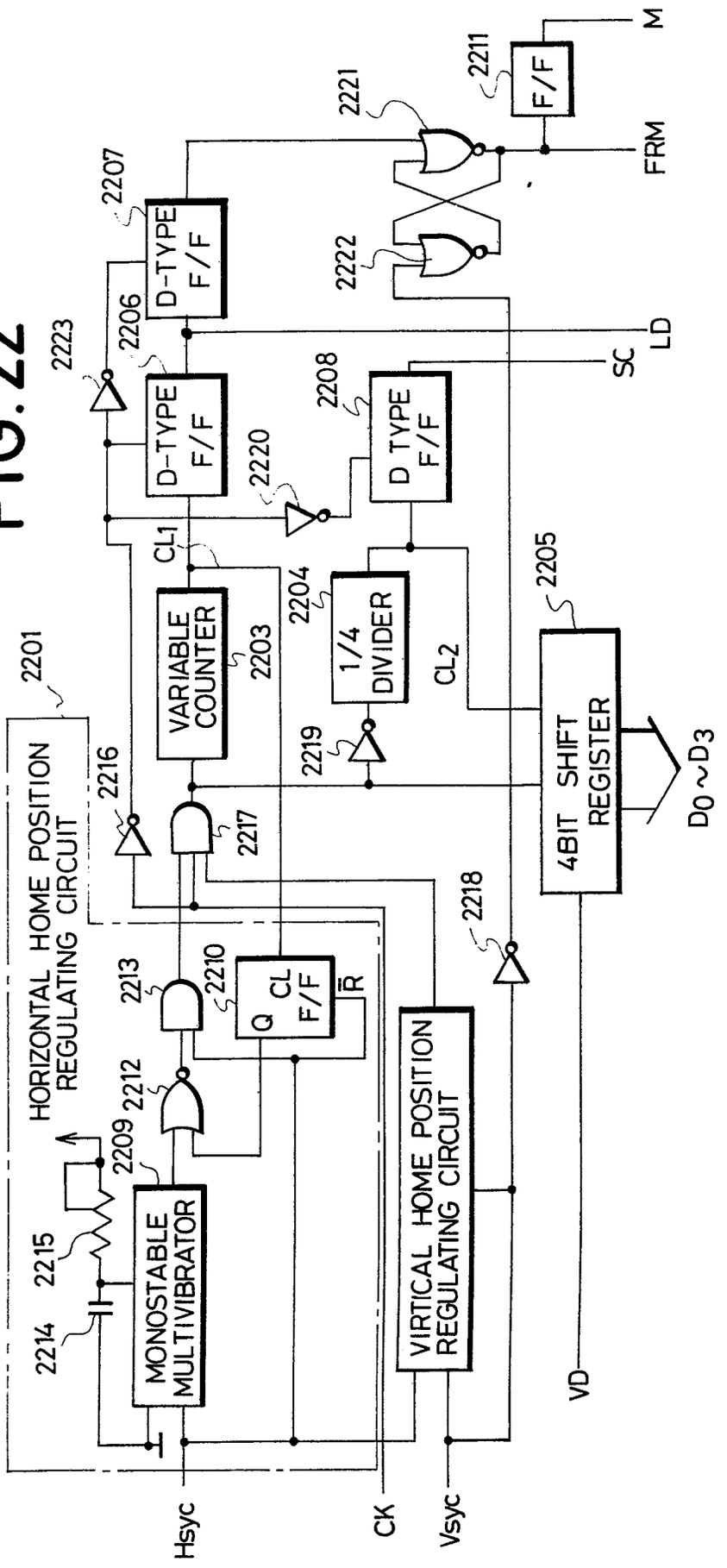

HORIZONTAL HOME POSITION REGULATING CIRCUIT
2201
VARIABLE COUNTER
2203
1/4 DIVIDER
2204
4BIT SHIFT REGISTER
2205
D-TYPE F/F
2206
D-TYPE F/F
2207
D TYPE F/F
2208
F/F
2211
MONOSTABLE MULTIVIBRATOR
2209
CL F/F
2210
VIRTICAL HOME POSITION REGULATING CIRCUIT
2215
2214
2216
2217
2218
2219
2220
2221
2222
2223
2212
2213
CL1
CL2
M
FRM
LD
SC
D0~D3
VD
Hsyc
CK
Vsyc

FIG. 23

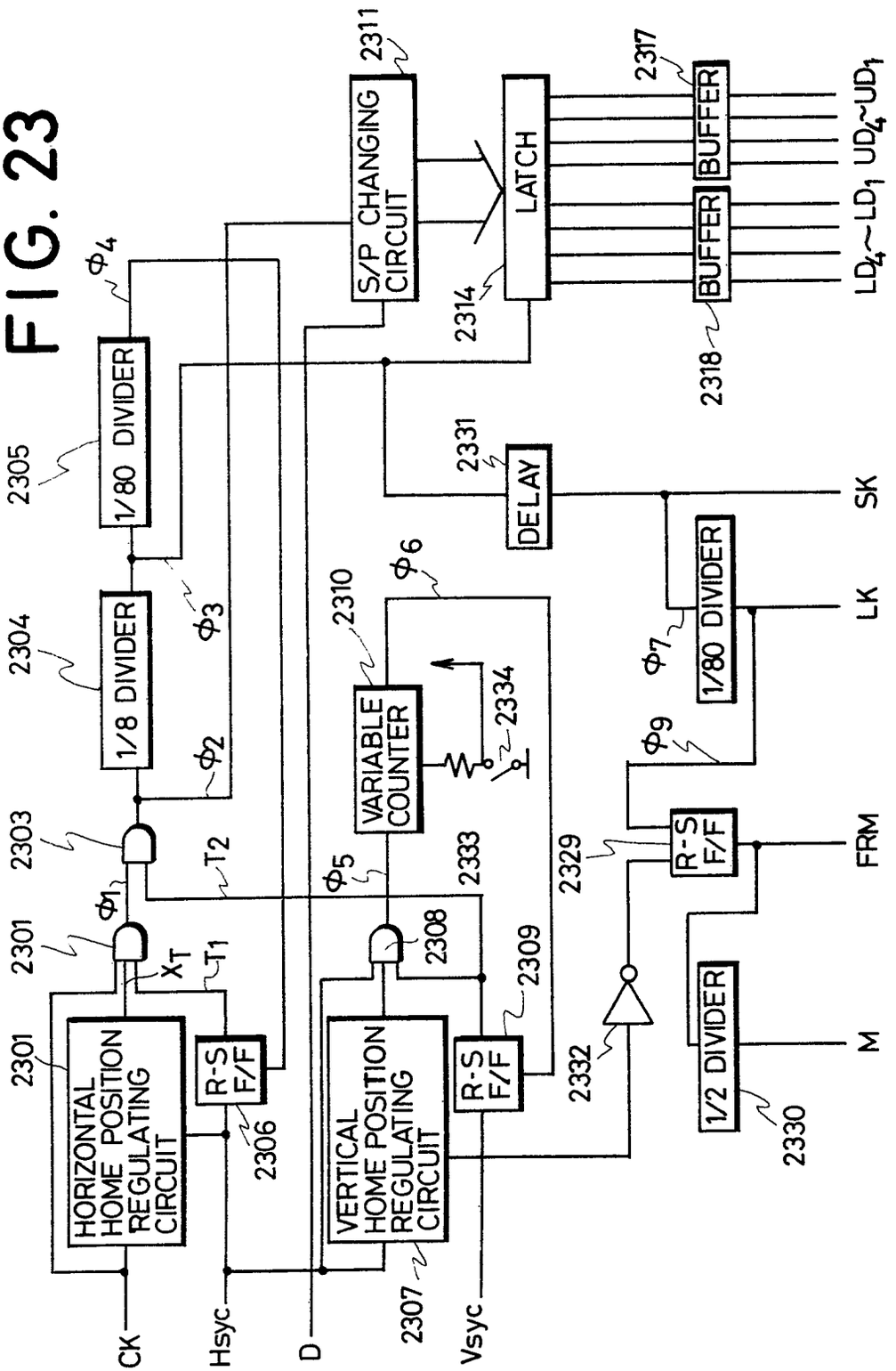

CK
Hsyc
D
Vsyc
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME POSITION REGULATING CIRCUIT
R-S F/F
R-S F/F
R-S F/F
1/80 DIVIDER
1/8 DIVIDER
1/80 DIVIDER
1/2 DIVIDER
VARIABLE COUNTER
DELAY
S/P CHANGING CIRCUIT
LATCH
BUFFER
BUFFER
2301
2303
2304
2305
2306
2307
2308
2309
2310
2311
2314
2317
2318
2329
2330
2331
2332
2333
2334
ϕ_1
ϕ_2
ϕ_3
ϕ_4
ϕ_5
ϕ_6
ϕ_7
ϕ_9
X_T
T_1
T2
$LD_4 \sim LD_1$ $UD_4 \sim UD_1$
SK
LK
FRM
M

FIG. 24

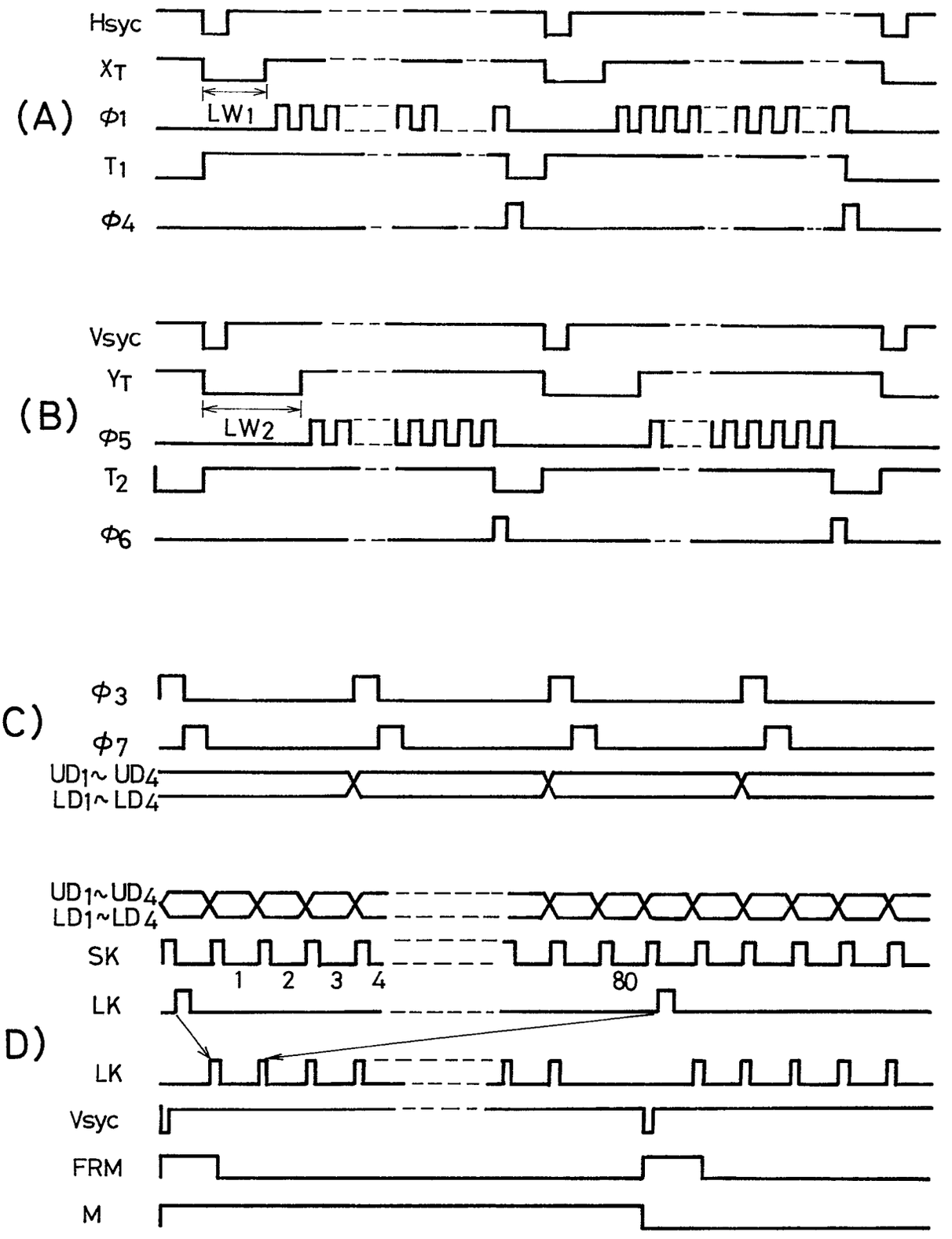

(A)
Hsyc
XT
LW1
Φ1
T1
Φ4
(B)
Vsyc
YT
LW2
Φ5
T2
Φ6
(C)
Φ3
Φ7
UD1~UD4
LD1~LD4
(D)
UD1~UD4
LD1~LD4
SK
1
2
3
4
80
LK
LK
Vsyc
FRM
M

FIG. 25

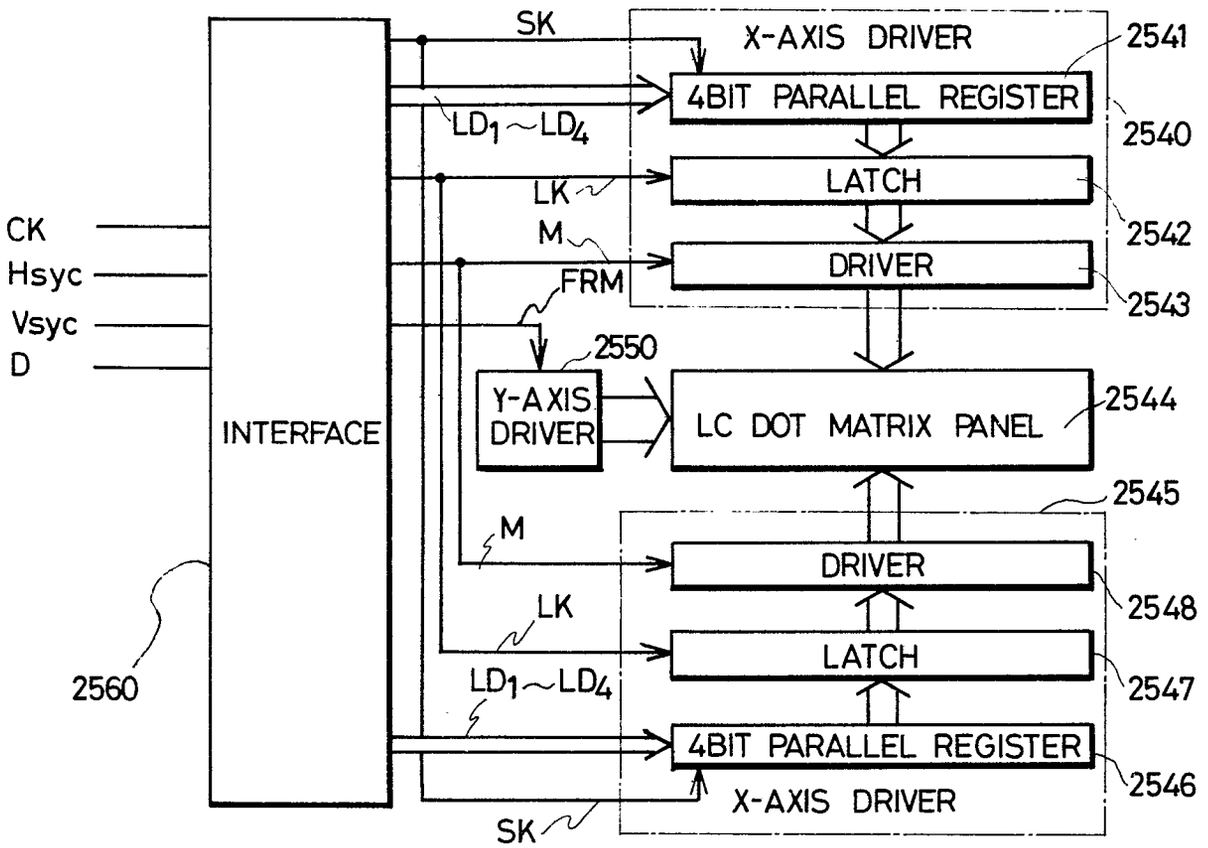

SK
X-AXIS DRIVER
2541
4BIT PARALLEL REGISTER
2540
LD1~LD4
LK
LATCH
2542
M
DRIVER
2543
FRM
2550
CK
Hsyc
Vsyc
D
INTERFACE
Y-AXIS DRIVER
LC DOT MATRIX PANEL
2544
2545
M
DRIVER
2548
LK
LATCH
2547
2560
LD1~LD4
4BIT PARALLEL REGISTER
2546
X-AXIS DRIVER
SK

FIG. 26

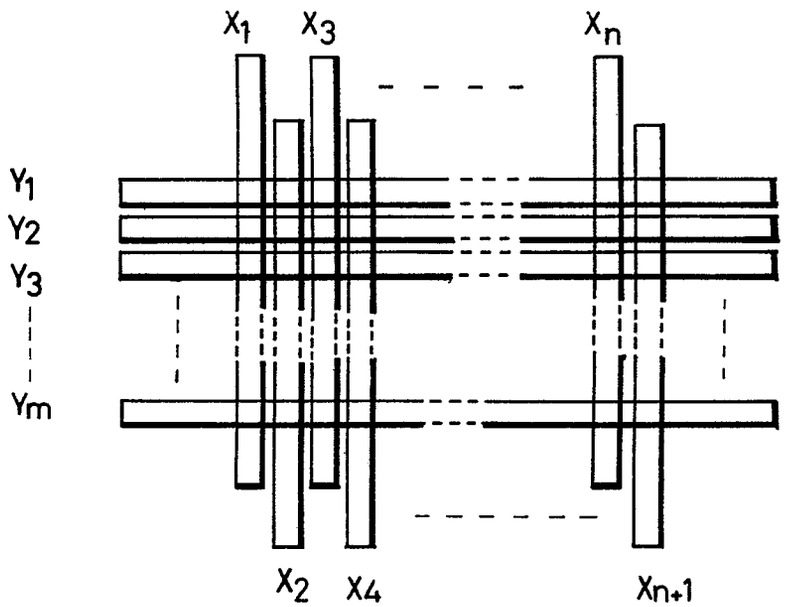

X1
X3
Xn
Y1
Y2
Y3
Ym
X2
X4
Xn+1

FIG. 27

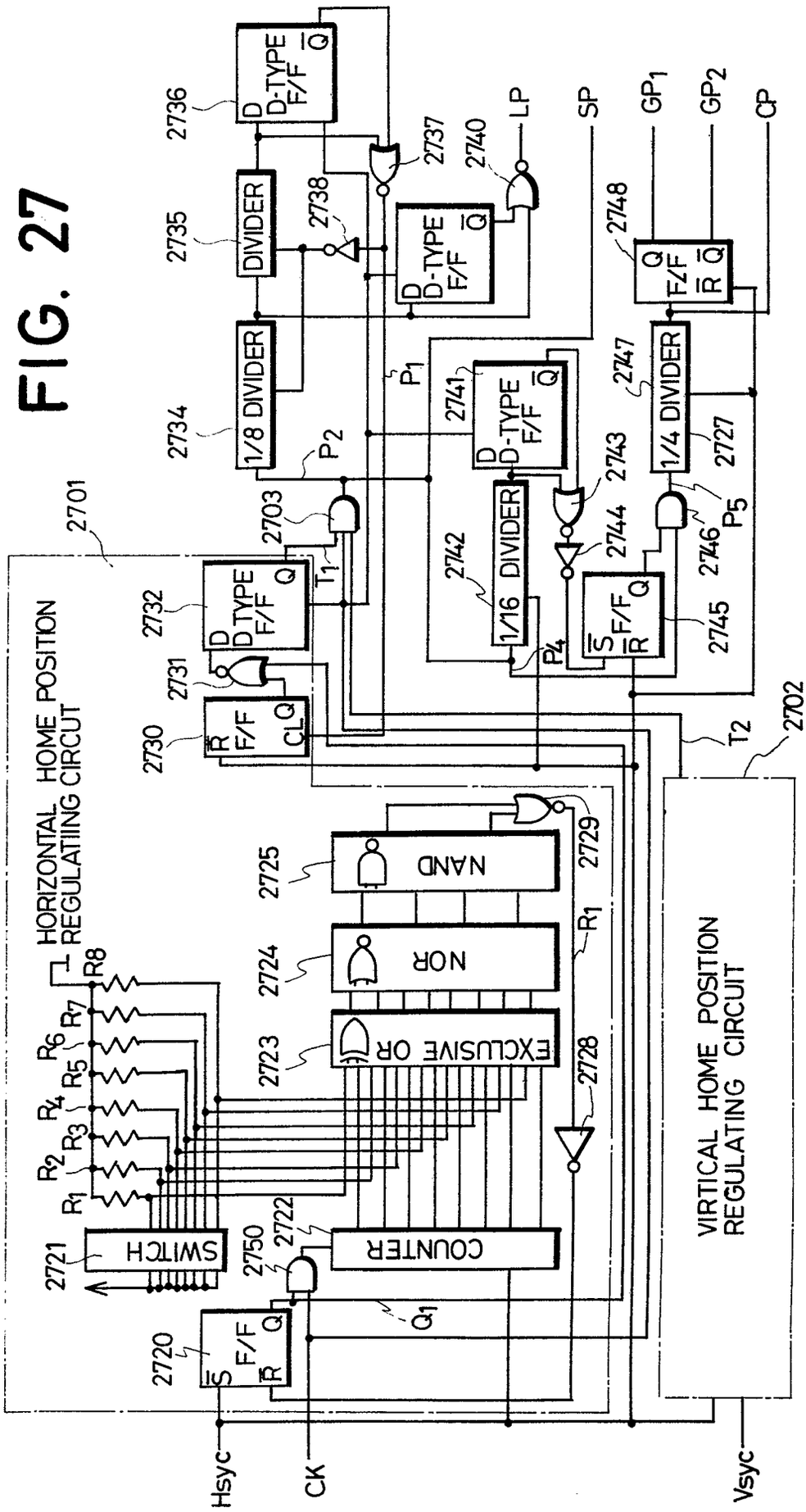

HORIZONTAL HOME POSITION REGULATIING CIRCUT
VIRTICAL HOME POSITION REGULATING CIRCUIT
SWITCH
COUNTER
EXCLUSIVE OR
NOR
NAND
DIVIDER
1/8 DIVIDER
1/16 DIVIDER
1/4 DIVIDER
D-TYPE F/F
F/F
Hsyc
CK
Vsyc
LP
SP
GP1
GP2
CP

FIG.28

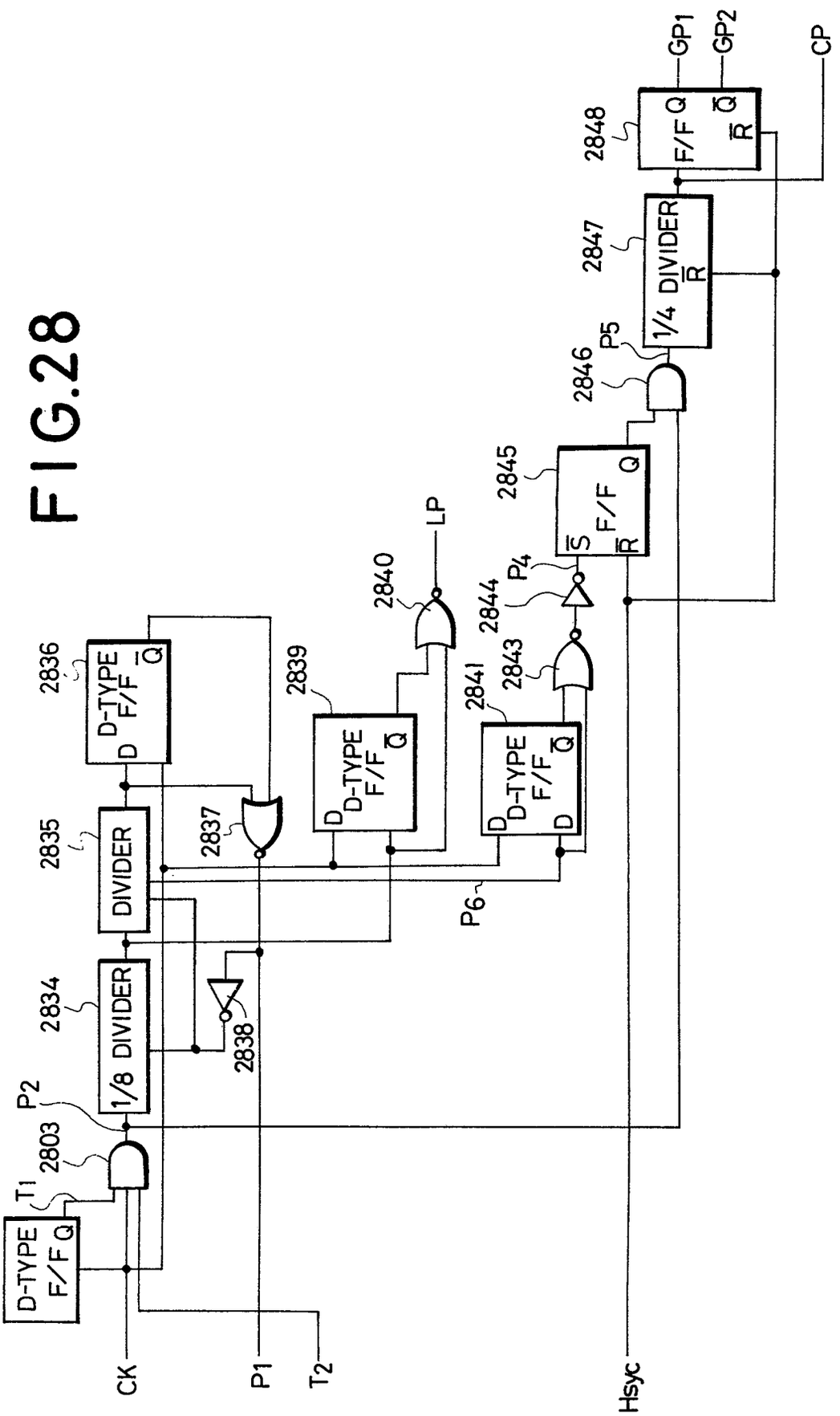

D-TYPE F/F Q
T1
2803
P2
1/8 DIVIDER
2834
DIVIDER
2835
D-TYPE F/F Q
2836
2837
2838
D-TYPE F/F Q
2839
2840
LP
D-TYPE F/F Q
2841
2843
P4
2844
P6
F/F Q
2845
P5
2846
1/4 DIVIDER
2847
F/F Q
2848
GP1
GP2
CP
CK
P1
T2
Hsyc

FIG. 29

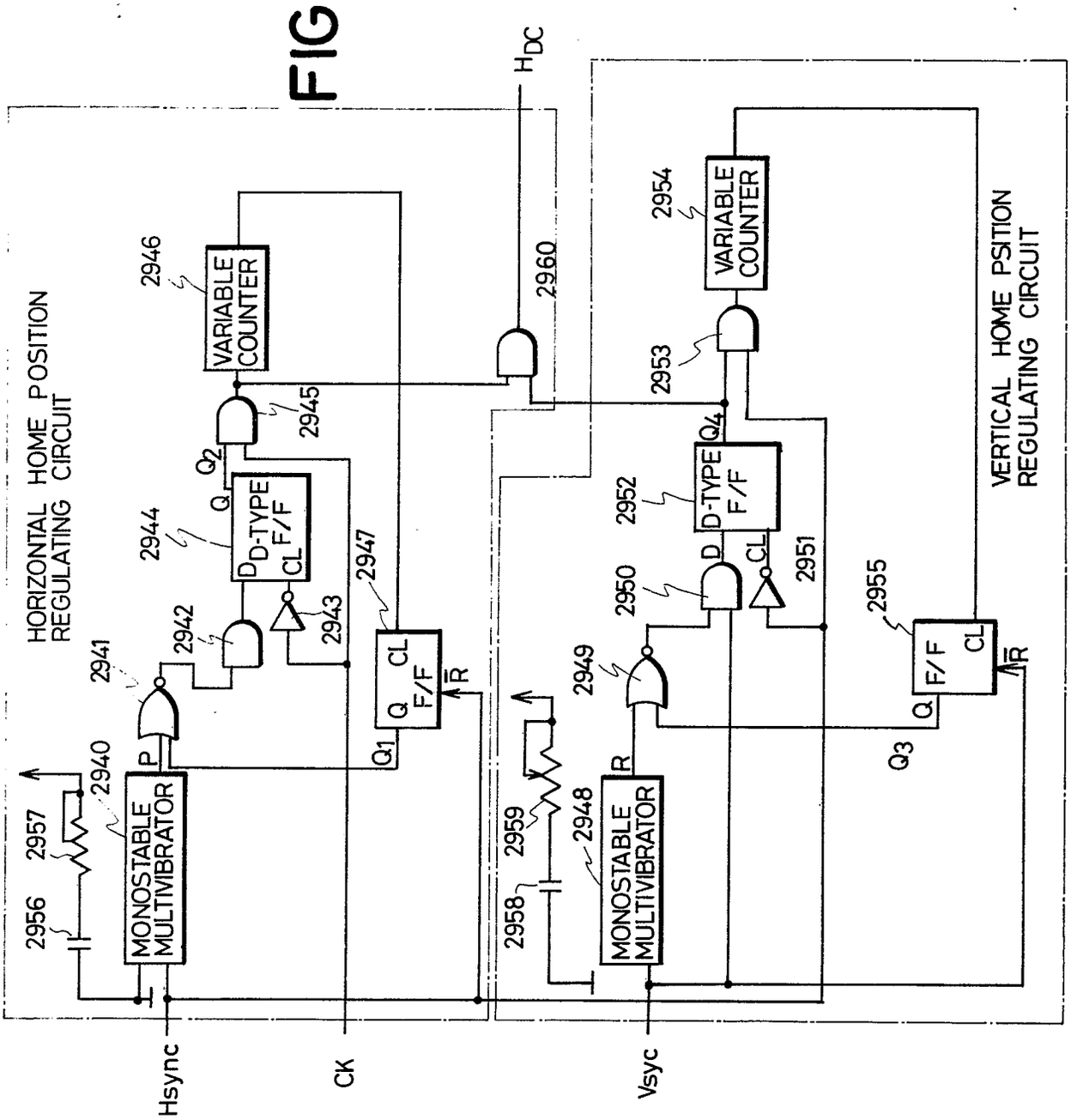

HORIZONTAL HOME POSITION REGULATING CIRCUIT
VERTICAL HOME PSITION REGULATING CIRCUIT
MONOSTABLE MULTIVIBRATOR
VARIABLE COUNTER
D-TYPE F/F
F/F
2940
2941
2942
2943
2944
2945
2946
2947
2948
2949
2950
2951
2952
2953
2954
2955
2956
2957
2958
2959
2960
Hsync
CK
Vsyc
HDC
Q1
Q2
Q3
Q4

FIG.30

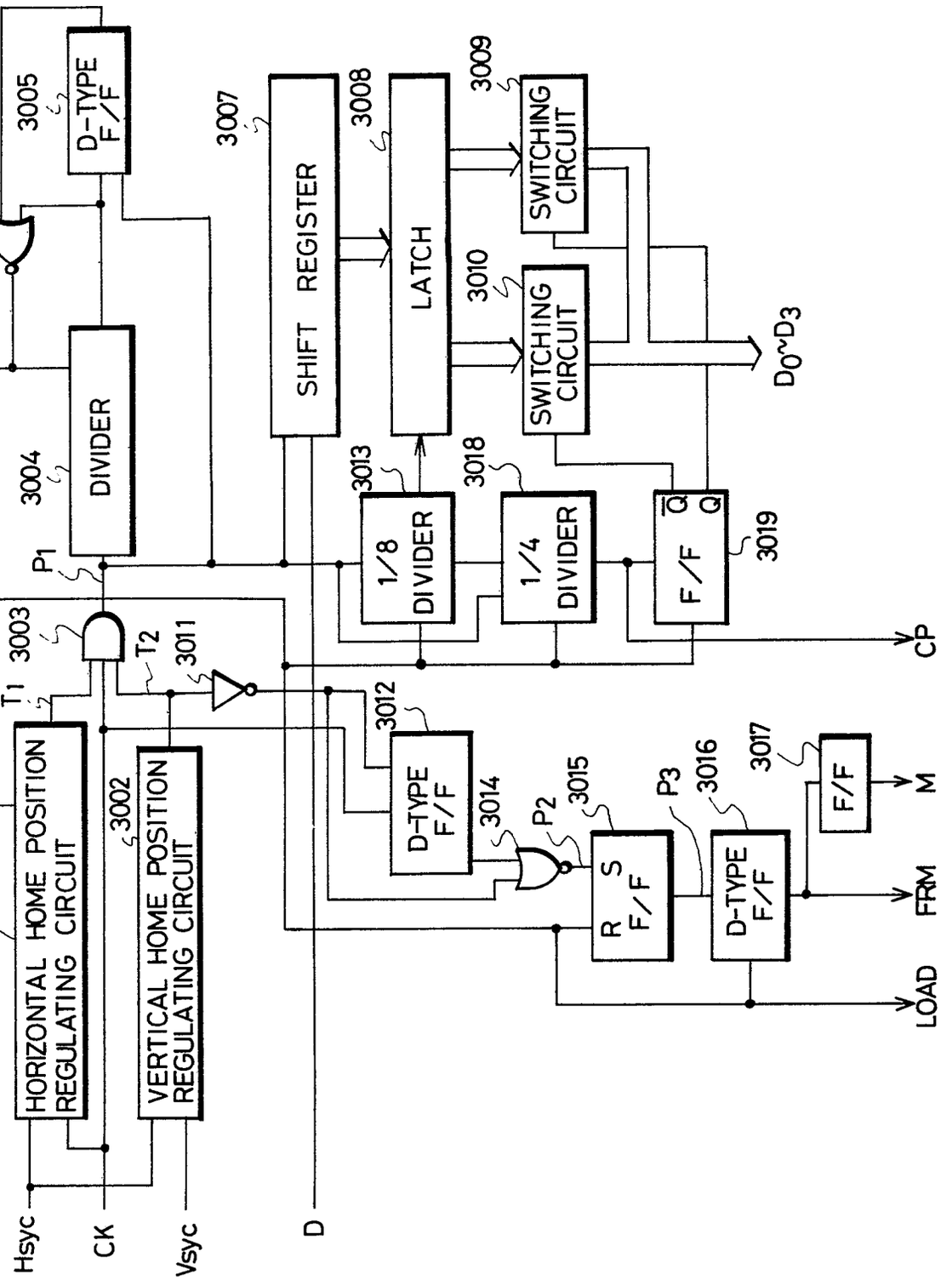

3001
HORIZONTAL HOME POSITION REGULATING CIRCUIT
3002
VERTICAL HOME POSITION REGULATING CIRCUIT
3003
3004
DIVIDER
3005
D-TYPE F/F
3006
3007
SHIFT REGISTER
3008
LATCH
3009
SWITCHING CIRCUIT
3010
SWITCHING CIRCUIT
3011
3012
D-TYPE F/F
3013
1/8 DIVIDER
3014
3015
R S F/F
3016
D-TYPE F/F
3017
F/F
3018
1/4 DIVIDER
3019
F/F
R1
P1
P2
P3
T1
T2
Hsyc
CK
Vsyc
D
CP
M
FRM
LOAD
D0~D3

FIG.31

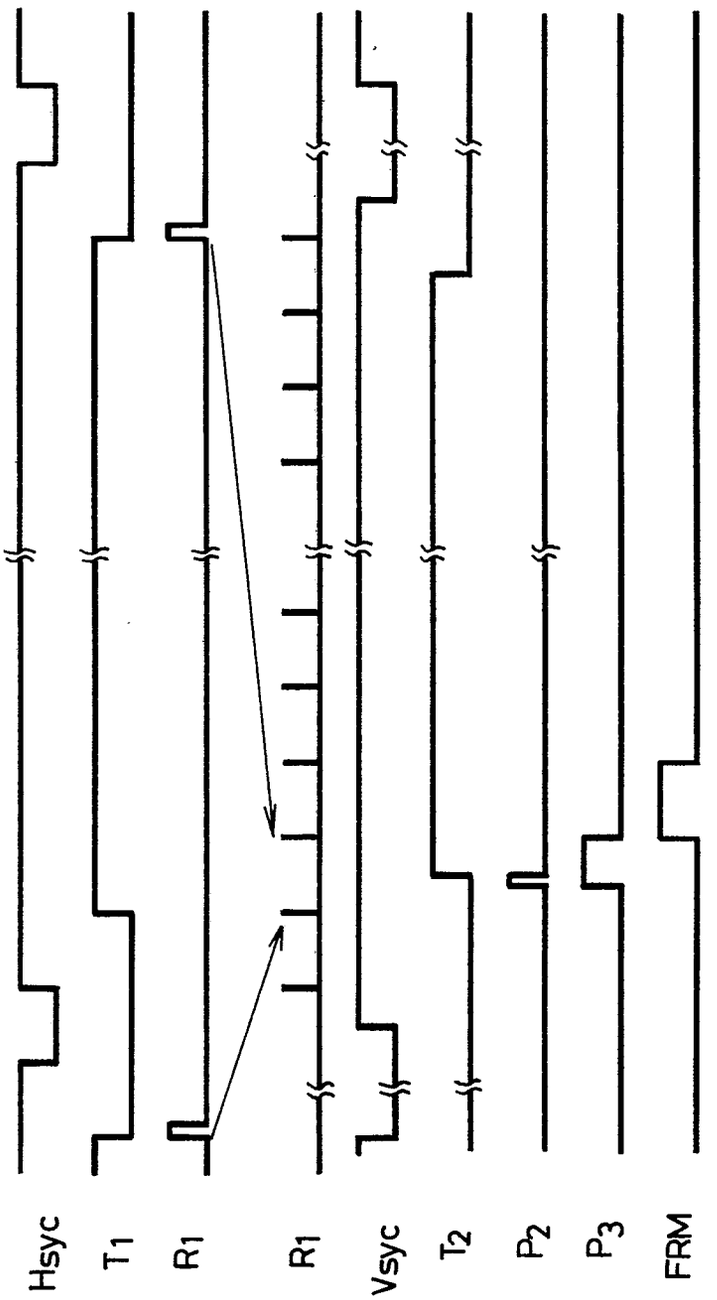


FIG. 32

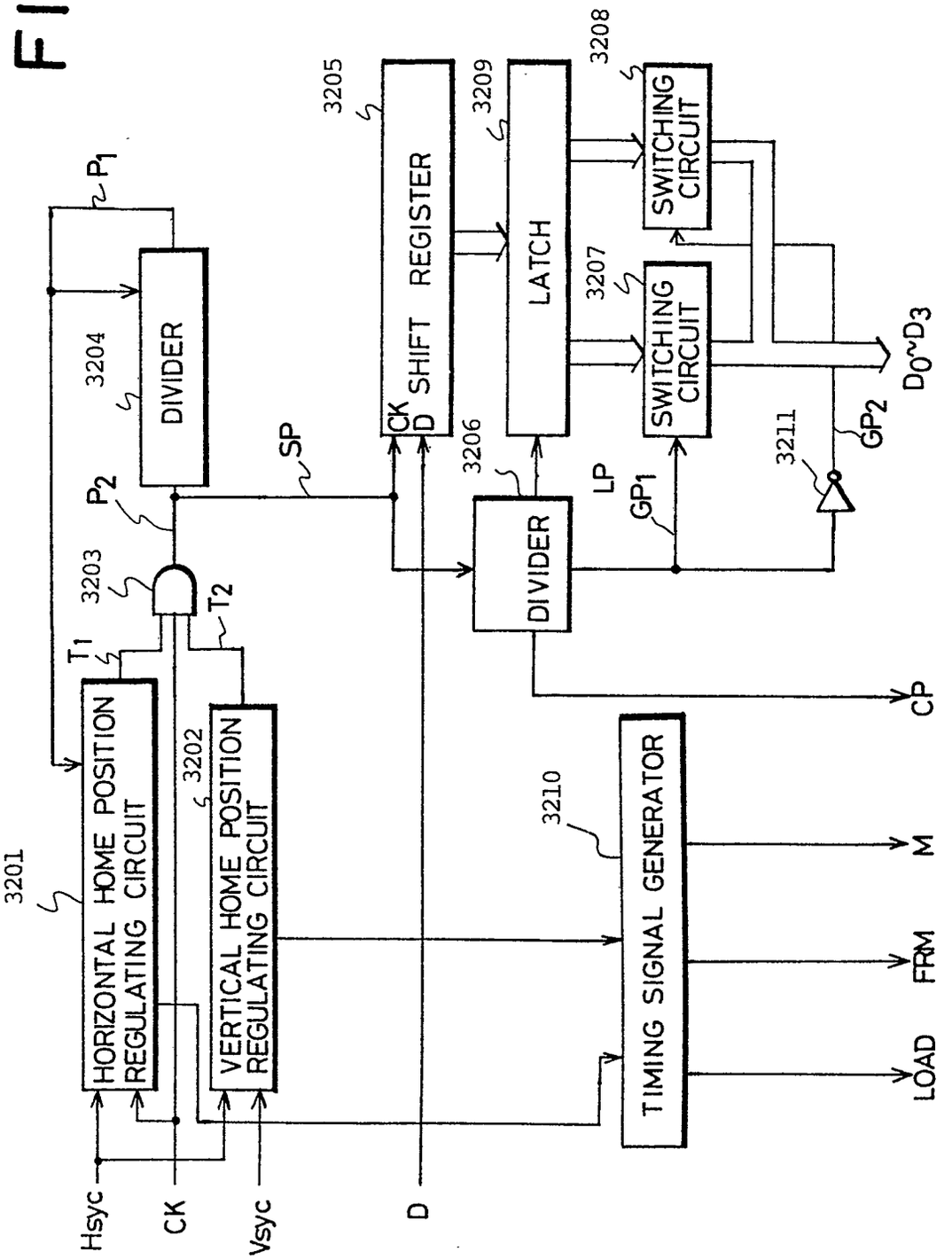

3201
HORIZONTAL HOME POSITION REGULATING CIRCUIT
3202
VERTICAL HOME POSITION REGULATING CIRCUIT
3203
3204
DIVIDER
3205
SHIFT REGISTER
3206
DIVIDER
3207
SWITCHING CIRCUIT
3208
SWITCHING CIRCUIT
3209
LATCH
3210
TIMING SIGNAL GENERATOR
3211
P1
P2
T1
T2
SP
LP
GP1
GP2
CK
D
Hsyc
CK
Vsyc
D
CP
M
FRM
LOAD
D0~D3

FIG.33

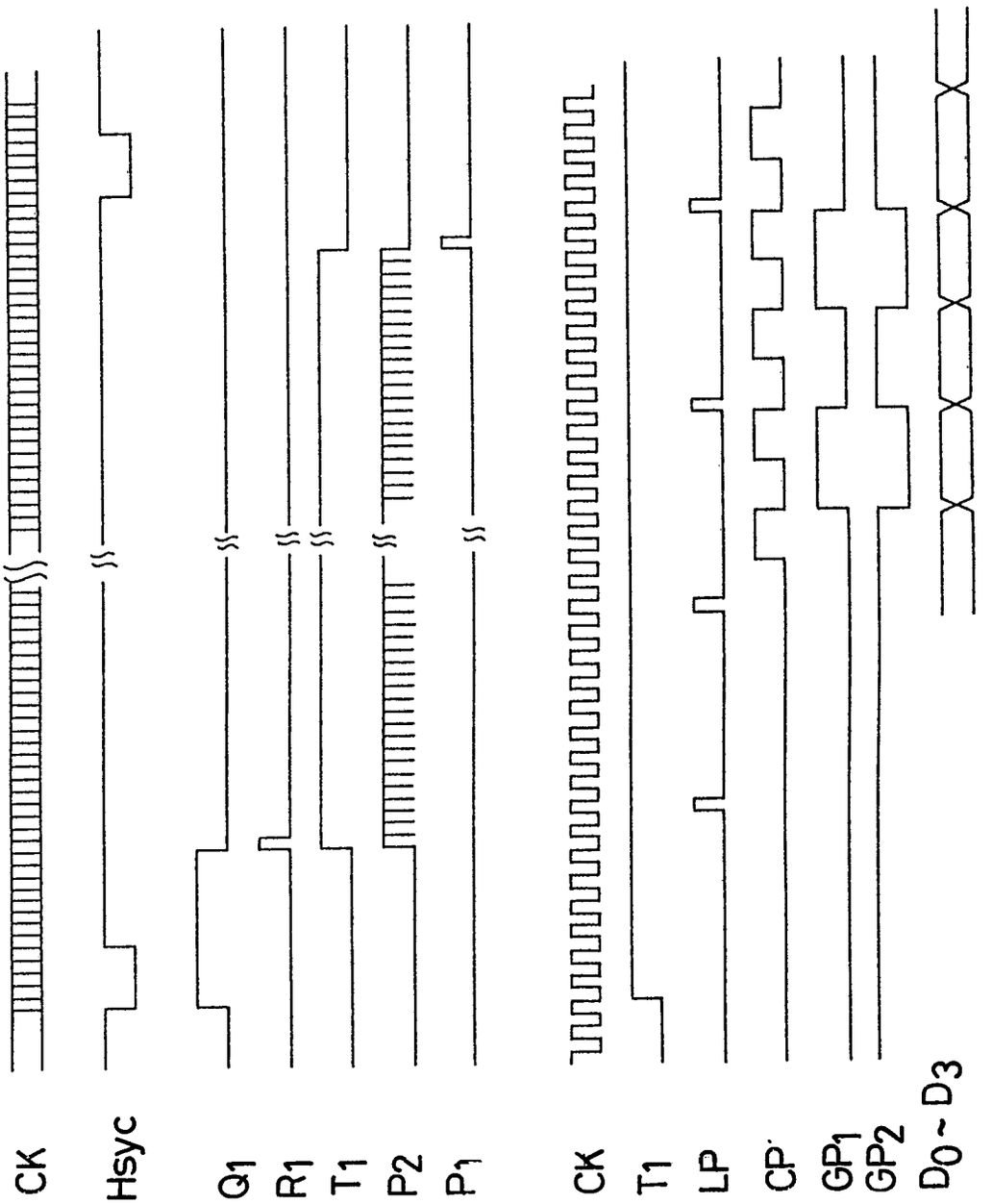
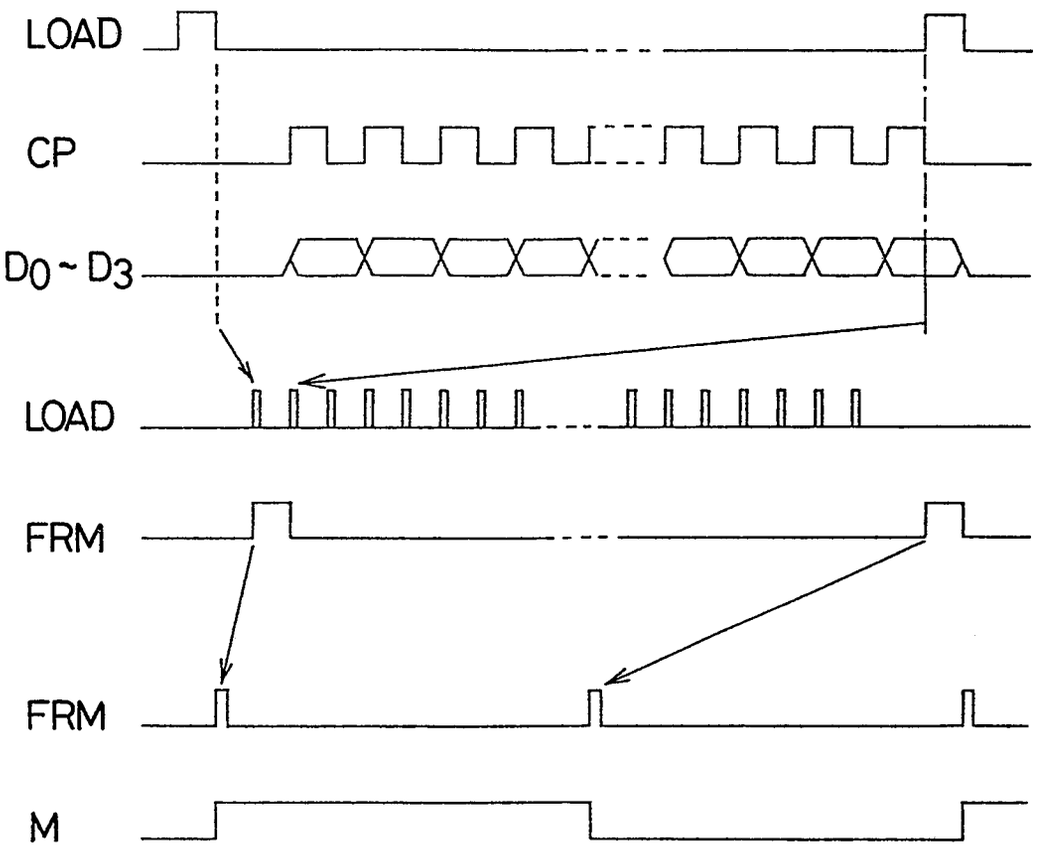


FIG. 34



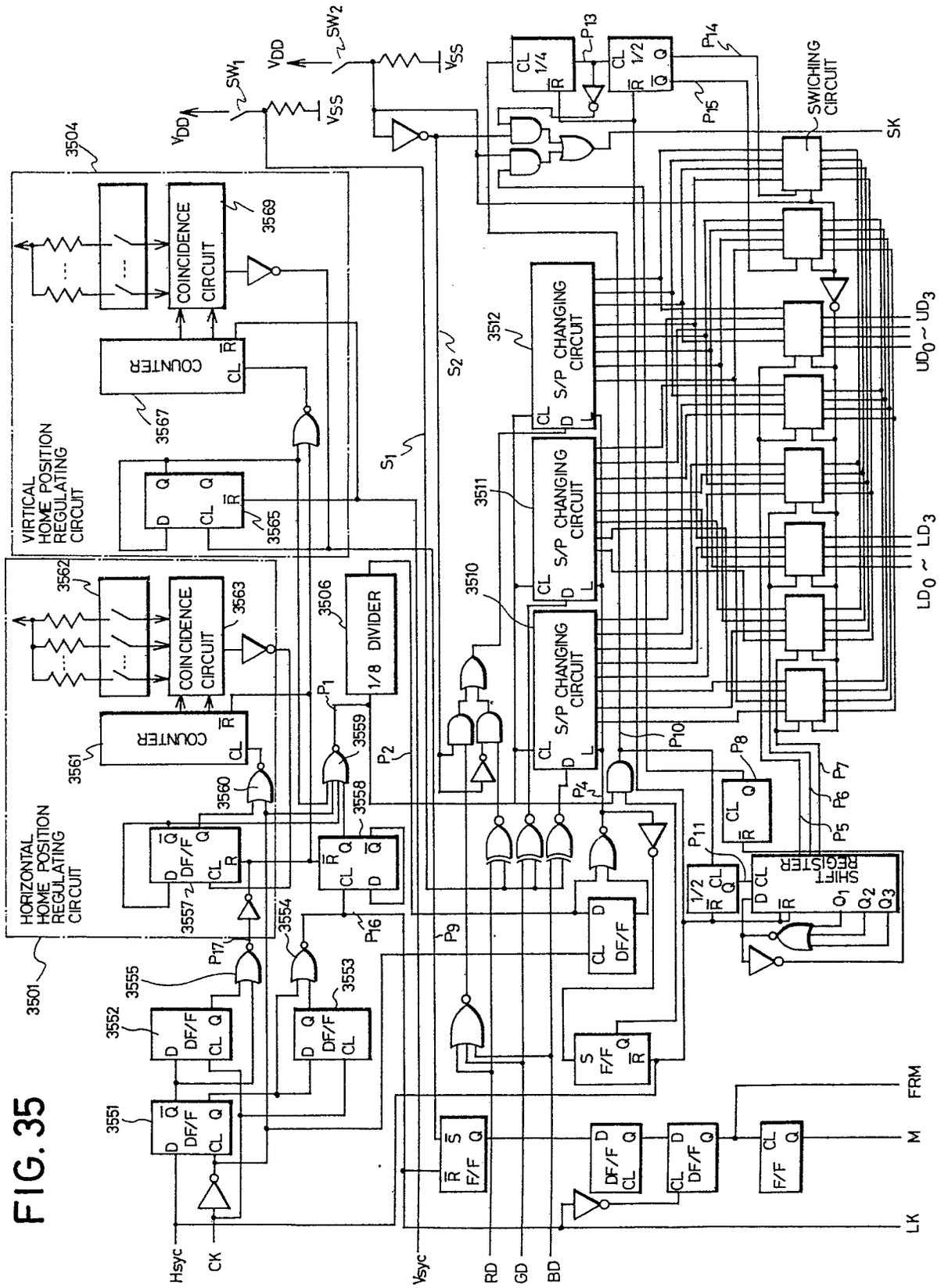
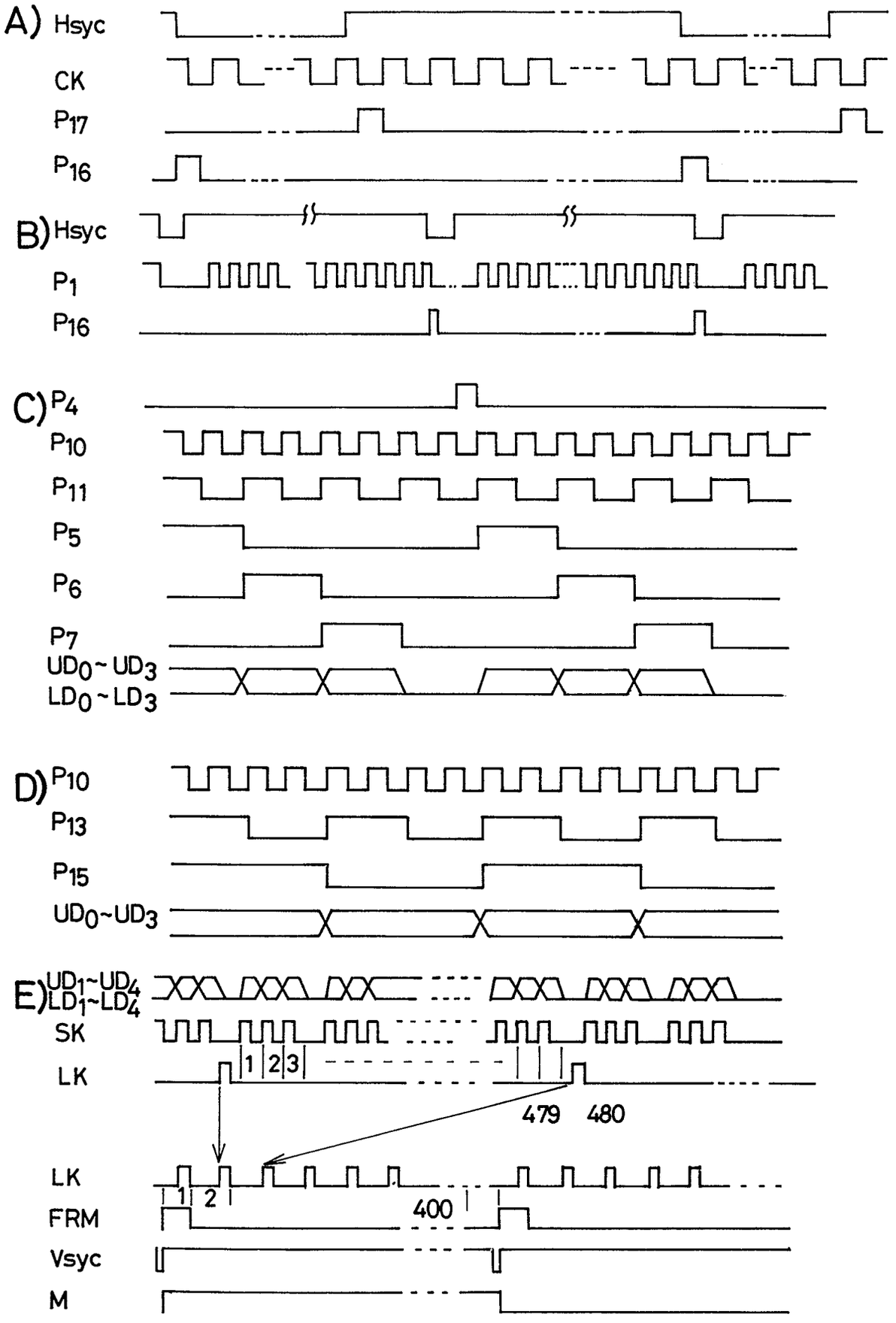

3501
HORIZONTAL HOME POSITION REGULATING CIRCUIT
VIRTICAL HOME POSITION REGULATING CIRCUIT
3504
3506
1/8 DIVIDER
COINCIDENCE CIRCUIT
COUNTER
DF/F
S/P CHANGING CIRCUIT
SWICHING CIRCUIT
SHIFT REGISTER
F/F
1/2
1/4
Hsyc
CK
Vsyc
RD
GD
BD
SK
LK
FRM
M
UD0 ~ UD3
LD0 ~ LD3
VDD
VSS
SW1
SW2

FIG. 35

FIG. 36


A) Hsyc
CK
P17
P16
B) Hsyc
P1
P16
C) P4
P10
P11
P5
P6
P7
UD0~UD3
LD0~LD3
D) P10
P13
P15
UD0~UD3
E) UD1~UD4
LD1~LD4
SK
LK
1 2 3
479 480
LK
1 2
400
FRM
Vsyc
M