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(54) A multiport memory and source arrangement for pixel information.

(57) The present system includes, in a preferred embodiment, a plurality of bit map memory units which together define a large bit map memory. For each bit map memory unit there is also included a mask means and four extended shift registers. The shift registers can be loaded in parallel with pixel information through bidirectional data transmission channels which include bidirectional mask means. The pixel information can be routed through said bidirectional mask means to different address locations, or to the same address location, with certain of the pixel bits removed by the mask means. The shift registers have both serial and parallel input and output mans and are clocked at different speeds to accommodate different peripherals. At least a first shift register is designed to be serially read out at a relatively high rate which can be advantageously used by a video display device or the like. Information signals from the other shift registers are transferred at high speed (in parallel) into and out of the large bit map memory to said first shift register whereby pixel information signals are settled down before being routed from said first shift register. The bidirectional mask means and the bidirectional data transmission channels along with the multiplicity of shift registers permit the present system to handle many varied operations which operate at different speeds.

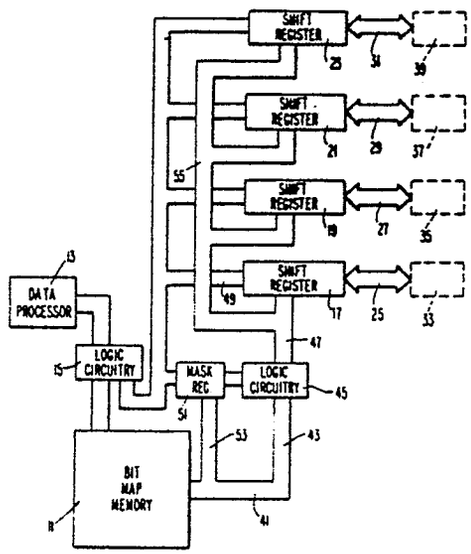

Fig. 1

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A MULTIPORT MEMORY AND SOURCE ARRANGEMENT FOR PIXEL INFORMATION

The invention is described with reference to its use in a video display device but other output devices, such as printers which handle serial information, can employ the present invention.

It is generally the practice in the video display art (in order to display information on a video screen), to store information in a memory device and read said information therefrom into a shift register. The shift register is stepped in synchronism with the scan rate of an electron beam in the CRT. If the pixel information indicates that a dot should be present on the CRT, the beam will be turned on and if the pixel information indicates that a dot should not be present, then the beam will be turned off. In the prior art, video display manufacturers have employed bit map memory devices and in particular bit map memory units formed on integrated circuit chips. The bit map memories have the advantage that for each pixel location on the face of the display means, there is a pixel location in memory. Hence, the pixel information in the bit map memory can be read out to paint the picture, or to paint an alpha-numeric display, on the screen, without necessitating a great number of manipulations of information, and accordingly very rapidly. However, the state of the art has advanced such that pixel information is available (and desirable) from a number of pixel information input means. A major problem is that the pixel information sources operate at different speeds and very often the information signals are burdened with phase distortion, jitter, timing irregularities and the like. If such information is transmitted directly from the source to the video display, the picture provided to the viewer is often unsatisfactory. In addition, with the introduction of high-resolution display devices (including means that provide varying character intensities and color presentations), the operational speeds of the shift registers and memories have been limiting factors. Further, as video display systems have become more sophisticated, demand has increased for high-resolution devices; full-screen scrolling operations; window scrolling operations; the use of multiple video information sources, and the like. Heretofore there has not been a compact, flexible arrangement to accommodate the foregoing demands, particularly an arrangement with the capability of being disposed on an integrated circuit chip. The present system provides a multiport memory means as well as a flexible signal routing means which enables the operations enumerated above, as well as other operations, to be effected. The present system is compact enough to be disposed on an integrated circuit chip.

The present invention provides a large bit map memory to accommodate a high-resolution display means. In a preferred embodiment, the large bit map memory is made up of a plurality of bit map memory units, each disposed on an integrated circuit chip. For each bit map memory chip (in a preferred embodiment) there is included a bidirectional mask means and four shirt register units, each of which is designated to handle pixel information for different purposes. Each of the shift register units has several information input means and output means. The shift register units associated with each bit map memory unit and which are assigned to the same purpose are coupled to one another to form extended shift register means, to accommodate the large bit map memory. Connecting the extended shift register means to the large bit map memory is a plurality of bidirectional data transmission channels, including bidirectional mask means. Accordingly pixel information can be loaded in parallel form from the bit map memory over said bidirectional channels, and alternatively can be read from the shift register means in parallel form to be transferred back into said bit map memory. The extended shift register means can be stepped to be read out serially to a peripheral device or to change the position of the pixel information held therein. Accordingly the pixel information read from the extended shift register means can be returned in a different arrangement to the large bit map memory. In addition, such pixel information can be masked en route and thus only certain pixel bits are loaded into the bit map memory. Alternatively, only certain pixel bits are read from the bit map memory to effect such operations as window scrolling or a split-screen presentation. The present system further includes an arrangement whereby the shift registers are clocked at different speeds to accommodate different input sources, such as different speed peripherals. Through this arrangement, pixel information signals from a peripheral source which are infirmed with phase distortion, jitter, timing irregularities and the like can be loaded into a suitable one of said shift registers. Thereafter the information, in better form, can be transferred through said large bit map memory into a particular shift register which is used to provide signals to a video display device. In a preferred embodiment said particular shift register is designed to be read out at a rate which is very much higher than the shift register units that make it up. This last-mentioned extended shift register operates to be read out at very much higher rates than the remainder of the extended shift register means. The foregoing

high-speed readout enables the extended shift register to refresh and/or paint pictures on a high-resolution display device. At the same time the information read into the high-speed extended shift register can be read into a slower-speed extended shift register and used to provide information to a slower-speed peripheral. The bidirectional mask means enables the system to effect a split-screen presentation, window scrolling, or the like.

The features and objects of the present invention will be better understood in view of the following description taken in conjunction with the drawings wherein:

Figure 1 is a block diagram of the present system;

Figure 2 is a block diagram schematic of the elements found on an integrated circuit chip employed in the present system;

Figures 3A and 3B depict a block diagram - schematic showing four bit map memory units in one plane and the accompanying shift register arrangements therefor;

Figures 4A and 4B depict, in far less detail, the arrangement of three other rows of four bit map memory units and the accompanying shift register arrangements associated therewith;

Figure 5 shows the arrangement of Figures 3A, 3B, 4A and 4B;

Figure 6 depicts the arrangement of a shift register unit used in making up the extended high-speed shift register of Figure 3B;

Figure 7 shows the relationship between 80, 40 and 20 MHz clock signals;

Figure 8 shows the relationship between control signals during a read cycle and a write cycle;

Figure 9 shows the relationship between control signals during a "register to memory" cycle and a "memory to register" cycle; and

Figure 10 shows circuitry to generate certain clock signals.

The preferred embodiment of the present invention is formed on an integrated circuit chip. The technique for producing integrated circuit memory devices, logic devices, active and passive elements and shift registers is well understood in the art of fabricating integrated circuits. Instruction information for fabricating such circuits can be found, for instance, in the text "Physics and Technology of Semiconductor Devices" by Andrew Grove, as well as in the text "Introduction to VLSI Systems" by Carver Mead and Lynn Conway. The present invention resides in the architecture of the circuitry and not in the fabrication of the integrated circuit chip per se. However, since the architecture enables the circuitry to be readily made part of an integrated circuit and enhances the data handling of pixel signals, the use of the present invention as provided in integrated circuit form is a substantial advance in the art.

In the following description, the circuitry and its operation will be described as if the components were hard-wired on a circuit board. Indeed the present system could be a hard-wired set of components, or one or more hybrid circuit boards, and could employ core memories, transistor logic memories, etc. In Figure 2, the elements of the present system which are mounted on an integrated circuit chip are shown. By way of limited explanation of the fabrication of the integrated circuits employed in the present system, it should be pointed out that in order for 256 lines to be arranged as input/output channels, to and from a bit map memory unit, it was necessary to extend the digit lines beyond the physical positions of the decoder circuits found on a commercially available chip. The foregoing is accomplished by employing a technique of etching a polysilicone layer whereby the digit lines are extended.

Figure 1 shows a large bit map memory 11, a data processor 13 and a block of logic and control circuitry 15. In addition, four extended shift registers 17, 19, 21 and 23 are provided, each of which has an input means and an output means as depicted by the double-arrowed channels 25, 27, 29 and 31. Channels 25, 27, 29 and 31 are respectively connected to peripherals 33, 35, 37, and 39 (denoted by dashed lines to indicate that they are not part of the invention).

The overall system of Figure 1 operates as follows. Information to be shown on a high-resolution video display 33, can be transmitted from the data processor 13 by way of the logic circuitry 15 to the large bit map memory 11. Said information thereafter can be addressed by the data processor 13 and transferred along channels 41 and 43, through logic circuitry 45, along channel 47, to the shift register 17. Shift register 17 is conditioned to accept said information by control signals on channel 49. Thereafter the shift register 17 serially transfers said information along channel 25 to the high-resolution video display 33.

If the information just described represents window information, i.e. less than a whole screen display, then some of the information bit signals are inhibited by logic circuitry 45 and other bit signals are passed. This partial inhibition is effected by masking information in the mask register 51. Prior to passing the information from the large bit map memory 11 to the shift register 17, the system, under the direction of the data processor 13, transfers masking data from the bit map memory 11 to the masking register 51 along channels 41 and 53. Thereafter, and in response to control

signals from the logic circuitry 15, the masking information is transferred to logic circuitry 45 and controls certain gates therein to inhibit the flow of certain bit signals therethrough, to effect the window display.

The shift register 19 is arbitrarily assigned to handle pixel information for a slow-speed video display 35. Information to be shown on the slow-speed video display can be loaded into the shift register 19 from the data processor 13 by way of the bit map memory 11 from any of the shift registers 17, 21 and 23, a transfer of said information into and out of the large bit map memory; or from an outside peripheral connected to its serial input means.

The shift register 21 has been arbitrarily assigned the role of accepting information signals from a slow-speed source, such as a disk, camera, tape or the like. If the information received by the shift register 21 were to be displayed on the low-speed video, it would be transferred to the shift register 19 along a route (composed of channels 55, 47, 43 and 41) into and out of the bit map memory 11, in a fashion similar to that just described. If that information were burdened, as often is the case, with phase distortion, jitter or timing irregularities, such information would be loaded into the shift register 21 and held there momentarily while the irregularities settled down. Thereafter that same information would be transferred in good form as just described, to be seen on the low-speed video display 35. If such information were intended to be seen on the high-resolution video display, the information would be transferred to the shift register 17.

The shift register 23 has been arbitrarily assigned to handle information which is going to be used in scrolling presentations or window presentations. The shift register 23 can be activated to shift right or left, and hence information bits which need to be located in new positions in the right or left sense are manipulated in this shift register. As will be explained in more detail hereinafter, to effect a scrolling operation, information is loaded into the shift register 23 from a certain address in the bit map memory 11 and is returned to the bit map memory at a new address so that the viewer sees the text, or picture, gently moving up (and possibly off) the screen.

Figure 2 shows the system elements coupled together on an integrated circuit chip. The elements shown in Figure 2 are the same as those shown in Figures 3A and 4A to be discussed below. However, some differences should be noted. Figure 2 shows a mask register 57 associated with the shift register units 64, 65, 67 and 69. In the system there is one mask register for each chip and hence for each vertically (in the drawings) associated set of four shift register units. However, in the description of figures 3A and 4A only one mask register is discussed. Only one mask register is shown to simplify the drawing but theoretically the system operates in the same manner with the one mask register as it would with four mask registers. Each chip also has an RA latch, a CA latch and a decoder. The description of Figures 3A and 4A discusses only one such RA latch 59, CA latch 61 and decoder 63, however the arrangement would be the same if four of each were used.

Figure 3A shows a preferred embodiment with four bit map memory units 71, 73, 75 and 77, which are similar to the integrated circuit chips manufactured by Micron Technology Corporation and designated as MT4264 but are altered as described above and as shown in Figure 2. Each bit map memory unit has 256 columns and 256 rows. In the present system a total of sixteen bit map memory units are employed, as shown in Figures 3A and 4A. Figure 4A shows bit map memory units 78 through 89. The bit map memory units 71, 73, 75, 77 and 78-89 together represent a large bit map memory having 1024 rows and 1024 columns. Actually, the preferred embodiment accommodates a high-resolution display device 91, shown in Figure 3B, which has 1024 column positions and 660 row positions. It should be apparent that the large bit map memory formed by the interconnecting of the bit map memory units actually has some positions which are "offscreen". In other words, rows 661 through 1024 contain information which does not appear on the screen during a display. That information is used to effect operations such as masking and font character storage.

As can be seen in Figures 3A and 4A, the bit map memory units each contain two logic means for decoding as well as a logic means to effect read/write (write enable) operations. As depicted in Figure 3A, the logic circuitry to the right decodes the column addresses, while the logic circuitry to the left decodes the row address information. The decoding logic circuitry, as well as the write enable logic circuitry, is part of the commercially available bit map memory (mentioned above) and no further description of such an operation is deemed necessary. Although the embodiment presented herein is related to a high-resolution display having 1024 columns and 660 row positions, in accordance with the invention other configurations could be used. Also other bit map memory unit sizes could be employed.

The data processor 93 may be any well-known data processor having the capability of being programmable, handling such programs, and providing data information, instruction information, and address information. If we assume that the data processor has been programmed to transfer informa-

tion into the large bit map memory, then the information will be loaded into the bit map memory at some column address and some row address and accordingly the data processor 93 will transmit both column address signals and row address signals to the buffer 95. Part of the address signals will be transmitted from the buffer 95 to the row address (RA) latch 59 and to the column address (CA) latch 61 through the multiplexer (MUX) 97. Two bits of the row address are sent directly to the decoder 99 while three bits of the column address are sent to decoder 101. MUX 97 can be any well-known multiplexer such as a 74F157 manufactured by Fairchild Semiconductor Corporation.

The multiplexer 97 separates the column address signals and the row address signals. The column address signals are transmitted to the CA latch 61, while the row address signals are transmitted to the RA latch 59. The latches 59 and 61 can each be a 74F374 manufactured by Fairchild Semiconductor Co. or a similar device. A row address strobe (RAS) signal is transmitted from the timing generator to the RA latch 59 and a column address strobe (CAS) signal is transmitted to the CA latch 61. In a preferred embodiment the address information comprises a 20-bit address on line 107. Bits 0 through 6 of the address are decodable to provide the column address. Bit 7 indicates whether the system is in a random access mode or a register mode of operation. Bits 8 and 9 used to determine which of the bit map memory units is to receive the column address information. The second ten bits of the address information include bits 10 through 17 to determine the row address within the bit map memory, and bits 18 and 19 to determine which one of the rows of bit map memory units, such as the rows starting respectively with bit map memory units 71, 78, 82 and 86, is to receive the row address information. The system needs only 7 bits to determine the column address but needs 8 bits to determine the row address because the data processor 93 transmits (or reads) two bits for two column positions, at one time, in response to a single column address. In other words, if the column address is "zero", one bit in column 1 and one bit in column 2 will be transmitted to or selected from the bit map memory. If the second column address is "one", a bit would be transferred to or from both selected columns 3 and 4. The two-column bit pattern continues throughout the column addressing. Hence, if there are 1024 column bits to be accommodated, it is only necessary that 512 addresses be available, which requires only 7 bits.

The 20-bit address signals are transmitted on line 107 to the MUX 97. The MUX 97 is controlled by a delayed RAS signal. When the delayed RAS signal is not present, bits 10 through 17 are transmitted to both latches 59 and 61. However, only latch 59 will be enabled to store the bits 10 through 17. Latches 59 and 61 only respond to leading edge changes in control signals. When the delayed RAS signal is present, bits 0-7 are transmitted to both latches 59 and 61. However, only latch 61 will be enabled (by the leading edge of the CAS signal) to store bits 0 through 7. Bits 7, 8 and 9 are transmitted on line 109 to the decoder 101. If the bit 7 is high, then all of the column lines are activated because bit 7 in its high form indicates a register mode and hence every bit in the row selected by the row address should be transferred from the bit map memory unit. If the bit 7 is low, the system is in a random access mode and the column of bit map memory units selected by decoding bits 8 and 9 receives the column address signals from latch 61. Accordingly the decoder 101 transmits one of four signals on the lines H, J, K and L, which lines respectively go to logic gates 111, 113, 115 and 117. Hence one of those gates is fully enabled and passes the CAS signal, which in turn causes the logic within the bit map memory unit to permit bits 0-6 to select a column address in the correct bit map memory unit.

In a similar manner the eight bits 10 through 17 which make up the row address are transmitted to the latch 59 as described above. The bits 18 and 19 are separately transmitted on line 119 to the decoder 99. In a manner similar to that described for the column address signals, the row address signals are transmitted from RA latch 59 to the decoders of the respective bit map memories 71, 73, 75 and 77. At the same time such row address information is transmitted to similar logic gates associated with the bit map memory units 78 through 89. The same row address information will be sent to each of the bit map memory units in a row. The large bit map memory includes (collectively) the 256 bits of each of the bit map memory units 71, 73, 75 and 77 to provide 1024 column positions.

The decoder 99 provides enabling signals A, B, C and D to the bit map memories, which signals determine which one of the rows of bit map memory units will respond to the row address information. For instance, the A signal to logic circuit 121 permits the RAS signal to pass to the internal logic, which causes the bit map memory unit 71 to respond to the row address signals at decoder 123.

Two lines 125 are connected to the data processor 93. The designations DI/01 and DI/02 stand for data input/output one and data input/output two. The present system uses a two-bit simultaneous input from the data processor for two reasons. First, the data processor is a 16-bit word data processor. Second, in the preferred embodiment, instead of one plane of bit map memory units (as

shown in Figures 3A and 4A), there are eight planes in order to accomodate variations in picture intensity and the need to provide color presentations. Since there are eight planes and there are sixteen bits available in a single word transmission, it follows that two bits are available for each bit map memory plane. As stated before, for a single column address two bits can be written or read as directed by the data processor. In Figure 3A, the DI/01 and DI/02 signals are transmitted over the lines 125 to the lines 127, 129 and 131, and then to each bit map memory unit. The information from lines 125, going to the bit map memory units, is available to each pair of column lines in each bit map memory. However, only the column lines selected by the column address actually participate in the read or write operation. This procedure is well understood in the data processing art and no further description of that operation is necessary. In the large bit map memory there is a position for every pixel position on the high-resolution screen of device 91. The information to paint that display can be read into the bit map memory from the data processor through the DI/01 and DI/02 lines.

Channels 133, 135, 137 and 139 are respectively connected to bit map memories 71, 73, 75 and 77. Each of these channels is made up of 256 lines so that during readout from a bit map memory unit, 256 bits can be read onto the channel and transmitted therefrom to the shift register structure as shown in Figure 3B. If readout of the row of bit map memory units in Figure 3A is to be effected, then the row address signals will be transmitted to the bit map memory, in particular to decoder 123 as well as the column address bit 7, equal to a logic ONE. The write enable signal transmitted to the logic circuitry 141 will be high to effect the readout. In addition, the logic circuitry 121 will be fully enabled. The 256 bits will be transmitted over channel 133 to the two logic circuit blocks 143 and 145. If the information read from the bit map memory unit 71 is "mask information", then logic circuitry 143 will be enabled by a signal on line 147, and the 256 bits will be transmitted into the mask register 57. Such mask information will be used to condition a plurality of gates (during the presence of a control signal on line 149) in the logic circuit 145 to enable certain of the signals on channel 133 to be transmitted therethrough and to inhibit the remaining signals. While the same information is transmitted through the gates 145 and along the channel 151, none of the logic circuits 153, 155, 157 and 159 will be enabled to transmit that information therethrough to the associated shift register units.

If, on the other hand, the readout from the bit map memory unit 71 is for some other purpose (e.g., to store information in the shift register unit 64), then logic circuit 153 would be conditioned by a signal on line 161 to transmit that information therethrough and the 256 bits would be loaded, in parallel, into shift register unit 64.

The 8-bit address signals (bits 0-7) transmitted to the column address latch 61 serve a multiple purpose. In one mode these signals are column address signals, while in another mode these signals are decoded to determine which shift register will receive information; whether the mask register 57 will receive mask information; whether the mask information is to be used at logic circuit 145; and which direction, right or left, shift register 163 is to be shifted. Seven lines 165 leave decoder 63. The signals on those lines are generated in response to the decoding of bits 0-7 of the column address information which are transmitted to the column address latch 61. If bit 7 is a ONE, decoder 63 will provide signals on lines 165. The bit 7 signal also renders all of the column lines active. When the data processor is effecting a readout from the bit map memory to the shift register, it also takes into consideration which shift registers that information is to be transmitted to. For instance, if such information is to be transmitted to shift register unit 64, then the bits transmitted to decoder 63 will be decoded to provide a signal on the enable line 161 which will enable logic circuitry 153 to transmit the 256 bits to shift register 64. The enabling or control signals on lines 147, 149, 167, 169, 171, and 173 are generated in a similar manner to that described for the enabling signal on line 161. The decoder 63 is shown as having output lines to each of the logic gates connected to the shift register units. There is a decoder 63 on each integrated circuit chip, as shown in Figure 2. Each integrated circuit chip also has its own RA latch 59 and CA latch 61.

The shift register units are arranged to form extended shift registers. The extended shift register made up of shift register units 64, 175, 177 and 179 is the high-speed extended shift register 181. Adjacent shift register units are coupled by two lines. The structure of one of the shift register units is shown in Fig. 6. A 20-MHz clock signal is transmitted on line 183. (Figure 7 shows the relationship between the 20, 40 and 80 MHz clock signals.) Figure 6 shows four shift register subunits, each of which has 64 bits of information therein. Together the four shift register subunits act as one shift register unit which is capable of handling 256 bits.

The contents of shift register subunits 185, 187, 189 and 191 can be read out in response to a 20-MHz clock signal on line 183. The shift register subunits 185 and 191 respond to the leading edges 197 of the 20-MHz clock signal (see Figure 7) by

shifting one bit position at a time, respectively, onto lines 193 and 195. The trailing edge 198 of the 20-MHz clock signal (Figure 7) is inverted at the inverter 199 (Figure 6) to provide a leading edge signal to the shift register subunits 187 and 189, in response to which one bit position is shifted at a time, respectively, onto lines 201 and 203. A bit signal on line 201 is immediately transmitted through the MUX 205 to output line 207 at the time when the leading edge 197 arrives. The MUX 205 receives the bit signals present on line 193 at the time when the trailing edge 198 arrives so that the signals output on line 207 appear at a rate of 40 MHz, as indicated by the trailing edges 209 and 211 in Figure 7. The times of the trailing edges 209 and 211 are the times that respective signals from shift register subunits 185 and 187 appear on line 207. Accordingly shift register subunits 185 and 187, although they are clocked out at a 20-MHz rate (in the arrangement shown in Figure 6), provide a 40-MHz output train of signals on line 207. In a similar manner the shift register subunits 189 and 191 are clocked to provide a train of bits on line 213 which are transmitted at a 40-MHz rate.

Figure 6 also shows terminals 215 and 217. Terminal 215 is connected to transmit information to shift register subunits 185 and 187. The information is clocked into those subunits by the 20-MHz clock signal as just described. In a similar manner terminal 217 is connected to transmit information to subunits 189 and 191, which information is clocked into those shift register subunits as described above. The output signals on lines 207 and 213 are connected to terminals in the next shift register unit similar to terminals 215 and 217. The above-described arrangement can be seen in Figure 3B1 in which shift register unit 64 is shown connected through two lines to shift register 175, which is in turn connected through two lines to shift register unit 177, and so forth. The two lines in Figure 3B1 are similar to lines 207 and 213. Hence signals being transmitted into the shift register subunits are being transmitted at the rate of 40 MHz, but since they are only clocked at 20 MHz, the train of bits coming in at 40 MHz is actually clocked into the respective subunits at 20 MHz. The bit signals are clocked out of those subunits, as just described, at 40 MHz through the respective MUX devices. In Figure 3A, each shift register units includes the MUX device as well as the inverter of Figure 6. The final output signals on lines 219 and 221 (in Figure 3B2) are transmitted to an ECL shift register 223 (for example 10141 manufactured by Fairchild Semiconductor Company). The ECL shift register 223 operates such that in response to the leading edge of a signal on the F terminal, with the E terminal low, the ECL logic will load a bit signal from line 219 onto the output line 225. On the other hand, in response to the leading edge of a signal on the F terminal, with the E terminal high, a bit signal from line 221 will be shifted onto line 225. The signal connected to the F terminal is at 80 MHz and that connected to the E terminal is at 40 MHz. The ECL shift register will load bit signals from line 219 as well as from line 221, via the logic within the block, onto the output line 225. At the leading edges 227 and 231, the bit signals from line 219 are transferred to line 225, whereas at the leading edges 229 and 233 the bit signals from line 221 are transferred to line 225. Hence the output on line 225 is an 80-MHz train of bit signals, which is a rate sufficient to accommodate the high-resolution display device 91.

Figure 4B shows the other three high-speed extended shift registers, which provide the same kind of outputs as are available on line 225 (Figure 3B2) on lines S, U, and W. The 80-MHz output signals on line S, U, and W are transmitted to the MUX 235 and therefrom to the high-resolution display device 91. The MUX 235 is controlled by the output of decoder 237 by way of latch 238, which passes the control signals in response to the enable signal on line 161. The output from decoder 99 selects which of the rows of bit map memory units is to be operative. Hence, the output from decoder 99 selects which of the lines S, U or V is to be selected by MUX 235. The enable signal on line 161, as explained above, indicates that the high-speed shift register is addressed. Accordingly, although the extended shift register is clocked at a 20-MHz rate, it has an output at 80-MHz which provides bit signals having the density necessary to accommodate the high-resolution display device 91.

The output signals on channel 133 from bit map memory unit 71 will be discussed by way of example, although the other bit map memories operate in a similar manner. If the user of the system decides, through the data processor, that the information should be transmitted into shift register unit 65 (Figure 3B1), then the 256 bits transmitted along channel 151 are routed to the logic circuit 155. Logic circuit 155 is enabled by enabling signal 167 and hence the 256 bits are parallel loaded into shift register unit 65. Each of the extended shift registers has a different clock input labelled G, P, N or M, these clock signals being at different clock rates depending upon the use of the extended shift register. In a preferred embodiment the clock signal P, N, and M have respective rates of 22, 14 and 25 MHz. The clock signals P, N, and M are generated by timing circuits 239, 241, and 243 (Figure 4B), which can be similar to the circuit shown in Figure 10. Timing circuit 241 generates a

sync 1 signal which can be used with an input device connected to terminal 245 (Figure 3B1). Timing circuit 239 generates a sync 2 signal which is used with display device 247.

The shift registers 249, 251, 253 and 255 are series-connected to form extended shift register 257, which is in general assigned the job of providing relatively low-speed output information to a low-resolution data display device 247. Corresponding sets of slow-speed shift registers provide video output signals to low-resolution device 247. The output from these other low-speed shift registers are input on lines R, T, and V to MUX 259, which is controlled by the output of decoder 261 passed to latch 262. Latch 262 provides the control signals in response to the enabling signal 167. The control operation is similar to that discussed with respect to the control operation of MUX 235.

If the same information is transmitted to the high-speed extended shift register 181 as well as the low-speed extended shift register 257, then the resulting displayed information can be viewed on both the high-resolution device 91 and the low-resolution device 247.

Shift register units 67, 263, 265, and 267 (Figures 3B1 and 3B2) are serially connected to form extended shift register 269. The shift register units are shifted in response to the clock signals N. The shift register unit 67 has an input line connected to terminal 245. The extended shift register 269 receives video input information from a video tape recorder, disk, or camera, and makes that information available to the low-resolution display device 247, the high-resolution device 91, or the data processor 93. As previously mentioned, information coming from a video tape recorder, disk or camera has time relationship problems and by loading such information into the extended shift register 269, before transferring it for ultimate use, these problems can be overcome. since channels 133 and 151 and logic circuitry 153, 155, 157, and 159 are bidirectional devices, input information from terminal 245 which is serially loaded into shift register units 67, 263, 265, and 267 can be parallel transferred into and out of the bit map memory to other shift registers. For instance, if the information in shift register unit 67 is to be transferred to the low-resolution device 247, the logic circuit 157 will be conditioned to transfer in parallel the 256 bits from the shift register unit 67 onto channel 151, through the bidirectional mask gate 145, and back to the bit map memory unit 71, where the bits are loaded at addresses determined by the row address information on line 60. Thereafter in a subsequent cycle, the information will be read from the bit map memory unit 71, along channel 133, through the bidirectional mask logic 145, along channel 151, to the gate 155. The gate 155 is enabled to load the information into the shift register unit 65. Hence the information which was in the shift register unit 67 has been loaded into the shift register unit 65 and can be serially clocked therefrom to the low-resolution display device 247. All of the shift register units and equivalent logic devices in Figures 3 and 4 operate in this manner.

Finally, the shift register units 69, 271, 273, and 275, which can shift the information held therein to the right or left, form an extended shift register 163 which effects a scrolling operation. These shift registers may, for example, be the 74S299 type manufactured by Texas Instruments Corporation, which are tri-state, bidirectional shift registers having an output enable terminal, a load terminal, a clock terminal, and a serial input terminal. When a "memory to register" cycle is in effect, the load terminal receives a signal from decoder 63 while the output enable terminal receives a high WE signal. During a "register to memory" cycle the load terminal again receives a signal from decoder 63 while the WE signal to the output enable terminal goes low. The logic circuitry shown associated with each shift register is part of the circuit design of such an integrated circuit chip.

In a scrolling operation the viewer sees, for instance, a line of text on the screen of a CRT and that line of text gently moves up and possibly off the screen. Sometimes this is a necessary operation if the screen cannot accommodate a full document to be viewed. The scrolling operation is accomplished by having the information rows, which are going to be moved up on the screen, read from the present bit map memory locations. That information is transferred along the channels (e.g. channels 133 and 151) to the shift registers 69, 271, and 275. Obviously in order to effect that transfer, the logic gates (e.g. logic gate 159) must be conditioned to permit the 256 bits to be transferred from channel 151 to shift register unit 69. The foregoing would also be true for the shift register units 271, 273, and 275. The next step would be to fetch the information from the extended shift register 163 and return it to the next higher row address in the bit map memory. This procedure would continue for each row of information of the text which is being scrolled. Accordingly the viewer will see text on the screen, each line of which was at a lower line a moment earlier. In the present system the time required to transfer 256 bits from the bit map memory unit 71 to the shift register unit 69 and back to the bit map memory at a new location is approximately 800 ns. Accordingly a whole page of text can be readily scrolled.

If the system were required by the user, through the data processor, to effect a window scroll, that is, a scrolling of only a part of a text or graphic display, then only the rows of information

corresponding to that portion of the display to be window-scrolled would be transmitted from the bit map memory to the extended shift register 163. However, prior to transmitting that information to the extended shift register 163, the mask register 57 would be loaded with a pre-determined set of mask bits so that only a portion of the row information, i.e. only the "window", made up of certain bits in certain columns, would pass through the logic circuitry 145. The window bits would be transmitted to the correct shift register units of extended shift register 163. Accordingly when the selected bits (i.e. the window bits) are returned from the extended shift register 163 to the bit memory unit 71, they are located at new addresses to effect scrolling and therefore the viewer would see only the window bits being scrolled. A similar operation would take place if a split-screen presentation were to be performed. For instance, if there were a window on the screen which was to have a different display than was present in the bit map memory, then "new" window information could be transferred (from some location in memory such as from the off-screen section) to the extended shift register 163. The new information to be displayed as the split-screen or window presentation could be read from the extended shift register 163 back into the addresses corresponding to the window.

Although the extended shift registers have been assigned specific tasks, they can be interchanged because they have similar hardware arrangements.

Figure 8 depicts the relationship between the RAS signals, the CAS signal, the address signals, and the WE signal for both the read and write cycles. As is shown in Figures 2 and 3A, each bit map memory unit has internal logic circuitry which responds to the WE, RAS and CAS signals. While a number of operations can be accomplished in response to different combinations of these signals, in the present description we shall only be concerned with the read, write, register to memory and memory to register cycles. If a WE signal is high before the CAS signal goes low, then the logic circuitry of a bit map memory unit (such as logic circuitry 141 of bit map memory 71) will cause the bit map memory unit to read out information. If at the time of a read cycle bit 7 of the column address is low, then the read-out is on the DI/01 and DI/02 lines. The relationship of the WE signal to the CAS signal is shown in the upper half of Figure 8. On the other hand, as shown in the lower half of Figure 8, if WE goes low before CAS goes low, then a write cycle is in effect. If bit 7 of the column address is low, the information written into the bit map memory unit comes from the DI/01 and DI/02 lines.

In Figure 9 the relationship between the RAS, CAS, and WE signals and the address signals "ROW" and "Register" is shown to effect a transfer of information from the shift registers to the bit map memory units and vice versa. According to Figure 9, if the WE signal goes low before the CAS signal goes low, there is a transfer of information from the shift register to the bit map memory. Such an operation would be a write-in to memory. However, in a register to memory cycle shown in Figure 9 the address available is the register address, i.e., the address signals from the column address latch 61 as decoded by decoder 63. At the time of the register to memory cycle, bit 7 is high which enables the decoder 63 to provide the register address signals (i.e. the enabling signals).

The lower half of Figure 9 shows the waveform for a memory to register cycle. If WE goes high before CAS goes low, then there is a transfer of information out of the bit map memory units (read out) to the registers. The register address is present because bit 7 of the column address is high.

Figure 10 depicts a timing signal generator to provide the signals RAS, CAS, WE and Sync 3, as well as the 80-, 40-and 20-MHz clock signals. Figure 10 shows a crystal oscillator 275 which transmits an 80-MHz signal to counters 277 and 279. A plurality of output signals (taps) from counter 277 are transmitted to the ROM 281. By virtue of a well-understood technique, the ROM 281 decodes the counter position of counter 277 and provides the gate signals RAS, CAS, WE and Sync 3 as shown in Figures 8 and 9. The WE signal is either high or low depending upon the state of the controllable inverter 283 shown in Figure 3A.

The 80-MHz signal is tapped from line 285 and provided to terminals such as terminal F of the ECL shift register 223 (as described earlier). The 80-MHz signal is transmitted to drive counter 279 to generate the 40-MHz signal through OR gate 287 and the 20-MHz signal through OR gate 289.

The present system advances the art of providing pixel signals by arranging a plurality of extended shift registers to be used with an enlarged bit map memory and by having the shift registers operate at different speeds. At least one of those shift registers in a preferred embodiment is designed to operate at very high speeds. The technology does not provide shift registers of different speed (particularly on the same integrated circuit chip) to be used with a common bit map memory. In addition, the present system advances the art of providing pixel signals by including a bidirectional mask device which can mask out any selected bits out of 256 bits or any bits out of 1024 bits, and by interconnecting extended shift registers and a bit map memory so that information can be entered

into the system from peripheral devices as well as read out of memory simultaneously by low-and high-resolution devices, and can be repeatedly transferred between shift register units and the bit map memory to effect window scrolling presentations and the like.

Claims

1. A circuit arrangement for storing pixel information and outputting signals representing said stored pixel information for display, comprising a data memory having an array of row and column positions for storing said pixel information thereat, said data memory having a plurality of data ports, a first control circuit connected to said data memory to enable inputting and outputting of signals representing said stored pixel information respectively to and from said data memory at predetermined locations, a first shift register having a plurality of data ports connected in parallel to said plurality of data ports of said data memory, a first timing circuit connected to said first shift register, said first timing circuit outputting clock signals at a first predetermined clocking rate, a first gating arrangement connected between said first shift register and said data memory for gating the flow of signals representing pixel information therebetween, a second control circuit connected to control the gating of said first gating arrangement, said first shift register being connected to shift and output signals representing pixel information in series to a first peripheral device at a first predetermined clocking rate for display, characterized in that said circuit arrangement further comprises a second shift register having a plurality of data ports connected in parallel to said plurality of data ports of said data memory, a second timing circuit connected to said second shift register, said second timing circuit outputting clock signals at a second predetermined clocking rate, a second gating arrangement connected between said second shift register and said data memory for gating the flow of signals representing pixel information therebetween, said second gating arrangement being connected to said second control circuit which controls the gating thereof, said second shift register being connected to shift signals representing pixel information at said second predetermined clocking rate.

2. The circuit arrangement of claim 1, characterized in that said data memory comprises a bit map memory.

3. The circuit arrangement of claim 1, characterized in that said second shift register has a data port for receiving signals representing pixel information in series at said second predetermined clocking rate.

4. The circuit arrangement of claim 1, characterized in that said second shift register has a data port for outputting signals representing pixel information in series to a second peripheral device at said second predetermined clocking rate for display.

5. The circuit arrangement of claim 3, characterized in that a third shift register is provided having a plurality of data ports connected in parallel to said plurality of data ports of said data memory, a third timing circuit is connected to said third shift register, said third timing circuit outputting clock signals at a third predetermined clocking rate, a third gating arrangement is connected between said third shift register and said data memory for gating the flow of signals representing pixel information therebetween, said third gating arrangement being connected to said second control circuit which controls the gating thereof, said third shift register being connected to shift and output signals representing pixel information to a second peripheral device at said third predetermined clocking rate for display.

6. The circuit arrangement of claim 3, characterized in that said first and second gating arrangements are connected to a masking gating arrangement, a masking register is connected to said data memory by way of a masking register gating arrangement for receiving masking information therefrom and is connected to said masking gating arrangement for controlling said masking gating arrangement in dependence on said masking information, said masking register gating arrangement being connected to said second control circuit.

7. The circuit arrangement of claim 6, characterized in that the transmission circuits connecting said data memory and said masking gating arrangement are capable of transmitting data in either of two directions, the data ports of said second shift register being capable of outputting signals representing pixel information in parallel to said data memory, and the data ports of said first shift register being capable of receiving signals representing pixel information in parallel from said data memory.

8. The circuit arrangement of claim 6, characterized in that said data memory, said first and second control circuits, said first and second shift registers, and said masking register are formed as an integrated chip.

9. The circuit arrangement of claim 4, characterized in that said first and second shift registers receive signals representing pixel information in parallel from said data memory, and said first and second shift registers respectively output said signals representing pixel information in series to

said first and second peripheral devices at said first and second predetermined clocking rates respectively.

10. The circuit arrangement of claim 5, characterized in that a fourth shift register is provided having a plurality of data ports connected in parallel to said plurality of data ports of said data memory, a fourth timing circuit is connected to said fourth shift register, said fourth timing circuit outputting clock signals at a fourth predetermined clocking rate, a fourth gating arrangement is connected between said fourth shift register and said data memory for gating the flow of signals representing pixel information therebetween, said fourth gating arrangement being connected to said second control circuits which controls the gating thereof, said fourth shift register being capable of receiving signals representing pixel information in parallel from said data memory, shifting said received pixel information in either of two directions, and outputting signals representing said shifted pixel information in parallel to said data memory.

11. The circuit arrangement of claim 11, characterized in that said data memory, said first and second control circuits, said masking register and said first, second, third and fourth shift registers are formed as an integrated chip.

12. The circuit arrangement of claim 11, characterized in that sixteen of said integrated chips are arranged to form a four-by-four array of data memories and four groups of four extended shift registers, each extended shift register comprising four shift registers connected in series, shift registers of each group being connected to a corresponding one of said data memories, the extended shift registers of said first group being connected to serially output signals representing pixel information at said first predetermined rate to said first peripheral device and the extended shift registers of said third group being connected to serially output signals representing pixel information to said second peripheral device.

Amended claims in accordance with rule 86(2) EPC.

1. An integrated circuit chip for storing pixel information and outputting signals representing said stored pixel information for display, comprising bit map memory means having an array of row and column positions for storing said pixel information thereat, said bit map memory means having a plurality of data ports, first control means connected to said bit map memory means for enabling the input and outpout of pixel and masking information to and from predetermined addresses in said bit map memory means, first shift register means for shifting pixel information stored therein, said first shift register means having a plurality of data ports connected to said plurality of data ports of said bit map memory means by way of first gating means, a mask register means for storing masking information, said mask register means being connected to said plurality of data ports of said bit map memory means by way of a second gating means, and said first and second gating means being connected to a second control means for controlling the gating of said first and second gating means, and said mask register means being connected to said first gating means,
wherein said second control means is capable of outputting a first control signal to said second gating means for enabling the transfer of masking information from said bit map memory means to said mask register means and a second control signal to said first gating means for enabling the transfer of pixel information from said bit map memory means to said first shift register means, said masking register means being capable of transferring said masking information to said first gating means for masking predetermined bits of said pixel information.

2. An integrated circuit chip for storing pixel information and outputting signals representing said stored pixel information for display, comprising bit map memory means having an array of row and column positions for storing said pixel information thereat, said bit map memory means having a plurality of data ports, first control means connected to said bit map memory means for enabling the input and output of pixel and masking information to and from predetermined addresses in said bit map memeory means, first shift register means having a plurality of data ports connected in parallel to said plurality of data ports of said bit map memory means by way of first gating means for gating the flow of pixel information between said bit map memory means and said first shift register means, second shift register means having a plurality of data ports connected in parallel to said plurality of data ports of said bit map memory means by way of second gating means for gating the flow of pixel information between said bit map memory means and said second shift register means, said first and second gating means being connected to second control means for controlling the gating of said first and second gating means, wherein said second control means is capable of outputting a first control signal to said first gating means for enabling the transfer of pixel information between said first gating means for enabling the transfer of pixel information between said bit map memory means and said first register means and a second control signal to said second gating means

for enabling the transfer of pixel information between said bit map memory means and said second shift register means.

3. A circuit arrangement for storing pixel information and outputting signals representing said stored pixel information for display, comprising bit map memory means having an array of row and column positions for storing said pixel information thereat, said bit map memory means having a plurality of data ports, first control means connected to said bit map memory means for enabling the input and output of pixel and masking information to and from predetermined addresses in said bit map memory means, first shift register means for shifting pixel information stored therein, said first shift register means having a plurality of data ports connected to said plurality of data ports of said bit map memory means by way of first gating means, a mask register means for storing masking information, said mask register means being connected to said plurality of data ports of said bit map memory means by way of a second gating means, said first and second gating means being connected to a second control means for controlling the gating of said first and second gating means, and said mask register means being connected to said first gating means,
wherein said second control means is capable of outputting a first control signal to said second gating means for enabling the transfer of masking information from said bit map memory means to said mask register means and a second control signal to said first gating means for enabling the transfer of pixel information from said bit map memory means to said first shift register means, said masking register means being capable of transferring said masking information to said first gating means for masking predetermined bits of said pixel information.

4. The circuit arrangement as defined in claim 3, further comprising third gating means connected between said first shift register means and said first gating means, and second shift register means for shifting pixel information stored therein, said second shift register means having a plurality of data ports connected to said plurality of data ports of said bit map memory means by way of fourth gating means and said first gating means in serties, wherein said second control means is capable of outputting a third control signal to said third gating means for enabling the transfer of pixel information between said first shift register means and said first gating means and a fourth control signal to said fourth gating means for enabling the transfer of pixel information between said second shift register means and said first gating means.

5. The circuit arrangement as defined in claim 4, wherein said circuit arrangement is formed as an integrated chip.

6. The circuit arrangement as defined in claim 4, further comprising third and fourth shift register means connected to said first gating means by way of fifth an sixth gating means respectively.

7. The circuit arrangement as defined in claim 4, further comprising a first clocking means connected to said first shift register means for supplying clock signals at a first clocking predetermined rate and a second clocking means connected to said second shift register means for supplying clock signals at a second predetermined clocking rate different than said first predetermined clocking rate.

8. The circuit arrangement as defined in claim 7, wherein said first shift register means has an output port for supplying pixel information in series to a first peripheral device at a first rate dependent on said first predetermined clocking rate, and said second shift register means has an output port for supplying pixel information in series to a second peripheral device at a second rate dependent on said second predetermined clocking rate.

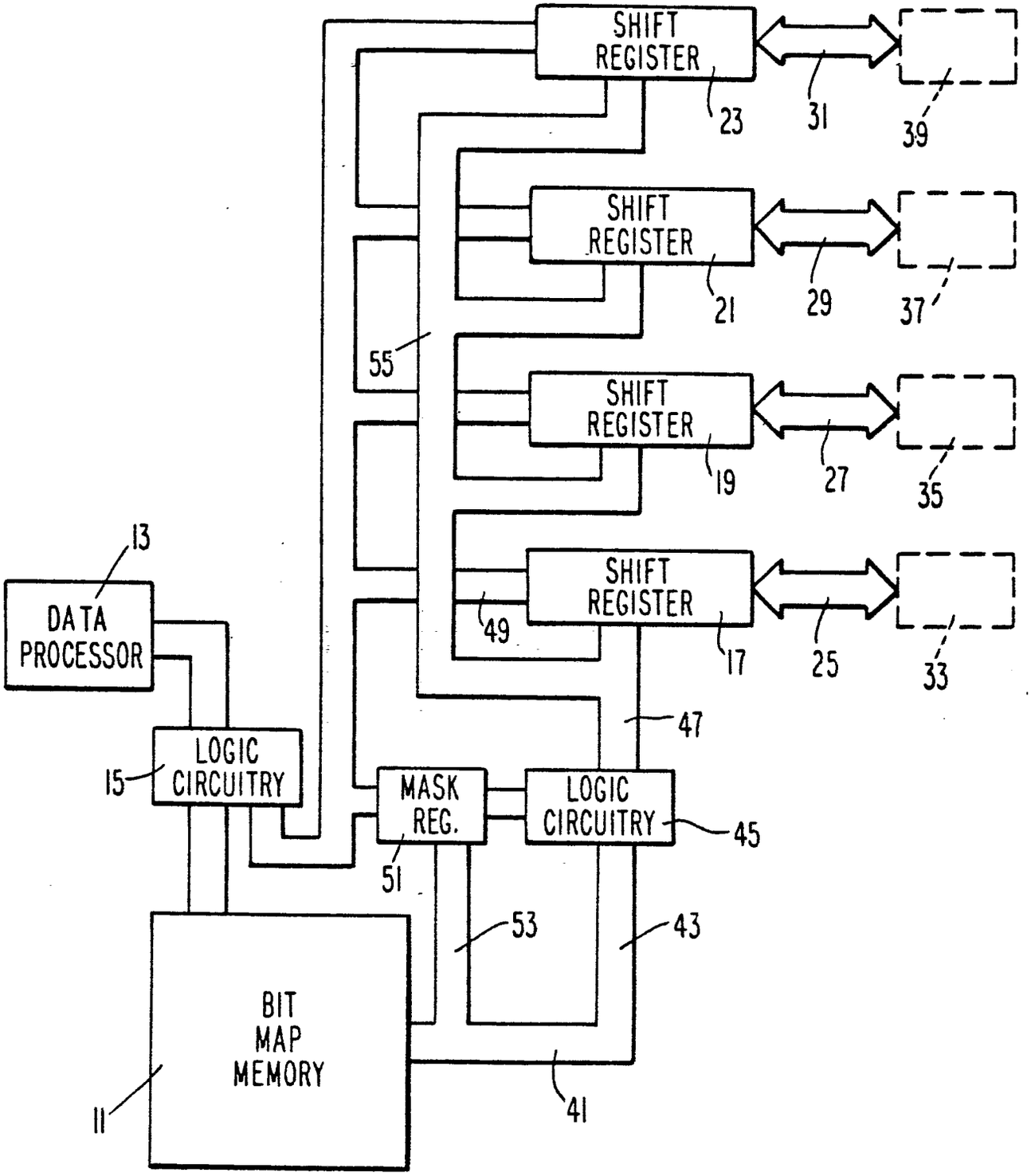
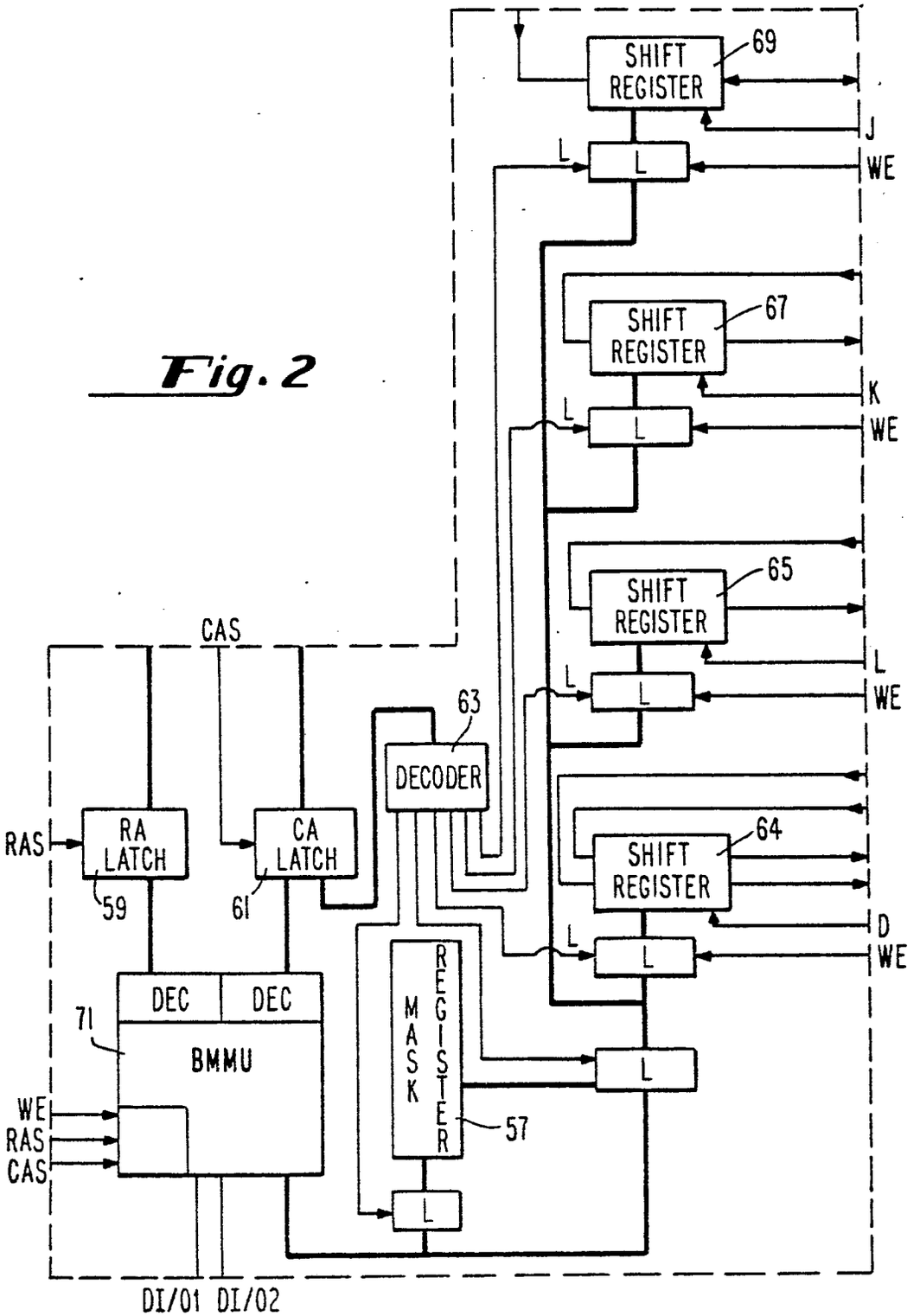

SHIFT REGISTER
23
31
39
SHIFT REGISTER
21
29
37
55
SHIFT REGISTER
19
27
35
SHIFT REGISTER
49
17
25
33
13
DATA PROCESSOR
47
LOGIC CIRCUITRY
15
MASK REG.
LOGIC CIRCUITRY
45
51
53
43
BIT MAP MEMORY
11
41

Fig. 1

Fig. 2


SHIFT REGISTER
69
J
L
WE
SHIFT REGISTER
67
K
L
WE
SHIFT REGISTER
65
L
L
WE
SHIFT REGISTER
64
D
L
WE
CAS
63
DECODER
RAS
RA LATCH
59
CA LATCH
61
DEC
DEC
71
BMMU
WE
RAS
CAS
MASK REGISTER
57
L
DI/01
DI/02

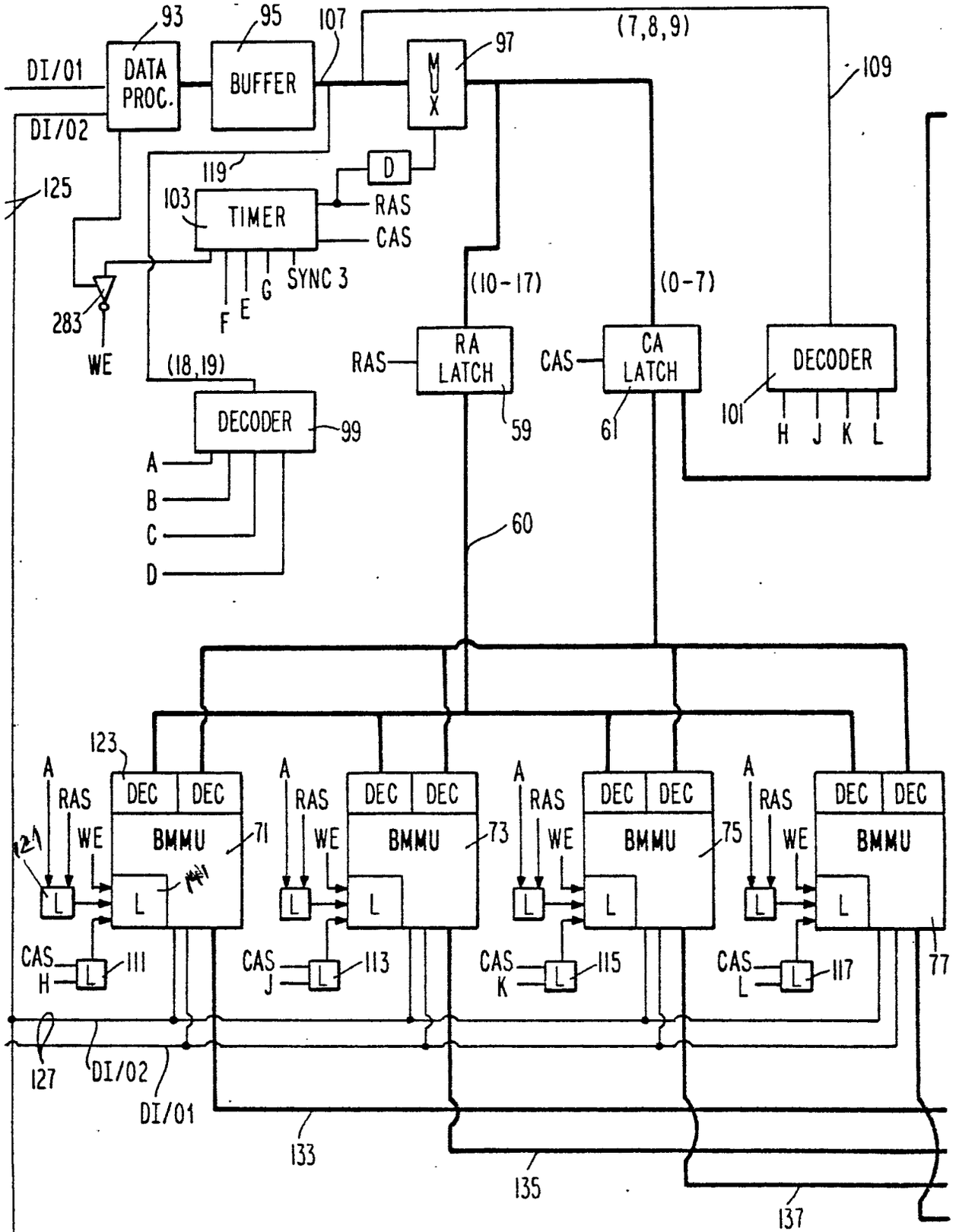

93
95
107
(7,8,9)
97
109
DI/01
DATA PROC.
BUFFER
MUX
DI/02
119
D
125
103
TIMER
RAS
CAS
SYNC 3
G
F
E
283
WE
(10-17)
(0-7)
RAS
RA LATCH
CAS
CA LATCH
DECODER
101
H J K L
59
61
(18,19)
DECODER
99
A
B
C
D
60
123
DEC DEC
BMMU
71
73
75
77
RAS
WE
CAS H
CAS J
CAS K
CAS L
111
113
115
117
127
DI/02
DI/01
133
135
137

Fig. 3A

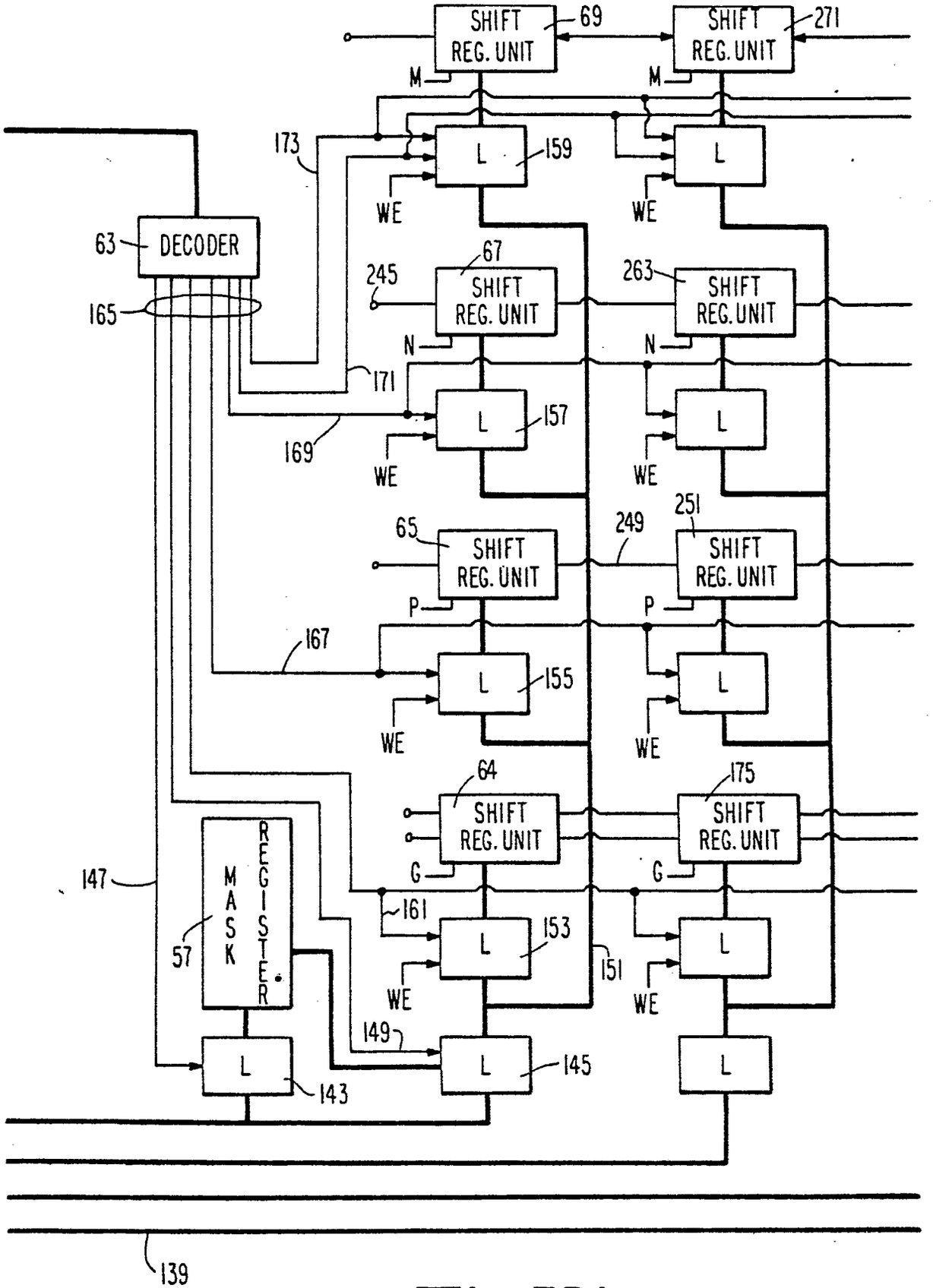

SHIFT REG. UNIT
69
271
M
L
159
WE
173
63
DECODER
165
67
245
263
N
171
157
169
65
249
251
P
167
155
64
175
G
147
MASK REGISTER
57
161
153
151
149
145
143
139

Fig. 3B1

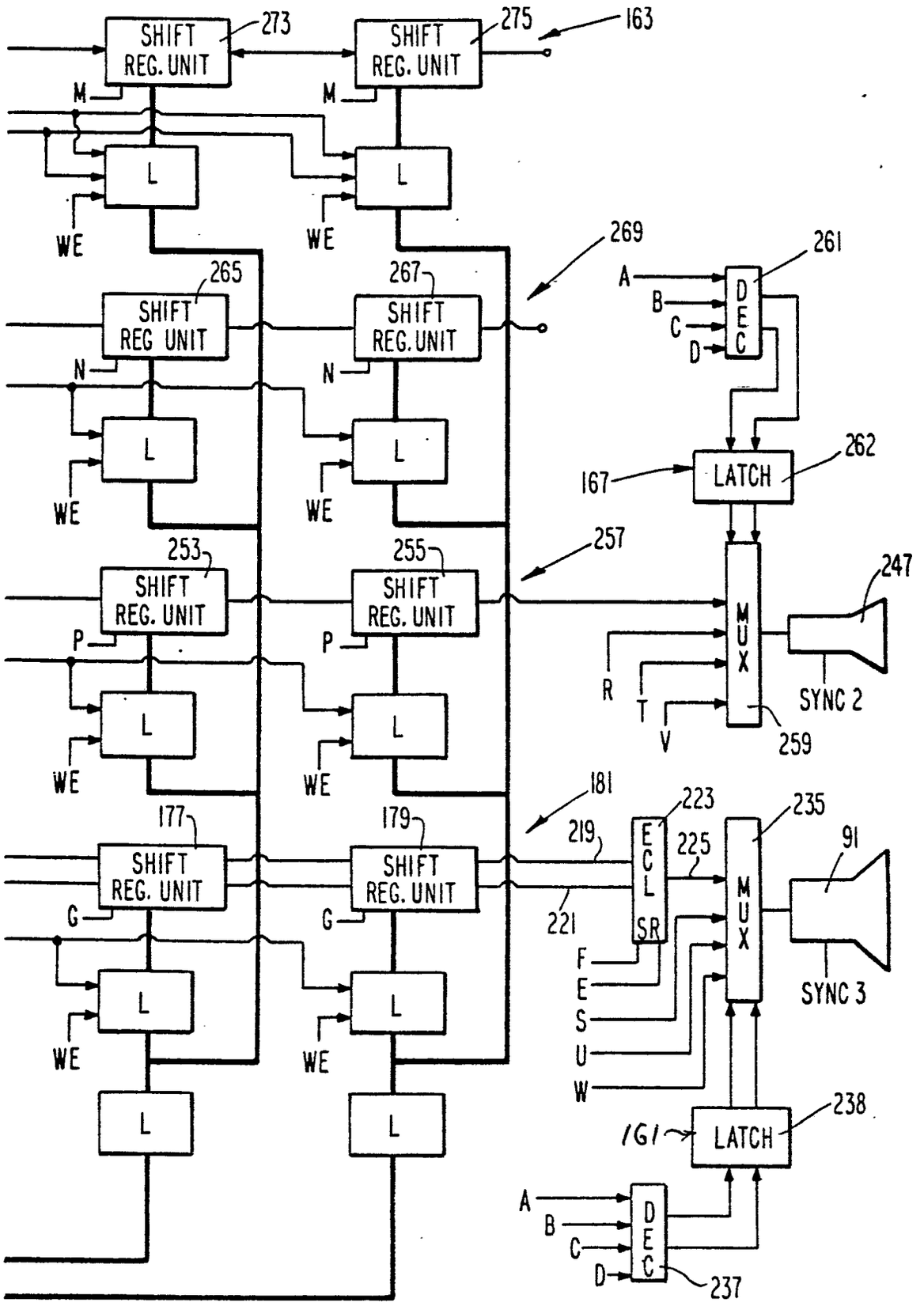
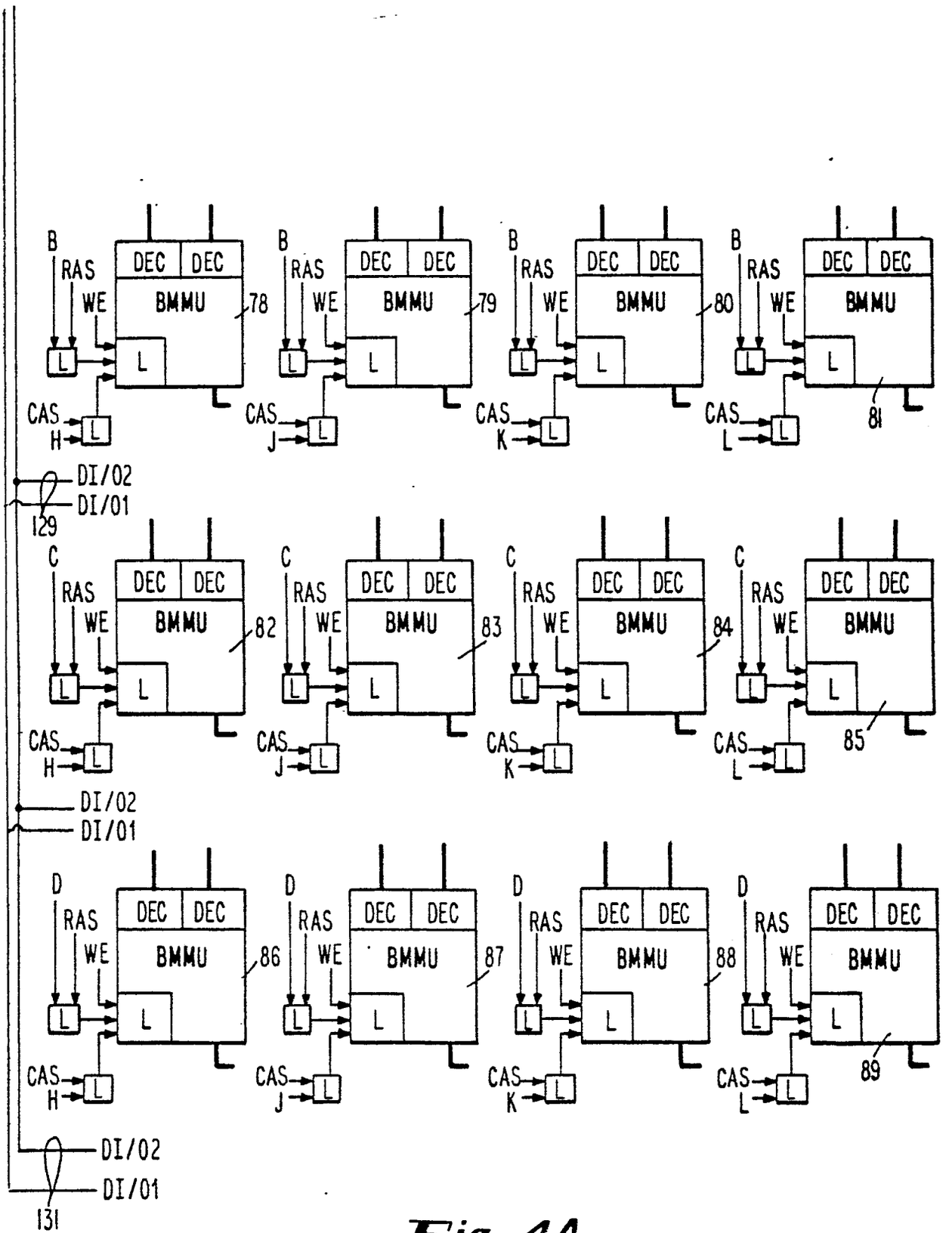

SHIFT REG. UNIT
273
275
163
M
L
WE
269
261
A
B
C
D
DEC
265
267
N
167
LATCH
262
253
255
257
P
247
MUX
R
T
V
SYNC 2
259
177
179
181
219
223
235
91
225
ECL SR
G
F
E
S
U
W
221
SYNC 3
238
161
237

Fig. 3B2


B
RAS
WE
DEC
DEC
BMMU
78
79
80
81
CAS
H
J
K
L
DI/02
DI/01
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C
82
83
84
85
D
86
87
88
89
131

Fig. 4A

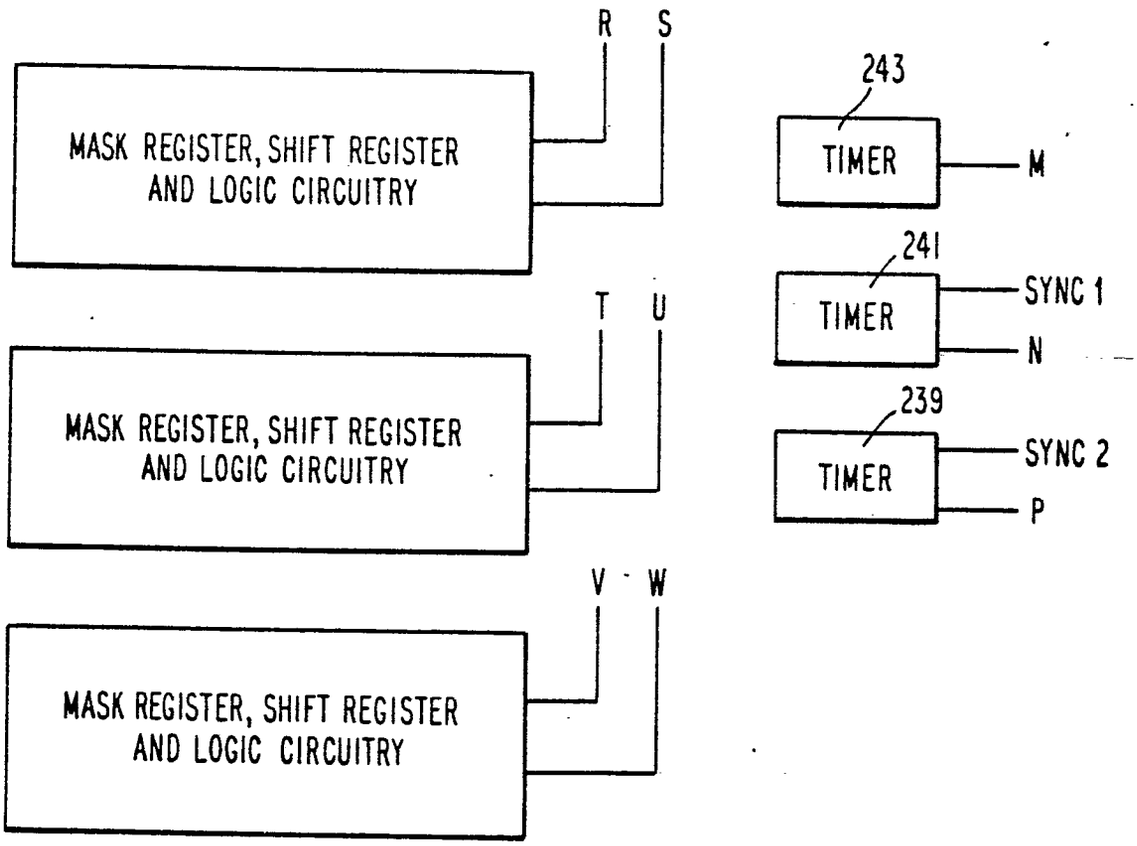
R
S
MASK REGISTER, SHIFT REGISTER AND LOGIC CIRCUITRY
243
TIMER
M
241
TIMER
SYNC 1
N
T
U
MASK REGISTER, SHIFT REGISTER AND LOGIC CIRCUITRY
239
TIMER
SYNC 2
P
V
W
MASK REGISTER, SHIFT REGISTER AND LOGIC CIRCUITRY

Fig. 4B

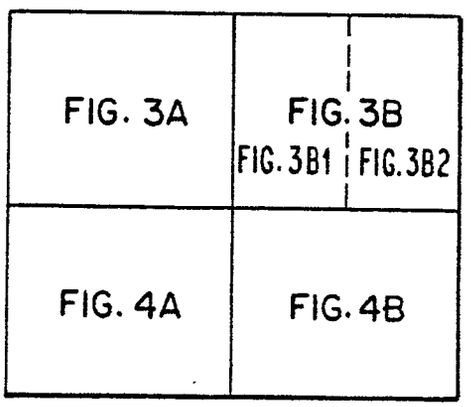
FIG. 3A
FIG. 3B
FIG. 3B1
FIG. 3B2
FIG. 4A
FIG. 4B

Fig. 5

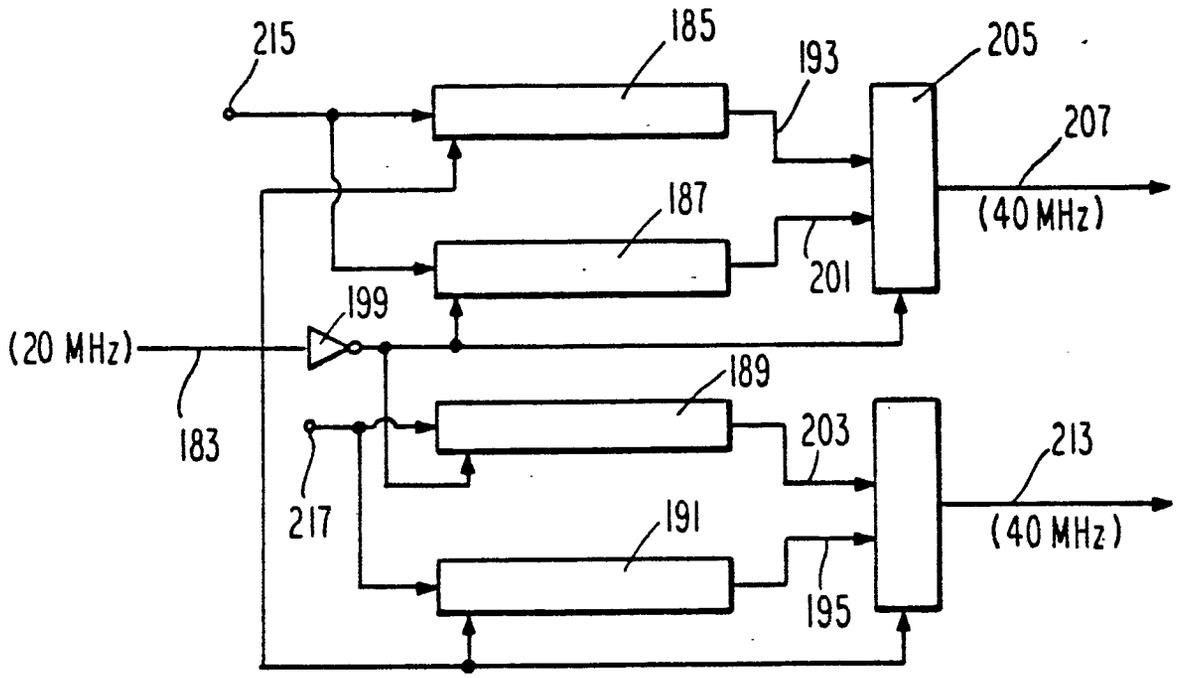
215
185
193
205
207
(40 MHz)
187
201
199
(20 MHz)
183
189
203
213
(40 MHz)
217
191
195

Fig. 6

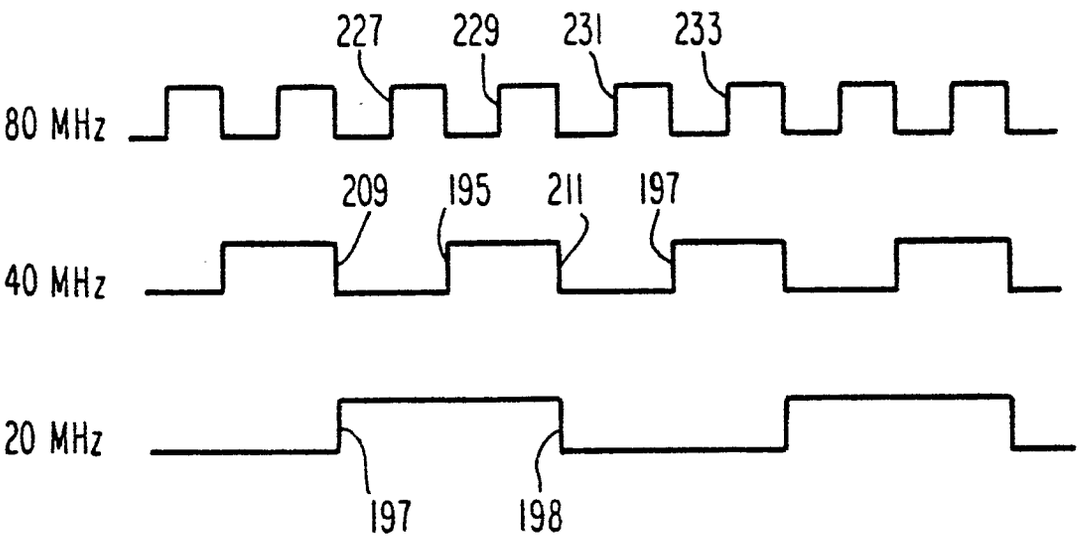
227
229
231
233
80 MHz
209
195
211
197
40 MHz
20 MHz
197
198

Fig. 7

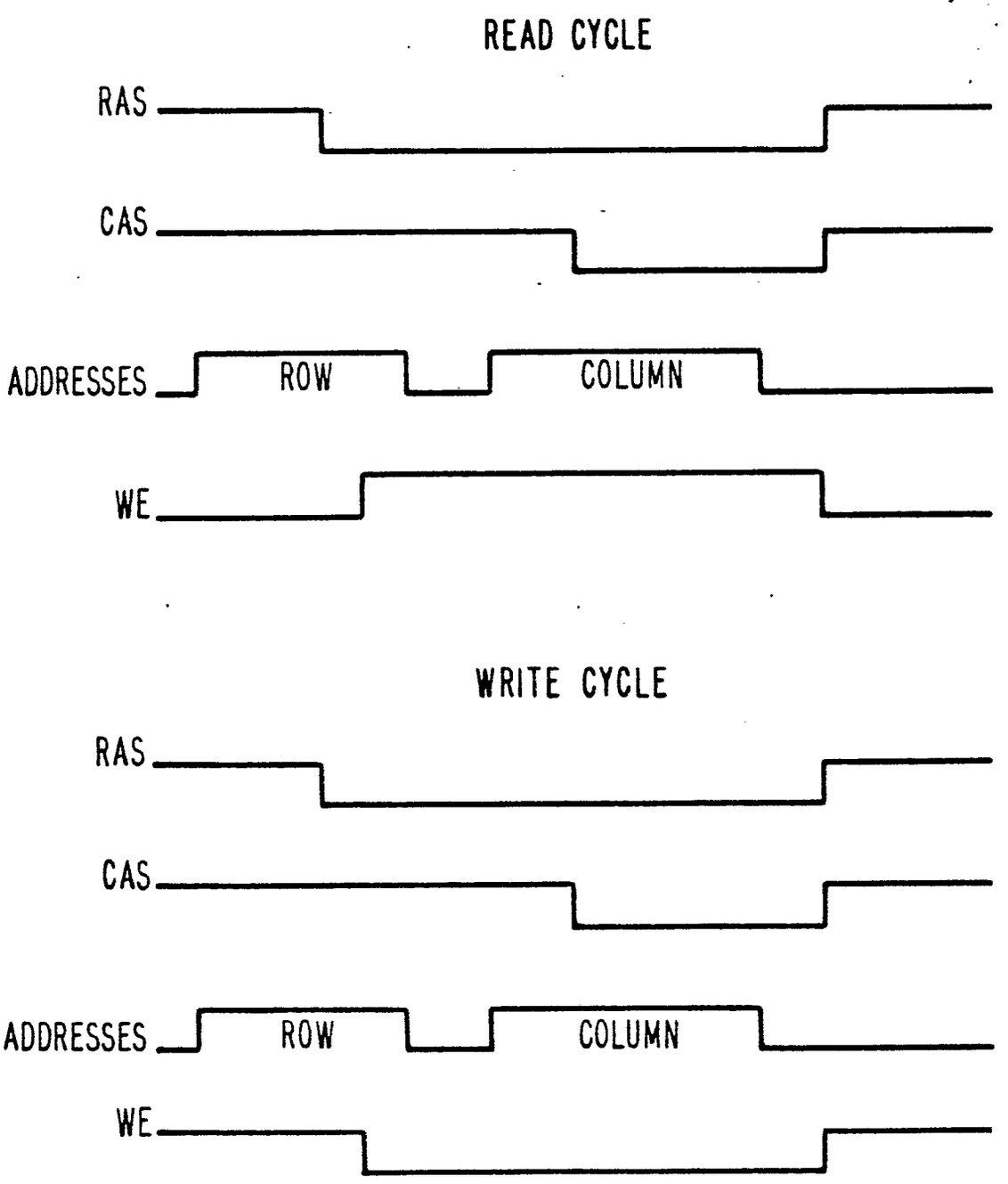
READ CYCLE
RAS
CAS
ADDRESSES
ROW
COLUMN
WE
WRITE CYCLE
RAS
CAS
ADDRESSES
ROW
COLUMN
WE

Fig. 8

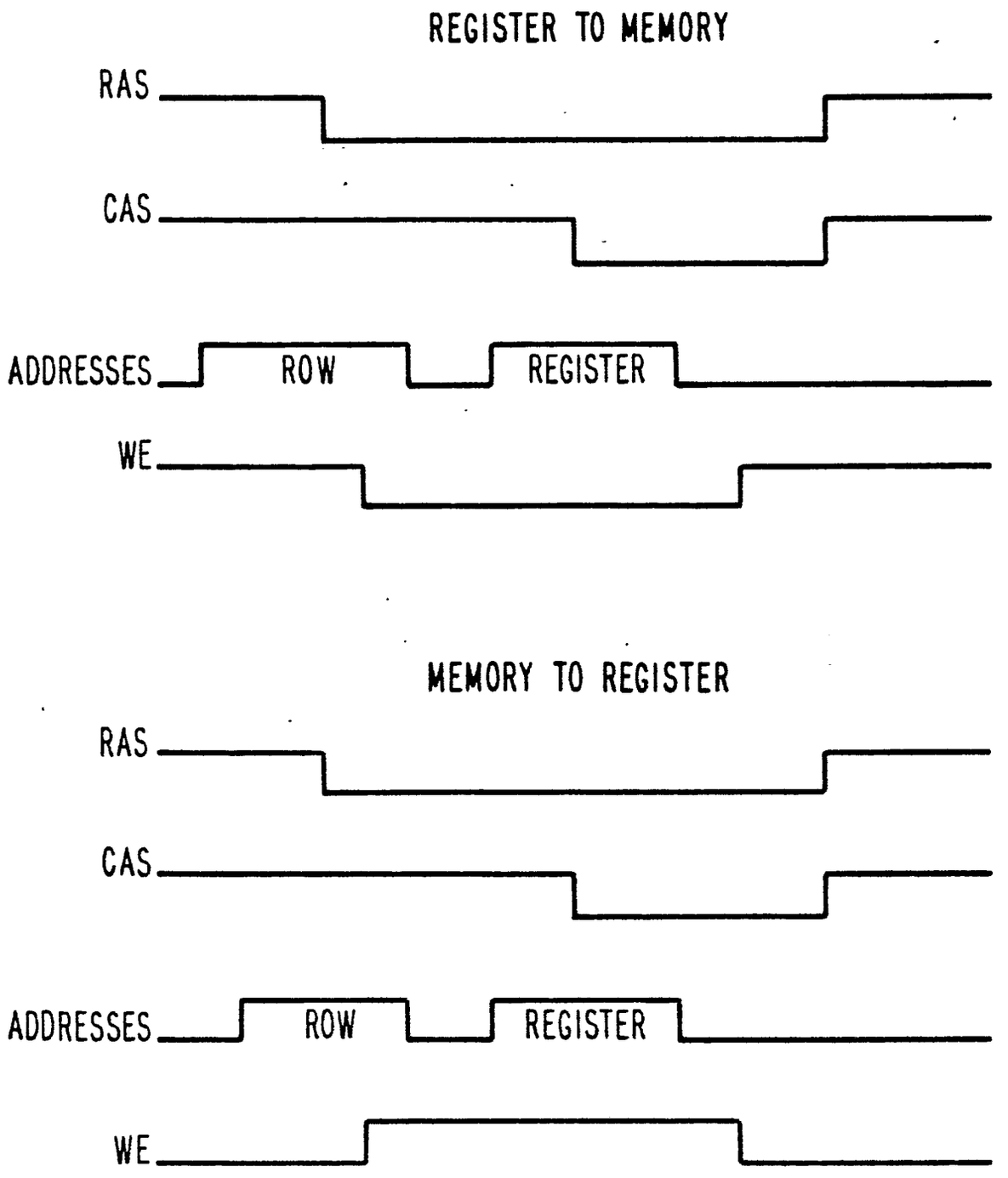
REGISTER TO MEMORY
RAS
CAS
ADDRESSES
ROW
REGISTER
WE
MEMORY TO REGISTER
RAS
CAS
ADDRESSES
ROW
REGISTER
WE

Fig. 9

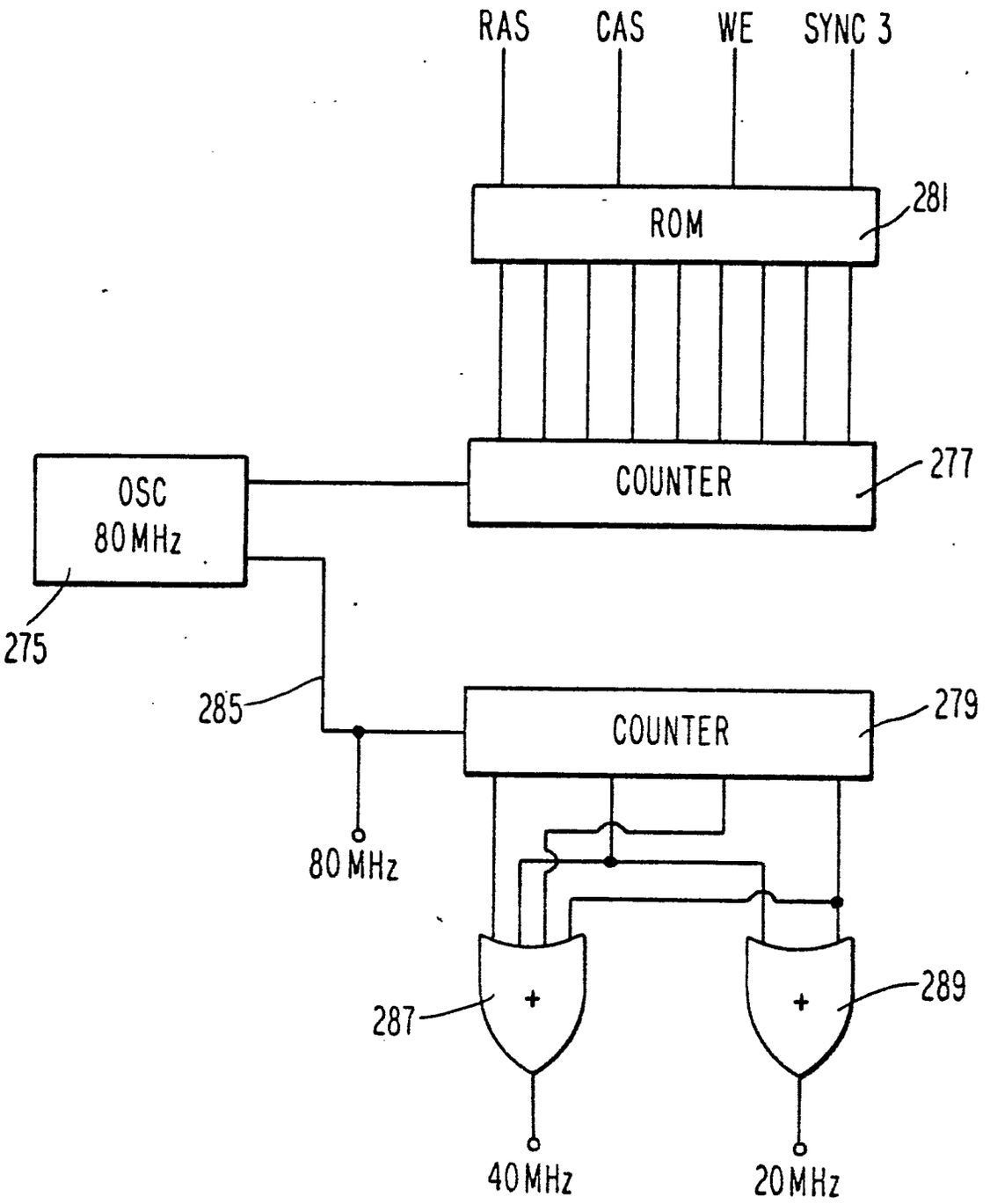
RAS
CAS
WE
SYNC 3
ROM
281
COUNTER
277
OSC
80 MHz
275
285
COUNTER
279
80 MHz
287
289
40 MHz
20 MHz

Fig. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 86 40 0976

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	US-A-4 546 451 (BRUCE) * Figure 3 *	1,2	G 09 G 1/16
A	US-A-4 174 536 (MISUNAS et al.) * Column 3, lines 11-20 *	1	
A	EP-A-0 147 500 (FUJITSU LTD.) * Page 15, line 30 - page 16, line 11 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 09 G 1/16

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28-01-1987	SIX G.E.E.

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