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Ignition system.

(57) A plurality of electric blasting caps are fired through the ignition system which includes a transformer (19) having a primary winding (17) and a secondary winding (21). The secondary winding (21) of the transformer (19) is connected to the resistive elements (53) of the blasting caps (55) through a blasting circuit which is electromagnetically coupled to the resistive elements (53) of the blasting caps (55) via a small toroid transformer. A D.C. voltage is stored on a storage capacitor (3) which has one end connected to the center point (15) of the primary winding (17). The other ends of each half of the primary winding (17) are connected through a driver circuit (29) to ground. Each driver circuit (29) is enabled by a flip-flop (35) at predeter-Minned intervals, whereby the storage capacitor (3) will discharge through the appropriate half of the mprimary, to thereby produce a pulse train at the output of the secondary. The pulse train provides the ignition power for igniting the electric blasting caps.

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IGNITION SYSTEM

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The invention relates to an ignition system for firing electric blasting caps. More specifically, the invention relates to such an ignition system which can simultaneously ignite more blasting caps than presently available ignition systems.

An ignition system which employs electromagnetic coupling between the energy source and the ignition element in the cap is taught in, for example, U.S. Patent No. 4,297,947, Jones et al, November 3, 1981. Although the patented system has proven to be very effective, it is limited as to the number of caps it can ignite simultaneously.

It is an object of the invention to provide an ignition system which overcomes the limitations of the prior art.

It is a more specific object of the invention to provide such an ignition system which can ignite more blasting caps simultaneously than can presently available ignition systems.

In accordance with the invention, there is provided, in an ignition system for firing a plurality of electric blasting caps, which ignition system includes a transformer having a primary winding and a secondary winding and means connecting the secondary winding to the resistive elements of the blasting caps, a means for storing a D.C. voltage. The means for storing is connected to the primary winding. The means for storing is dischared through the primary at predetermined intervals whereby a pulse train is produced in the primary winding. The pulse train is transmitted through the secondary winding to the resistive elements.

The invention will be better understood by an examination of the following description, together with the accompanying drawings, in which:

Figure I is a schematic drawing of the inventive system;

Figure 2 illustrates in greater detail the driver circuit in Figure I;

Figure 3 shows the signal at the primary of the transformer in Figure I;

Figure 4 shows the signal at the secondary of the transformer in Figure I; and

Figure 5 illustrates how the system of Figure I is connected to blasting caps.

Referring to Figure I, the system includes a high voltage D.C. power supply I. Basically, the power supply is nothing more than a circuit including rectifiers and the like for converting an A.C. input, from the A.C. mains, to a D.C. output. Such circuits are well known in the art and require no further description.

The output of the D.C. power supply I is fed to a means for storing charge, for example, a storage capacitor, illustrated at 3, through a charge current limiter 5 which, as is well known in the art, can comprise a resistor. One end of the storage capacitor 3 is connected to the output of the D.C. power supply, and the other end is connected to a point of common potential, e.g., ground. The one end of the storage capacitor is also connected to the input of a voltage sensing circuit 7. The purpose of the voltage sensing circuit is to determine when the voltage across the storage capacitor reaches a predetermined level. Such circuits are well known in the art.

The output of the voltage sensing circuit is fed to the input of an electronic latch 9 which has outputs 10 and 12. Output 10 of the electronic latch 9 is fed to an input of A.C. switch II, and the output of A.C. switch II is fed to the ON/OFF terminal of the D.C. power supply I. The other output, 12, of electronic latch 9, is fed to a delay latch means 13, as will be further discussed below.

The one end of the storage capacitor 3 is also fed to the mid-point 15 of primary winding 17 of transformer 19 which has a secondary winding 21. The one end of storage capacitor 3 is fed to the mid-point 15 through a fault protection current limiting device 16 which, once again, can comprise a resistor.

The primary winding I7 consists of a first half 23, which extends-from the mid-point I5 in one direction, and a second half 25, which extends from the center point I5 in the opposite direction. The half 23 is in circuit with a driver circuit 27, while the half 25 is in circuit with a driver circuit 29. Driver circuits 27 and 29 will be more fully described in association with Figure 2 below.

Over voltage protection means 3I is in circuit with the driver circuit 27 while over voltage protection means 33 is in circuit with the driver circuit 29 and over voltage protection means 34 is between the gates and the grounded terminals of the FETs. The over voltage protection means comprise arrangements of zener diodes to limit the voltage as well known in the art.

The output of delay latch means I3 is fed to an ON/OFF terminal of a flip-flop arrangement 35 which has outputs 37 and 39. As well known in the art, when the output 37 is high, then output 39 is low and vice versa.

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All of the electronic circuits, such as the voltage sensing circuit 7, the electronic latch 9, the delay latch means I3, the driver circuits 27 and 29 and the over voltage protection means 3I and 33 are powered by a bias voltage supply 4I which is also connected to the A.C. mains.

Turning now to Figure 2, the driver circuits 27 and 29 comprise a plurality of switches arranged in parallel. Specifically, in a preferred embodiment, they comprise eight (8) power FETs 43 in parallel arrangement. Output 37 is connected to the gates of the FETs of driver circuit 27, while output 39 is connected to the gates of the FETs of driver circuit 29.

Turning now to Figure 5, the secondary 2I of the transformer I9 is connected to a lead cable 45 which can be from 300 to I,000 feet in length of I0 to I2 gauge wire. The lead cable 45 is in turn connected to either end of a primary loop 47. The loop 47, which is I00-300 ft. long, is threaded through a plurality of toroids 49 (up to 300), and the secondary 5I of each toroid is connected to the resistive element 53 of a respective blasting cap 55. The latter arrangement is similar to the arrangement illustrated in Figure 2 of the 4,297,947 patent above referred to.

In operation, the system works as follows:

After the blasting caps have been placed and the toroids have been threaded, the plug of the D.C. power supply is plugged into the mains, and the A.C. of the mains is converted to D.C. voltage which charges the storage capacitor 3. When the charge on the storage capacitor causes a predetermined voltage to appear across the capacitor (in a preferred embodiment I40 volts), then the voltage sensing circuit will emit a signal to trip the electronic latch 9. The electronic latch will in turn, through its output I0, provide a signal to actuate the A.C. switch II which, in turn, will turn off the D.C. power supply. The A.C. switch II will remain activated until the A.C. source is disconnected from the system.

At the same time, the electronic latch will provide, through its output 12, a signal to trip delay latch means 13. The delay latch means will provide a predetermined delay (preferably 30ms), whereupon the delay latch means 13 will, in turn, provide an activating signal to the flip-flop arrangement 35. The flip-flop arrangement will then be turned on to provide signals alternately at its output 37 and 39. The frequency of the flip-flop is preferably made variable. In one arrangement, the frequency of the flip-flop is 10 kHz.

Turning now to Figure 2, when output 37 is high, the voltage will be applied to the FETs 43 of driver circuit 27 to turn ON all of these FETs. Thus, there will be provided a path for discharging storage capacitor 3 through half 23 and through the

short circuited FETs 43 of driver circuit 27. On the other half of the flip-flop cycle, the output 39 is high and a dischage path for the storage capacitor is provided through the half 25 and the driver circuit 29. Each of the driver circuits as is clearly shown in Figures I and 2 has an output connected to common potential, e.g., ground.

The signal at the center point I5 of the primary I7 is, thus, a pulse train of decreasing amplitude as illustrated in Figure 3. This signal, being an A.C. signal, is transformed and the signal, as illustrated in Figure 4, appears across the secondary 2I of the transformer I9. Preferably, the transformation ratio of the transformer I9 is of the order of 6-8:I. Thus, the output of the secondary is of the order of 950 volts "peak", 6 amps average. This output is applied, simultaneously, to each resistive element 53 of the blasting caps 55 connected to the primary loop 47 through the toroids 49.

In view of the fact that 8 FETs are used in parallel, it is not necessary to use any high power switch. The entire arrangement permits the delivery of sufficient energy to fire up to 300 detonators.

In addition, most prior art systems which employ electromagnetic coupling between the source of energy and the blasting caps require a capacitor circuit with the secondary to cancel part of the inductance of the blasting circuit. In the present arrangement, because of the level of energy delivered, such a capacitor is not required. Accordingly, the output is steadier in that it is not affected by unexpected resonance in the output circuit which unexpected resonance could lead to high voltages or currents.

Although a particular embodiment has been described, this was for the purpose of illustrating, but not limiting the invention. Various modifications, which will come readily to the mind of one skilled in the art, are within the scope of the invention as defined in the appended claims.

Claims

I. An ignition system for firing a plurality of electric blasting caps, said ignition system comprising a transformer having a primary winding and a secondary winding, and means connecting said secondary winding to the resistive elements of said blasting caps; characterised in that said system comprises

means for storing a D.C. voltage, said means for storing being connected to said primary winding; and

means for permitting dischage of said means for storing at predetermined intervals through said primary winding;

whereby, to produce a pulse train in said

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primary winding which is transmitted, through said secondary winding, to said resistive elements to thereby fire said blasting caps.

- 2. A system as defined in Claim I characterised in that said means for storing comprises a storage capacitor, and including means for charging said storage capacitor to a predetermined voltage level.
- 3. A system as defined in Claim I or Claim 2 characterised in that said means for permitting discharge comprises driver circuit means comprising a parallel arrangement of a plurality of electronic switch means, and means for activating the electronic switch means at said predetermined intervals.
- 4. A system as defined in Claim 3 characterised in that said primary winding has a center point, the first half of said primary winding extending from said center point at one end of said first half, in one direction to the other end of said first half, the second half of said primary winding extending from said center point, at one end of said second half, in the opposite direction to the other end of said second half;

one end of said storage capacitor being connected to said center point and the other end of said storage capacitor being connected to a point of common potential;

said driver circuit means comprising a first driver circuit and a second driver circuit;

said first driver circuit being connected between the other end of said first half and said point of common potential;

said second driver circuit being connected between the other end of said second half and said point of common potential.

5. A system as defined in Claim 4 characterised in that each said first and second driver circuits each comprise eight field effect transistors (FETs) connected in parallel arrangement;

said means for activating being connected to the gate terminals of all of said FETs.

6. A system as defined in Claim 5 characterised in that said means for activating comprises a flip-flop having a first output and a second output;

said first output being connected to the gate terminals of said FETs of said first driver circuit; and

said second output being connected to the gate terminals of said FETs of said second driver circuit.

- 7. A system as defined in any one of Claims 2 to 6 characterised in that said means for charging said storage capacitor to said predetermined level comprises:
- a D.C. power supply having an output connected to said one end of said storage capacitor, and also having an ON/OFF terminal;
- a voltage sensing circuit having an input connected to said one end of said capacitor and

also having a output;

a first latch means having an input connected to the output of said voltage sensing circuit and also having a first output;

switch means having an output connected to the first output of said first latch means and also having an output connected to the ON/OFF terminal of said D.C. power supply;

whereby, said D.C. power supply charges said storage capacitor to increase the D.C. level of said storage capacitor and, when said D.C. level reaches said predetermined level, said first latch means is tripped to activate said switch means to turn off said power supply.

- 8. A system as defined in Claim 6 and Claim 7 characterised in that said first latch means also has a second output, and further comprises:
- a delay latch means for providing a predetermined delay and having an input connected to the second output of said first latch means, and also having an output;

said flip-flop having an ON/OFF terminal connected to the output of said delay latch means;

whereby, said flip-flop is turned ON after passage of said predetermined delay following the time when said predetermined level is reached on said storage capacitor.

9. A system as defined in Claim 7 or Claim 8 and further characterised by including first current limiting means connected between the output of said D.C. power supply at said one end of said storage capacitor; and

second current limiting means connected between said one end of said storage capacitor and said center point of said primary winding.

IO. A system as defined in any one of Claims 5 to 9 and further characterised by including first over voltage protection means connected between the gates of said FETs and one other terminal of said FETs, and second over voltage protection means connected between the gates of said FETs and the other terminal of said FETs.

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