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(54) Reactive power compensation apparatus.

(57) A reactive power compensation apparatus for compensating for voltage fluctuation of an AC power supply system includes a first arithmetic circuit (403, 406, 408, 413) for synthesizing a positive-phase fundamental wave voltage signal (PIPD) from voltages (eRS, eST, eTR) of the AC power supply system, a second arithmetic circuit (403, 406, 410, 414, 415) for synthesizing negative-phase voltage signals (PIND, QIND) from the voltages (eRS, eST, eTR) of the AC power supply system, a third arithmetic circuit (420A), coupled to the first and second arithmetic circuits (413 - 415), for synthesizing current instructions (IU*, IV*, IW*) from the positive-phase fundamental wave voltage (PIPD) and the negative-phase voltage signals (PIND, QIND), and a circuit (200, 300, 500), coupled to the third arithmetic circuit (420A), for generating a reactive power corresponding to the current instructions (IU*, IV*, IW*).

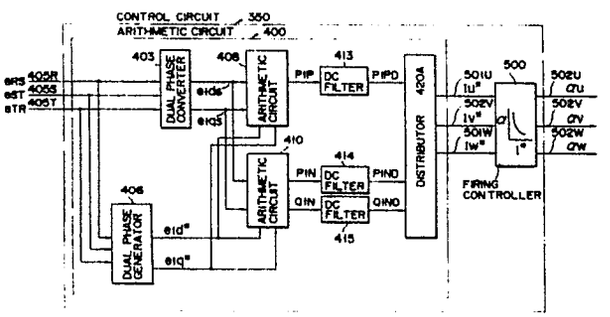

FIG. 3

EP 0 259 805 A2

Reactive power compensation apparatus

The present invention relates to a reactive power compensation apparatus and, more particularly, to an effective reactive power compensation apparatus which suppresses voltage fluctuation and unbalance in an AC power supply system so as to stabilize the power supply system.

In recent years, a load requiring a single-phase power such as an AC-powered electric train is coupled to a power supply system, and this causes a voltage unbalance of the power supply system due to the influences of an unbalanced current and an impedance of the power supply system. Voltage fluctuation upon a change in reactive power is also a problem. For this reason, the power supply system is equipped with a reactive power compensation apparatus to compensate for the reactive power of the power supply system and suppress the voltage fluctuation. Furthermore, the unbalanced current of the power supply system is compensated for to remove an unbalanced component of the voltage.

A power supply system equipped with a reactive power compensation apparatus is described in detail in an article entitled "Simulator Test for System Stabilization by Static Var Compensator (SVC) using Digital Controller" announced in Denki Gakkai, Denryoku Gijutsu Kenkyukai in July, 1985. The basic arrangement of this system is as shown in Fig. 1.

Referring to Fig. 1, reference numerals 10 and 11 denote power supply buses of branch lines coupled to the load such as an AC-powered electric train; 4, an AC power supply system; and 100, a reactive power compensation apparatus, which comprises reactor part 300 and phase-advanced capacitor part 200. Reactor part 300 comprises reactors 302U to 302W, cross-coupled thyristors 301U to 301W connected in series therewith, potential transformer 70, and control circuit 350 for thyristors 301U to 301W. Firing angles of thyristors 301U to 301W are adjusted by circuit 350 in accordance with a voltage detection value of power supply bus 6, thereby controlling current IR of reactor part 300. Note that reference numeral 3 denotes an impedance of a triple-phase AC power supply system; and 1, a triple-phase AC power supply system for trunk lines.

A power capacity (phase-delayed capacity) of reactor part 300 of apparatus 100 is normally set to be twice a power capacity (phase-advanced capacity) of phase-advanced capacitor part 200. When reactor current IR is changed from zero to maximum, power Q generated from apparatus 100 can be smoothly changed from an advanced-phase to a delayed-phase, as shown in Fig. 2.

In the power supply system with the above arrangement, if a reactive current (or reactive power) of bus 6 is changed, a voltage of bus 6 fluctuates upon a change in current (power) and impedance 3. When an unbalanced current generated by a single-phase load such as an AC-powered electric train flows through bus 6, the voltage of bus 6 is unbalanced due to the influence of the unbalanced current and impedance 3. The reactive power compensation apparatus is adopted to suppress and compensate for voltage fluctuation and unbalance. However, the performance of the apparatus is determined by the detection precision of the voltage fluctuation and unbalance.

The conventional reactive power compensation apparatus has the following drawbacks. More specifically, the voltage fluctuation of AC bus 6 includes a component caused by a change in positive-phase current (positive-phase voltage fluctuation) and an unbalanced component of a voltage caused by a negative-phase current (negative-phase voltage fluctuation). In the conventional voltage detection technique, the positive-and negative-phase voltage fluctuation cannot be distinctly separated. The voltage fluctuation of bus 6 is regarded simply as a fluctuation component arbitrarily including positive-and negative-phase voltage fluctuations, and the reactive power compensation apparatus is controlled based on this. For this reason, in the conventional reactive power compensation apparatus, an object to be compensated cannot be theoretically identified, that is, it cannot be identified whether positive-phase voltage fluctuation (in particular, fluctuation caused by a positive-phase reactive current) or negative-phase voltage fluctuation, i.e., an unbalanced component of a voltage, is to be controlled. Therefore, high-precision control cannot be achieved.

A strong demand has arisen for the improvement of power quality in an AC power system and hence for a reactive power compensation apparatus for stabilizing a power system, capable of higher-precision control. In order to meet such a demand, development of a reactive power compensation apparatus comprising a high-precision voltage detection technique (positive and negative-phase voltage fluctuation detection) based on a novel control principle has received a great deal of attention.

The present invention has been made in consideration of the above situation, and has as its object to provide a reactive power compensation apparatus for compensating for an unbalanced voltage, wherein voltage fluctuation of a power supply system is separated and detected to be positive and negative components to identify objects to be compensated, thereby realizing high-precision voltage compensation control.

In order to achieve the above object, a reactive power compensation apparatus for compensating for voltage fluctuation of an AC power supply system includes: a first arithmetic circuit (403, 406, 408, 413) for synthesizing a positive-phase fundamental wave voltage signal (PIPD) from voltages (eRS, eST, eTR) of the AC power supply system; a second arithmetic circuit (403, 406, 410, 414, 415) for synthesizing negative-phase voltage signals (PIND, QIND) from the voltages (eRS, eST, eTR) of the AC power supply system; a third arithmetic circuit (420A), coupled to the first and second arithmetic circuits (413 - 415), for synthesizing current instructions (IU*, IV*, IW*) from the positive-phase fundamental wave voltage (PIPD) and the negative-phase voltage signals (PIND, QIND); and a circuit (200, 300, 500), coupled to the third arithmetic circuit (420A), for generating a reactive power corresponding to the current instructions (IU*, IV*, IW*).

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a principal circuit of a reactive power compensation apparatus to which the present invention can be applied;

Fig. 2 is a graph for explaining the principle of the operation of the reactive power compensation apparatus;

Fig. 3 is a block diagram showing a control circuit of the reactive power compensation apparatus according to an embodiment of the present invention;

Fig. 4 is a block diagram showing an arrangement of a distributor (420A) in the control circuit shown in Fig. 3;

Fig. 5 is a block diagram showing another arrangement of the distributor (420A) in the control circuit shown in Fig. 3;

Fig. 6 is a block diagram showing still another arrangement of the distributor (420A) in the control circuit shown in Fig. 3; and

Fig. 7 is a block diagram showing a control circuit of a reactive power compensation apparatus according to another embodiment of the present invention.

The principle of the present invention will be described with reference to Figs. 3 and 4. System voltages (eRS, eST, eTR) are detected, and are supplied to elements 403 and 406 in Fig. 3. Element 406 generates unit-dual-phase voltage signals (eld*, elg*) in synchronism with the system voltages. Element 403 converts triple-phase voltage signals into dual-phase signals (elds, elgs). The signals from elements 403 and 406 are supplied to elements 408 and 410 to calculate instantaneous power signals (PIP, PIN, QIN). Elements 413, 414, and 415 extract DC components (PIPD: a positive-phase fundamental wave voltage signal, PIND, QIND: first-phase negative-phase voltage signals) from signals PIP, PIN, and QIN. These DC components PIPD, PIND, and QIND are supplied to element 420A.

Fig. 4 shows the content of element 420A. Elements 421A and 424A shown in Fig. 4 respectively calculate second-and third-phase negative-phase voltages (P2ND, Q2ND, P3ND, Q3ND) using signals PIND and QIND. Element 437 sets a voltage value of a power supply system to be retained. Element 430A calculates voltage deviation signals ΔEU, ΔEV, and ΔEW using signals PIPD, PIND, QIND, P2ND, Q2ND, P3ND, and Q3ND. Amplifiers 451U, 451V, and 451W amplify signals ΔEU, ΔEV, and ΔEW to obtain current instructions IU*, IV*, and IW* of reactors. The reactive power compensation apparatus is controlled based on these instructions.

With the above control circuit, information of the system voltages can be separated and detected in the forms of a positive component (PIPD) and of negative components (PIND, QIND, P2ND, Q2ND, P3ND, and Q3ND). The reactive power compensation apparatus is controlled by the positive-/negative-phase component signals. Therefore, the objects to be compensated can be identified, and a high-precision apparatus can be realized.

A power supply system comprising a reactive power compensation apparatus of the present invention can be the same as that shown in Fig. 1 (the triple-phase system will be described hereinafter for the sake of simplicity). Therefore, a description of elements referred to in the description of Fig. 1 will be omitted.

Referring to Fig. 1, potential transformer 70 detects line voltages (eRS, eST, eTR) of AC bus 6 as an object to be compensated, and supplies the detected voltages to control circuit 350. Reactor part 300 is normally delta-connected, and levels of currents flowing through reactors 302U to 302W are adjusted by adjusting firing angles of thyristors 301U to 301W. The reactor currents have a distorted waveform including a harmonic wave component in addition to a fundamental wave.

Arithmetic circuit 400, as the characteristic feature of the present invention, receives voltage signals eRS, eST, and eTR to perform various arithmetic operations, and outputs current instructions IU*, IV*, and IW* of DC values for instructing fundamental wave currents to be flowed from reactor part 300.

Firing controller 500 is operated in response to current instructions IU*, IV*, and IW*, and firing-controls thyristors 30IU, 30IV, and 30IW to cause them to flow currents instructed by instructions IU*, IV*, and IW* through reactors 302U, 302V, and 302W.

A combination of arithmetic circuit 400 and firing controller 500 is called control circuit 350, and Fig. 3 shows the detailed circuit arrangement thereof.

The principal part of the present invention will now be described with reference to Figs. 3 and 4.

Referring to Fig. 3, triple-phase AC bus voltage signals eRS, eST, and eTR in Fig. I are input to dual phase converter 403 and dual phase signal generator 406. Converter 403 converts voltage signals eRS, eST, and eTR into dual-phase voltage signals elds and elqs using equations (I) below:

$$\left.\begin{aligned} elds &= (\sqrt{2/3})\{eRS - (eST + eTR)/2\} \\ elqs &= (\sqrt{2/3})\{(\sqrt{3/2})(eST - eTR)\} \end{aligned}\right\} \quad \ldots(1)$$

Generator 406 is constituted by a phase-locked loop circuit, and receives voltage signals eRS, eST, and eTR. If the first phase is represented by an R phase, the second phase is represented by an S phase, and the third phase is represented by a T phase, generator 406 outputs unit-sine signal eld* synchronous with line voltage eRS across the first and second phases, and unit-sine signal elq* delayed by 90 degrees therefrom. Signals eld* and elq* can be expressed by equations (2):

$$\left.\begin{aligned} eld^* &= \cos\theta RS \\ elq^* &= \sin\theta RS \end{aligned}\right\} \quad \ldots(2)$$

Arithmetic circuit 408 receives signals elds and elqs and signals eld* and elq*, and yields signal PIP using equation (3):

$$PIP = eld^* \cdot elds + elq^* \cdot elqs \quad \ldots(3)$$

When system voltages eRS, eST, and eTR include positive-/negative-phase components, PIP is a pulse current including a DC component and an AC component which is oscillated with a magnitude twice that of a fundamental wave. DC filter 4I3 outputs the DC component of signal PIP as signal PIPD. More specifically, PIPD represents a positive-phase fundamental wave voltage included in system voltages eRS, eST, and eTR.

Arithmetic circuit 4I0 receives signals elds and elqs and signals eld* and elq*, and yields signals QIN and PIN using equations (4):

$$\left.\begin{aligned} QIN &= eld^* \cdot elqs - (-elq^*) \cdot elds \\ PIN &= eld^* \cdot elds + (-elq^*) \cdot elqs \end{aligned}\right\} \quad \ldots(4)$$

When system voltages eRS, eST, and eTR include positive-/negative-phase components, PIN and QIN are pulse current signals. Signals PIN and QIN are respectively filtered through DC filters PIN and QIN, thereby detecting DC component signals PIND and QIND. Resultant signals PIND and QIND respectively represent voltages of respective components when negative-phase voltage included in line voltage eRS across the first and second phases is separated into a component (PIND) in phase with the positive-phase fundamental wave component of the line voltage across the first and second phases and a component (QIND) having a 90-degree phase difference therefrom. PIND is called a first-phase in-phase negative-phase voltage signal, and QIND is called a first-phase 90-degree-out-of-phase negative-phase voltage signal.

Distributor 420A performs arithmetic operations in response to signals PIPD, PIND, and QIND, and outputs current instructions IU*, IV*, and IW* for instructing currents to be flowed from reactor part 300 shown in Fig. I. Fig. 4 shows the detailed arrangement of distributor 420A.

Firing controller 500 is operated in response to current instructions IU*, IV*, and IW*, and firing-controls thyristors 30IU, 30IV, and 30IW to cause reactor part 300 to flow currents (fundamental waves) instructed by IU*, IV*, and IW*.

Distributor 420A will now be described with reference to Fig. 4. The signals indicated by the same reference symbols in Figs. 3 and 4 are connected accordingly. Referring to Fig. 4, arithmetic circuits 42IA and 424A receive first-phase 90-degree-out-of-phase negative-phase voltage signal QIND and first-phase in-phase negative phase voltage signal PIND, and output second-phase 90-degree-out-of-phase negative-phase voltage signal Q2ND, second-phase in-phase negative-phase voltage signal P2ND, third-phase 90-degree-out-of-phase negative-phase voltage signal Q3ND, and third-phase in-phase negative-phase voltage signal P3ND through arithmetic operations represented by equations (5) and (6).

$$\left.\begin{aligned} Q2ND &= P1ND\cdot\sin(2\pi/3) + Q1ND\cdot\cos(2\pi/3) \\ P2ND &= P1ND\cdot\cos(2\pi/3) - Q1ND\cdot\sin(2\pi/3) \end{aligned}\right\} \quad \ldots(5)$$

$$\left.\begin{aligned} Q3ND &= -P1ND\cdot\sin(2\pi/3) + Q1ND\cdot\cos(2\pi/3) \\ P3ND &= P1ND\cdot\cos(2\pi/3) + Q1ND\cdot\sin(2\pi/3) \end{aligned}\right\} \quad \ldots(6)$$

P2ND and Q2ND represent an in-phase voltage component (P2ND) and a voltage component (Q2ND) having a 90-degree phase difference therefrom obtained when the negative-phase component of line voltage eST across the second and third phases is decomposed into a component in phase with the positive-phase fundamental wave component of line voltage eST and a component having a 90-degree phase difference therefrom.

Similarly, P3ND and Q3ND represent an in-phase voltage component (P3ND) and a voltage component (Q3ND) having a 90-degree phase difference therefrom obtained when the negative-phase component of line voltage eTR across the third and first phases is decomposed into a component in phase with the positive-phase fundamental wave component of line voltage eTR and a component having a 90-degree phase difference therefrom.

Setting device 437 outputs voltage setting signal EREF* for instructing a voltage to be maintained on AC bus 6 shown in Fig. I.

Distributor 430A performs arithmetic operations represented by equations (7) presented below based on positive-phase fundamental wave voltage signal PIPD; first-, second-, and third-phase 90-degree-out-of-phase negative-phase voltage signals QIND, Q2ND, and Q3ND and in-phase negative-phase voltage signals PIND, P2ND, and P3ND; and voltage setting signal EREF*, detected from the AC bus voltages; and outputs voltage deviation signals ΔEU, ΔEV, and ΔEW.

Amplifiers 45IU, 45IV, and 45IW, constituted by proportional integrators and the like, amplify deviations ΔEU, ΔEV, and ΔEW, and output amplified results as signals IU*, IV*, and IW*. Signals IU*, IV*, and IW* are first-phase current instruction IU* for instructing a current to be flowed through first-phase reactor 302U of reactor part 300 shown in Fig. I, second-phase current instruction IV* for reactor 302V, and third-phase current instruction IW* for reactor 302W.

Distributor 430A is constituted by the following elements. More specifically, coefficient multipliers 43IA, 432A, and 433A multiply input signals by $1/\sqrt{3}$, and output the products. Adders 434A, 435A, and 436A add the outputs from multipliers 43IA, 432A, and 433A in polarities shown in Fig. 4.

The outputs from adders 434A, 435A, and 436A correspond to the arithmetic operation in the third terms of equations (7). Adder 438A adds setting signal EREF* to signal PIPD in the polarities shown in Fig. 4. More specifically, the output from adder 438A corresponds to the first term of each equation (7). Adders 439A, 440A, and 44IA add signals PIND, P2ND, P3ND, an output signal from adder 438A, and the output signals from coefficient multipliers 434A, 435A, and 436A in the polarities shown in Fig. 4, and respectively output ΔEU, ΔEV, and ΔEW in equations (7):

$$\left.\begin{aligned}\Delta EU &= (-EREF^* + P1PD) + P1ND + (1/\sqrt{3})(Q2ND - Q3ND)\\ \Delta EV &= (-EREF^* + P1PD) + P2ND + (1/\sqrt{3})(Q3ND - Q1ND)\\ \Delta EW &= (-EREF^* + P1PD) + P3ND + (1/\sqrt{3})(Q1ND - Q2ND)\end{aligned}\right\} \quad \ldots(7)$$

Signals IU*, IV*, and IW* obtained through the above arithmetic operations correspond to signals representing DC levels, each of which includes information associated with a positive-phase voltage (term PIPD) and information associated with a negative-phase voltage (terms (PIND - P3ND) and (QIND - Q3ND)). Therefore, reactor part 300 shown in Fig. I can be controlled based on signals IU*, IV*, and IW*, so that a voltage fluctuation caused by a positive-phase reactive current generated in branch line power supply lines I0 and II shown in Fig. I and by bus impedance 3, and an unbalanced voltage of bus 6 caused by a negative-phase current generated in lines I0 and II and by bus impedance 3 can be desirably stabilized and balanced.

The above is a typical arrangement of the present invention.

Referring to Fig. I, voltages of the AC bus are detected as signals eRS, eST, and eTR. In general, these voltages are unbalanced voltages including positive-and negative-phase components.

The voltages are first supplied to dual phase generator 406 shown in Fig. 3, so that dual-phase signals eld* and elq* are output based on equations (2). Dual phase generator 406 is adjusted to be responsive to only the positive-phase fundamental wave components of voltage signals eRS, eST, and eTR. Therefore, dual-phase signals include information associated with only a positive-phase fundamental wave of the voltage.

Voltage signals eRS, eST, and eTR are also input to dual phase converter 403, and are subjected to conversion represented by equations (I), thus obtaining dual-phase signals elds and elqs. The arithmetic operation given by equation (3) is performed by arithmetic circuit 408 to obtain signal PIP. Signal PIP is filtered through DC filter 4I3 to extract DC signal PIPD therefrom. Extracted signal PIPD represents a positive-phase fundamental wave voltage included in system voltages eRS, eST, and eTR.

The arithmetic operations given by equations (4) are performed by arithmetic circuit 4I0 to obtain signals PIN and QIN. Signals PIN and QIN are filtered through DC filters 4I4 and 4I5, thereby extracting DC signals PIND and QIND therefrom. Signals PIND and QIND respectively represent voltages of respective components, i.e., an in-phase voltage component (PIND) and a voltage component (QIND) having a 90-degree phase difference therefrom when the negative-phase voltage component included in line voltage eRS across the first and second phases is separated into a component in phase with the positive-phase fundamental wave component of the line voltage across the first and second phases and a component having a 90-degree phase difference therefrom. (Note that PIND will be referred to as a first phase in-phase negative-phase voltage hereinafter; and QIND will be referred to as a first-phase 90-degree-out-of-phase negative-phase voltage.)

In distributor 420A shown in Fig. 4, the arithmetic operations represented by equations (5) and (6) are performed by arithmetic circuits 42IA and 424A, thereby obtaining second-phase in-phase negative-phase voltage P2ND, second phase 90-degree-out-of-phase negative-phase voltage Q2ND, third-phase in-phase negative-phase voltage P3ND, and third-phase 90-degree-out-of-phase negative-phase voltage Q3ND.

Signal PIPD obtained as described above is a signal associated with only a positive-phase fundamental wave voltage included in system voltages eRS, eST, and eTR. More specifically, signal PIPD is a signal associated with only a component in phase with the positive-phase fundamental wave voltage. In various arithmetic operations associated with the positive-phase component of a voltage, e.g., in the conversion represented by equation (3), even if the arithmetic operation is performed for any phase, the same calculation can be determined. Therefore, the arithmetic operation for the positive-phase component need be performed only for a single phase.

Paying attention to signals PIND and QIND, signals P2ND and Q2ND, and signals P3ND and Q3ND, these signals are associated with only negative-phase components included in system voltages eRS, eST, and eTR. That is, signals PIND and QIND are associated with only the negative-phase component of voltage eRS, signals P2ND and Q2ND with that of voltage eST, and signals P3ND and Q3ND with that of voltage eTR. More specifically, in the case of PIND and QIND, PIND is associated with a voltage component in phase with the positive-phase fundamental wave component of the line voltage in the negative-phase component of voltage eRS, and QIND is associated with a voltage component having a 90-degree phase difference from the positive-phase fundamental wave voltage.

As described above, all the information of system voltages eRS, eST, and eTR are independently separated and detected in the form of signals PIPD, PIND, P2ND, P3ND, QIND, Q2ND, and Q3ND.

The signals obtained in this manner are subjected to arithmetic operations in accordance with equations (7) in distributor 430A shown in Fig. 4 to obtain voltage deviation signals ΔEU, ΔEV, and ΔEW. The resultant signals are amplified to obtain current instructions IU*, IV*, and IW*.

When the current of reactor part 300 shown in Fig. I is controlled based on current instructions IU*, IV*, and IW*, reactive power compensation apparatus I00 is operated as follows.

For example, if a negative current flows through the systems of bus 6 to cause an unbalanced voltage, this is detected by control circuit 350 (in the form of signals PIND, QIND, P2ND, Q2ND, P3ND, and Q3ND shown in Fig. 4). Based on these signals, reactor part 300 generates a compensation negative-phase current to cancel the unbalanced voltage (to have a phase opposite to that of a negative phase current supplied from the load to the systems). Therefore, the negative-phase current cannot be apparently flowed through impedance 3 shown in Fig. I, and the unbalanced voltage of bus 6 caused thereby can be removed. Note that since distributor 420A shown in Fig. 4 includes amplifiers 45IU, 45IV, and 45IW each comprising a proportional integrator, the compensation operation can be executed until the negative-phase voltage of the systems can be completely reduced to zero.

When a reactive current flows through the system to change the system voltage, this is detected by control circuit 350 (signal PIPD shown in Fig. 4), and the current of reactor part 300 is adjusted based on the comparison result between the detected voltage and voltage setting value EREF*. For example, if the voltage of the systems is decreased, the reactor current is reduced. Thus, as can be seen from the description of Fig. 2, the phase of a current (IR) generated from reactive power compensation apparatus I00 is advanced, the voltage of system bus 6 is increased (i.e., when a phase-advanced current is flowed through inductance 3, the voltage of bus 6 is increased), and the bus voltage is maintained at the set value. When the voltage of bus 6 is increased, reactive power compensation apparatus I00 generates a delayed current (IR) to decrease the voltage of system bus 6, and hence, the voltage of system bus 6 is maintained at a set value (EREF*).

As can be seen from the above description, in the power supply system comprising the reactive power compensation apparatus according to the present invention, if a voltage fluctuation is caused by reactive power fluctuation in the load, or if a voltage unbalance is caused by a negative-phase current, they can be compensated for by the reactive power compensation apparatus. Therefore, a high-quality power with less voltage fluctuation and a balanced voltage can be supplied.

The typical embodiment of the present invention has been described above.

As the invention related to the present invention, there is European Patent Application No. 86II2529.2 (filed on September I0, I986) corresponding to Japanese Patent Application Nos. 60-200010 and 60-200012. All the disclosures of European Patent Application No. 86II2529.2 are incorporated in the present application.

The invention of European Patent Application No. 86II2529.2 can be applied only to a specific reactive power compensation control directed to a specific load such as an arc furnace equipped for a factory. In such an application, the configuration of a power system has to be simple, and the direction of a current-flow of the power system must be actually specified so as to be able to detect the current. More specifically, in that application, a power source and a load, mutually connected to each other via a power system, must be clearly distinguished in the compensation control.

In addition, the invention of European Patent Application No. 86II2529.2 depends on a current detection to achieve the reactive power compensation control. For this reason, if the voltage of the power system is increased or decreased continuously, this control cannot compensate for the voltage increase or decrease, so that no constant voltage is obtained for the power system.

In contrast, the present invention can be applied to a reactive power compensation control generally directed to various loads such as power transmission systems. In such an application, the configuration of a power system may be complex, and the direction of a current-flow of the power system may not be actually specified so as to disable the current detection. In other words, in that application, a power source and a load, mutually connected to each other via a power system, may be undefined.

In addition, the present invention depends on a voltage detection, not on a current detection, to achieve the reaction power compensation control. For this reason, the compensation control serves to provide a controlled voltage source. Consequently, even if the voltage of the power system is increased or decreased, the control can compensate for the voltage increase or decrease so that a constant voltage is obtained for the power system.

As mentioned above, the present invention materially differs from the invention of European Patent Application No. 86II2529.2 with respect to the application, the manner of practicing, and the effect. Which invention (the present invention or the invention of European Patent Application No. 86II2529.2) should be used depends on the target of the compensation control.

Note that dual phase generator 406 shown in Fig. 3 can be arranged the same as that in Fig. 7 of European Patent Application No. 86II2529.2. In this case, $\cos\theta$ldl* and $-\sin\theta$ldl* in Fig. 7 of the European patent replace eld* and elq* in Fig. 3 of the present invention.

Another embodiment of the present invention will now be described with reference to Fig. 5. Fig. 5 shows a modification of distributor 420A shown in Fig. 5 according to the present invention. The circuit shown in Fig. 5 is inserted in distributor 420A shown in Fig. 3. Therefore, most of this modification encompasses the above embodiment of the present invention, and a description of the identical portions will be omitted. The portions indicated by the identical symbols in Figs. 5 and 3 are connected according to the symbols.

Referring to Fig. 5, arithmetic circuits 42IB and 424B receive first-phase 90-degree-out-of-phase negative-phase voltage signal QIND and first-phase in-phase negative-phase current signal PIND described above, and output second-phase in-phase negative-phase voltage signal P2ND and third-phase in-phase negative-phase P3ND through the arithmetic operations represented by equations (8) and (9) as follows:

$$P2ND = PIND \cdot \cos(2\pi/3) - QIND \cdot \sin(2\pi/3) \quad ...(8)$$

$$P3ND = PIND \cdot \cos(2\pi/3) + QIND \cdot \sin(2\pi/3) \quad ...(9)$$

P2ND and P3ND are the same as signals P2ND and P3ND obtained from equations (5) and (6) in the above embodiment.

Setting device 437 outputs voltage setting signal EREF*. Distributor 430B receives positive-phase fundamental wave voltage signal PIPD, first-, second-, and third-phase in-phase negative-phase voltage signals PIND, P2ND, and P3ND, and voltage setting signal EREF*, and performs the arithmetic operations represented by equations (I0) based on these signals, thereby outputting voltage deviation signals ΔEU, ΔEV, and ΔEW:

$$\left.\begin{aligned} \Delta EU &= (-EREF^* + P1PD) + 2 \cdot P1ND \\ \Delta EV &= (-EREF^* + P1PD) + 2 \cdot P2ND \\ \Delta EW &= (-EREF^* + P1PD) + 2 \cdot P3ND \end{aligned}\right\} \quad ...(10)$$

Amplifiers 45IU, 45IV, and 45IW comprising proportional integrators respectively amplify deviation signals ΔEU, ΔEV, and ΔEW and output first-, second-, and third-phase current instructions IU*, IV*, and IW*. Note that coefficient multipliers 446B, 447B, and 448B respectively multiply the input signals by 2 and output the obtained results. Adders 438A, 439B, 440B, and 44IB add the signals shown in Fig. 5 in the polarities shown therein.

Current instructions IU*, IV*, and IW* are quite similar to those obtained in Fig. 4. Therefore, when the current of reactor part 300 shown in Fig. I is controlled based on instructions IU*, IV*, and IW*, the same compensation effect as that in the embodiment shown in Figs. 3 and 4 can be obtained.

In this modification, the arithmetic operations in arithmetic circuits 42IB and 424B shown in Fig. 5 can be simpler than those in arithmetic circuits 42IA and 424A shown in Fig. 4.

Still another embodiment of the present invention will now be described with reference to Fig. 6. This embodiment is also associated with a modification of Fig. 4, and the circuit shown in Fig. 6 is inserted in distributor 420A shown in Fig. 3. Therefore, a description of the portions identical to those in the above embodiments will be omitted.

Referring to Fig. 6, arithmetic circuits 42IC and 424C receive first-phase 90-degree-out-of-phase negative-phase voltage signal QIND and first-phase in-phase negative-phase current signal PIND described above, and output second-phase 90-degree-out-of-phase negative-phase voltage signal Q2ND and third-phase 90-degree-out-of-phase negative-phase Q3ND through the arithmetic operations represented by equations (II) and (I2). Q2ND and Q3ND are the same as signals Q2ND and Q3ND obtained from equations (5) and (6) in the above embodiment.

$$Q2ND = PIND \cdot \sin(2\pi/3) + QIND \cdot \cos(2\pi/3) \quad ...(II)$$

$$Q3ND = -PIND \cdot \sin(2\pi/3) + QIND \cdot \cos(2\pi/3) \quad ...(I2)$$

Setting device 437 outputs voltage setting signal EREF*. Distributor 430C receives positive-phase fundamental wave voltage signal PIPD, first-, second-, and third-phase 90-degree-out-of-phase negative-phase voltage signals QIND, Q2ND, and Q3ND, and voltage setting signal EREF*, and performs the arithmetic operations represented by equations (I3) based on these signals, thereby outputting voltage deviation signals ΔEU, ΔEV, and ΔEW:

$$\left.\begin{aligned}\Delta EU &= (-EREF^* + P1PD) + (2/\sqrt{3})(Q2ND - Q3ND)\\ \Delta EV &= (-EREF^* + P1PD) + (2/\sqrt{3})(Q3ND - Q1ND)\\ \Delta EW &= (-EREF^* + P1PD) + (2/\sqrt{3})(Q1ND - Q2ND)\end{aligned}\right\} \quad \ldots(13)$$

Amplifiers 45IU, 45IV, and 45IW, comprising proportional integrators, respectively amplify deviation signals ΔEU, ΔEV, and ΔEW and output first-, second-, and third-phase current instructions IU*, IV*, and IW*. Note that coefficient multipliers 43IA, 432A, and 433A respectively multiply the input signals by (I/√3), and output the products. Coefficient multipliers 446B, 447B, and 448B respectively multiply the input signals by 2 and output the products. Furthermore, adders 438A, 439B, 440B, 44IB, 434A, 435A, and 436A respectively add the signals shown in Fig. 6 in the corresponding polarities shown therein.

Current instructions IU*, IV*, and IW* are the same as those obtained in Fig. 4. Therefore, when the current of reactor part 300 shown in Fig. I is controlled based on instructions IU*, IV*, and IW*, the same compensation effect as that in the embodiment shown in Figs. 3 and 4 can be obtained.

In this modification, the arithmetic operations in arithmetic circuits 42IC and 424C shown in Fig. 6 can be simpler than those in arithmetic circuits 42IA and 424A shown in Fig. 4.

Another embodiment of the present invention will now be described with reference to Fig. 7.

Referring to Fig. 7, AC bus voltage signals eRS, eST, and eTR shown in Fig. I are input to dual phase converter 403X and dual phase signal generator 406X. Dual phase converter 403X converts voltage signals eRS, eST, and eTR into dual-phase voltage signal elds and elqs through the arithmetic operations shown in equations (I) given above. Dual phase signal generator 406X comprises a phase-locked loop circuit. Generator 406X receives voltage signals eRS, eST, and eTR, and outputs unit-sine signal eldI* synchronous with line voltage eRS across the first and second phases, unit-sine signal elqI* advanced from signal eldI* by 90 degrees, and its phase signal θldI* if the first phase shown in Fig. I is referred to as an R phase; the second phase, an S phase, and the third phase, a T phase. Signals eldI* and elqI* can be represented by equations (I4) below. (The detailed arrangement of generator 406X can be the same as that shown in Fig. 7 of the above-mentioned U.S. Patent Application No. 903,957.)

$$\left.\begin{aligned}eld1^* &= \cos\theta ld1^*\\ elq1^* &= -\sin\theta ld1^*\end{aligned}\right\} \quad \ldots(14)$$

Dual phase generator 407X is operated in response to phase angle signal θldI* and generates dual phase voltage signals eld2* and elq2* each having a frequency twice the AC bus voltage frequency and represented by equations (I5):

$$\left.\begin{aligned}eld2^* &= \cos 2\theta ld1^*\\ elq2^* &= \sin 2\theta ld1^*\end{aligned}\right\} \quad \ldots(15)$$

Arithmetic circuit 404X receives signals elds and elqs and signals eldI* and elqI*, and yields signals QIN and PIN through equations (I6):

$$\left.\begin{aligned} QIN &= eld1^{*} \cdot elqs - elq1^{*} \cdot elds \\ PIN &= eld1^{*} \cdot elds + elq1^{*} \cdot elqs \end{aligned}\right\} \quad \ldots(16)$$

When system voltages eRS, eST, and eTR include positive-/negative-phase components, QIN and PIN are pulse currents including DC and AC components which are oscillated at a frequency twice that of the fundamental wave.

Separator 409X comprises DC filters 410X and 411X and adders 412X and 413X. Separator 409X receives signals PIN and QIN. The DC components are detected by DC filters 410X and 411X, and the detected components are output as signals PIND and QIND. Separator 409x removes the DC components, i.e., PIND and QIND from signals PIN and QIN by adders 412X and 413X, and outputs only the AC components as signals PINA and QINA. Signals PIND and QIND obtained as described above respectively represent voltages of respective components when the negative-phase voltage component included in line voltage eRS across the first and second phases is separated into a component (PIND) in phase with a positive-phase fundamental wave voltage of the line voltage across the first and second phases and a component (QIND) having a 90-degree phase difference therefrom. Note that hereinafter, when PIND is referred to, it will relate to a first-phase in-phase negative-phase voltage signal, and QIND will relate to a firstphase 90-degree-out-of-phase negative-phase voltage signal.

Arithmetic circuit 408x receives signals PINA and QINA, and signals eld2* and elq2*, and calculates signal PIPD in accordance with equation (17):

$$PIPD = eld2^{*} \bullet PINA + elq2^{*} \bullet QINA \quad \ldots(17)$$

Signal PIPD is a DC signal, and represents the positive-phase fundamental wave voltage included in system voltages eRS, eST, and eTR.

Distributor 420A performs the arithmetic operations upon reception of signals PIPD, PIND, and QIND, and outputs current instructions IU*, IV*, and IW* for instructing a current to be flowed from reactor part 300 shown in Fig. 1. The arrangement of distributor 420A can be any of Figs. 4 to 6.

Firing controller 500 is operated upon reception of current instructions IU*, IV*, and IW*, and firing-controls thyristors 301U, 301V, and 301W so that reactor part 300 supplies the currents (fundamental wave) instructed by instructions IU*, IV*, and IW*. The following operation of Fig. 7 is the same as that in Fig. 3.

As can be seen from the above description, the reactive power compensation apparatus of the present invention can provide the following effects.

(1) When a fluctuating or unbalanced load is connected to an AC power supply system, voltage fluctuation and voltage unbalance of the AC bus provide problems. However, according to the present invention, whether these fluctuations are caused by positive-or negative-phase components can be clearly differentiated. Therefore, an object to be compensated of the reactive power compensation circuit can be identified. As a result, control with respect to only the voltage fluctuation of the system (voltage fluctuation control), control with respect to only the unbalanced voltage of the system (voltage balance control), control with respect to both the objects to be controlled, and the like can be desirably achieved, and high-precision voltage compensation control can be easily realized as compared to the conventional apparatus.

(2) The positive-and negative-phase components of the system voltages can be continuously detected in the form of DC signals, and hence, the control experiences no discontinuity, thereby realizing stable control.

(3) In the control circuit, when the positive-and negative-phase components of the voltage are to be detected, simple elements such as coefficient multipliers, adders, multipliers, and the like are adopted as a signal processing means, and desired signals can be obtained through simple arithmetic operations. Therefore, the detection signals include no variations, and accurate high-precision signals (associated with positive-and negative-phase components) can be obtained. Since the circuit is simple, the cost can also be reduced.

According to the reactive power compensation apparatus of the present invention as described above, since a novel control concept that "positive-and negative-phase components are separately detected and compensation control is made based on these detection results" is employed, complicated and high-precision reactive power compensation control can be performed.

Claims

1. A reactive power compensation apparatus for compensating for voltage fluctuation of an AC power supply system, comprising:

first arithmetic means (403, 406, 408, 413) for synthesizing a positive-phase fundamental wave voltage signal (PIPD) from voltages (eRS, eST, eTR) of the AC power supply system;

second arithmetic means (403, 406, 410, 414, 415) for synthesizing negative-phase voltage signals (PIND, QIND) from the voltages (eRS, eST, eTR) of the AC power supply system;

third arithmetic means (420A), coupled to said first and second arithmetic means (413 - 415), for synthesizing current instructions (IU*, IV*, IW*) from the positive-phase fundamental wave voltage (PIPD) and the negative-phase voltage signals (PIND, QIND); and

means (200, 300, 500), coupled to said third arithmetic means (420A), for generating a reactive power corresponding to the current instructions (IU*, IV*, IW*).

2. A reactive power compensation apparatus for compensating for voltage fluctuation of an AC power supply system, comprising:

first conversion means (403) for converting voltages (eTS, eST, eTR) of the AC power supply system into dual phase voltage signals (eIds, eIqs);

second conversion means (406) for converting the voltages (eTS, eST, eTR) of the AC power supply system into unit-dual-phase voltage signals (eId*, eIq*);

first synthesizing means (408, 413), coupled to said first and second conversion means (403, 406), for synthesizing a positive-phase fundamental wave voltage signal (PIPD) from the dual phase voltage signals (eIds, eIqs) and the unit-dual-phase voltage signals (eId*, eIq*);

second synthesizing means (410, 414, 415), coupled to said first and second conversion means (403, 406), for synthesizing negative-phase voltage signals (PIND, QIND) from the dual phase voltage signals (eIds, eIqs) and the unit-dual-phase voltage signals (eId*, eIq*);

third synthesizing means (420A), coupled to said first and second synthesizing means (413 - 415), for synthesizing current instructions (IU*, IV*, IW*) from the positive-phase fundamental wave voltage signal (PIPD) and the negative-phase voltage signals (PIND, QIND); and

means (200, 300, 500), coupled to said third synthesizing means (420A), for supplying a reactive power corresponding to the current instructions (IU*, IV*, IW*) to the AC power supply system (4).

3. A reactive power compensation apparatus for compensating for an unbalanced voltage and voltage fluctuation of a multi-phase AC power supply system (4), comprising:

first means (406) for, if N is an integer not less than 2, generating, from multi-phase voltages (e1s, e2s,..., eNs) of the N-phase multi-phase AC power supply system, unit-sine signal eId*, synchronous with a first-phase voltage (e1s), and unit-sine signal eIq*, whose phase is delayed by substantially 90 degrees from unit-sine signal eId*;

second means (403) for generating dual phase voltage signal eIds and dual phase voltage signal eIqs from the multi-phase voltages (e1s, e2s,..., eNs) by dual-phase conversion which has d and q axes and in which the d axis is in-phase with the first-phase voltage (e1s);

third means (408, 410) for generating signals PIP, PIN, and QIN from unit-sine signals eId*, eIq* and dual phase voltage signals eIds and eIqs in accordance with the following arithmetic operations:

$$PIP = eId^* \cdot eIds + eIq^* \cdot eIqs$$

$$PIN = eId^* \cdot eIds - eIq^* \cdot eIqs$$

$$QIN = eId^* \cdot eIqs + eIq^* \cdot eIds$$

fourth means (413) for generating signal PIPD corresponding to a detected DC component of signal PIP;

fifth means (414, 415) for generating signals PIND and QIND corresponding to detected DC components of signals PIN and QIN; and

sixth means (420A) for generating first-to Nth-phase current instructions (IU*, IV*, IW*,...) of the N-phase multi-phase AC power supply system from signals PIPD, PIND, and QIND,

wherein said reactive power compensation apparatus compensates for the unbalanced voltage and the voltage fluctuation of the multi-phase AC power supply system (4) based on the first-to Nth-phase current instructions (IU*, IV*, IW*,...).

4. An apparatus according to claim 3, characterized in that said sixth means (420A) includes:

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (421A, 424A) for generating signals P2ND, Q2ND, P3ND, and Q3ND from signals PIND and QIND using the following arithmetic operations:

P2ND = PIND•cos(2π/3) - QIND•sin(2π/3)
Q2ND = PIND•sin(2π/3) + QIND•cos(2π/3)
P3ND = PIND•cos(2π/3) + QIND•sin(2π/3)
Q3ND = -PIND•sin(2π/3) + QIND•cos(2π/3)

second arithmetic means (430A) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, QIND, Q2ND, Q3ND, PIND, P2ND and P3ND through the following arithmetic operations:

ΔEU = -EREF* + PIPD + PIND + (Q2ND - Q3ND)/√3
ΔEV = -EREF* + PIPD + P2ND + (Q3ND - QIND)/√3
ΔEW = -EREF* + PIPD + P3ND + (QIND - Q2ND)/√3

and

current instruction means (45IU, 45IV, 45IW) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

5. An apparatus according to claim 3, characterized in that said sixth means (420A) includes:

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (42IB, 424B) for generating signals P2ND and P3ND from signals PIND and QIND using the following arithmetic operations:

P2ND = PIND•cos(2π/3) - QIND•sin(2π/3)
P3ND = PIND•cos(2π/3) + QIND•sin(2π/3)

second arithmetic means (430B) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, PIND, P2ND, and P3ND through the following arithmetic operations:

ΔEU = -EREF* + PIPD + 2•PIND
ΔEV = -EREF* + PIPD + 2•P2ND
ΔEW = -EREF* + PIPD + 2•P3ND

and

current instruction means (45IU, 45IV, 45IW) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

6. An apparatus according to claim 3, characterized in that said sixth means (420A) includes:

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (42IC, 424C) for generating signals Q2ND and Q3ND from signals PIND and QIND using the following arithmetic operations:

Q2ND = PIND•sin(2π/3) + QIND•cos(2π/3)
Q3ND = -PIND•sin(2π/3) + QIND•cos(2π/3)

second arithmetic means (430C) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, QIND, Q2ND, and Q3ND through the following arithmetic operations:

ΔEU = -EREF* + PIPD + 2•(Q2ND - Q3ND)/√3
ΔEV = -EREF* + PIPD + 2•(Q3ND - QIND)/√3
ΔEW = -EREF* + PIPD + 2•(QIND - Q2ND)/√3

and

current instruction means (45IU, 45IV, 45IW) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

7. A reactive power compensation apparatus for compensating for an unbalanced voltage and voltage fluctuation of a multi-phase AC power supply system (4) comprising

first means (406X) for, if N is an integer not less than 2, generating, from multi-phase voltages (els, e2s,..., eNs) of the N-phase multi-phase AC power supply system, unit-sine signal eldl* which changes synchronously with a first-phase voltage (els), unit-sine signal elql* whose phase is advanced by substantially 90 degrees from unit-sine signal eldl*, and phase angle signal θldl* indicating a phase of unit-sine signal eldl*;

second means (403X) for generating dual phase voltage signal elds and dual phase voltage signal elqs from the multi-phase voltages (els, e2s,..., eNs) by dual-phase conversion which has d and q axes and in which the d axis is in-phase with the first-phase voltage (els);

third means (404X) for generating signals PIN and QIN from unit-sine signals eldl* and elql* and dual phase voltage signals elds and elqs in accordance with the following arithmetic operations:

PIN = eldl*•elds + elql*•elqs

QIN = eldl*•elqs - elql*•elds

fourth means (410X, 411X) for generating signals PIND and QIND corresponding to detected DC components of signals PIN and QIN;

fifth means (412X, 413X) for generating signals PINA and QINA corresponding to detected AC components of signals PIN and QIN;

sixth means (407X) for generating, based on phase angle signal θldl*, unit-sine wave signal eld2* which changes at phase angle 2.θldl* and unit-sine signal elq2* whose phase is delayed by substantially 90 degrees from unit-sine signal eld2*;

seventh means (408X) for generating signal PIPD based on unit-sine signals eld2* and elq2* and AC component detection signals PINA and QINA through the following arithmetic operation:

PIPD = eld2*•PINA + elq2*•QINA

and

eighth means (420A) for generating first-to Nth-phase current instructions (IU*, IV*, IW*,...) for the N-phase multi-phase AC power supply system from signals PIPD, PIND, and QIND,

wherein said reactive power compensation apparatus compensates for the unbalanced voltage and the voltage fluctuation of the multi-phase AC power supply system (4) based on the first-to Nth-phase current instructions (IU*, IV*, IW*,...).

8. An apparatus according to claim 7, characterized in that said eighth means (420A) includes

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (421A, 424A) for generating signals P2ND, Q2ND, P3ND, and Q3ND from signals PIND and QIND using the following arithmetic operations:

$P2ND = PIND \bullet \cos(2\pi/3) - QIND \bullet \sin(2\pi/3)$

$Q2ND = PIND \bullet \sin(2\pi/3) + QIND \bullet \cos(2\pi/3)$

$P3ND = PIND \bullet \cos(2\pi/3) + QIND \bullet \sin(2\pi/3)$

$Q3ND = -PIND \bullet \sin(2\pi/3) + QIND \bullet \cos(2\pi/3)$

second arithmetic means (430A) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, QIND, Q2ND, Q3ND, PIND, P2ND and P3ND through the following arithmetic operations:

$\Delta EU = -EREF^* + PIPD + PIND + (Q2ND - Q3ND)/\sqrt{3}$

$\Delta EV = -EREF^* + PIPD + P2ND + (Q3ND - QIND)/\sqrt{3}$

$\Delta EW = -EREF^* + PIPD + P3ND + (QIND - Q2ND)/\sqrt{3}$

and

current instruction means (451U, 451V, 451W) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

9. An apparatus according to claim 7, characterized in that said eighth means (420A) includes:

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (421B, 424B) for generating signals P2ND and P3ND from signals PIND and QIND using the following arithmetic operations:

$P2ND = PIND \bullet \cos(2\pi/3) - QIND \bullet \sin(2\pi/3)$

$P3ND = PIND \bullet \cos(2\pi/3) + QIND \bullet \sin(2\pi/3)$

second arithmetic means (430B) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, PIND, P2ND, and P3ND through the following arithmetic operations:

$\Delta EU = -EREF^* + PIPD + 2 \bullet PIND$

$\Delta EV = -EREF^* + PIPD + 2 \bullet P2ND$

$\Delta EW = -EREF^* + PIPD + 2 \bullet P3ND$

and

current instruction means (451U, 451V, 451W) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

10. An apparatus according to claim 7, characterized in that said eighth means (420A) includes:

setting signal generating means (437) for generating system voltage setting signal EREF* for setting the voltage of the AC power supply system (4) to be maintained by the operation of said reactive power compensation apparatus;

first arithmetic means (421C, 424C) for generating signals Q2ND and Q3ND from signals PIND and QIND using the following arithmetic operations:

$Q2ND = PIND \bullet \sin(2\pi/3) + QIND \bullet \cos(2\pi/3)$

$Q3ND = -PIND \bullet \sin(2\pi/3) + QIND \bullet \cos(2\pi/3)$

second arithmetic means (430C) for generating voltage deviation signals ΔEU, ΔEV, and ΔEW from signals EREF*, PIPD, QIND, Q2ND, and Q3ND through the following arithmetic operations:

$\Delta EU = -EREF^* + PIPD + 2 \bullet (Q2ND - Q3ND)/\sqrt{3}$

$\Delta EV = -EREF^* + PIPD + 2 \bullet (Q3ND - QIND)/\sqrt{3}$

$\Delta EW = -EREF^* + PIPD + 2 \bullet (QIND - Q2ND)/\sqrt{3}$

and

current instruction means (45IU, 45IV, 45IW) for amplifying voltage deviation signals ΔEU, ΔEV, and ΔEW and generating current instructions IU*, IV*, and IW* corresponding to the voltage deviation signals.

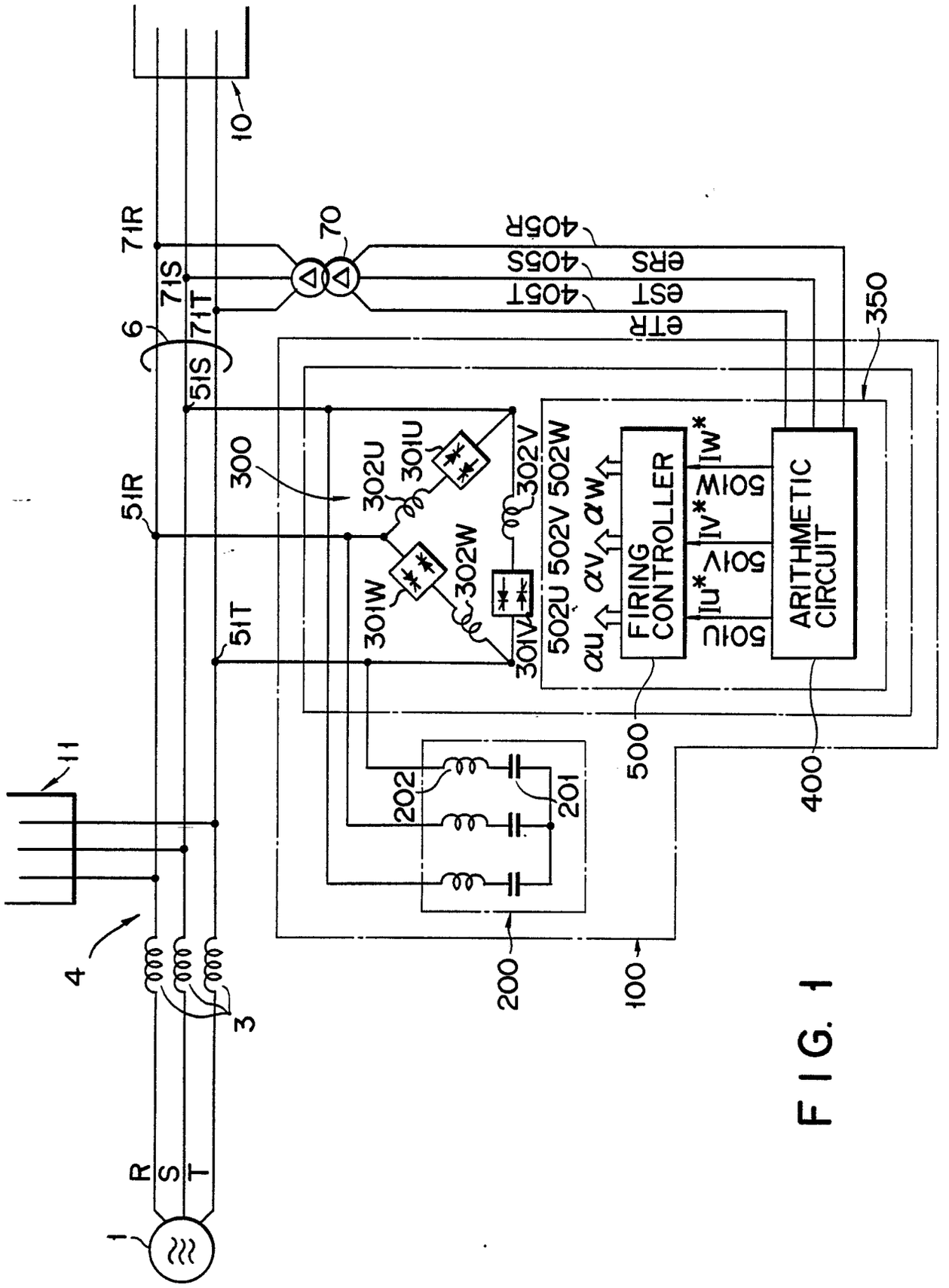
10
71R
71S
71T
70
6
51S
51R
51T
405R
405S
405T
eRS
eST
eTR
350
300
302U
301U
302V
301V
302W
301W
502U 502V 502W
αU αV αW
FIRING CONTROLLER
501U*
501V*
501W*
ARITHMETIC CIRCUIT
500
400
202
201
200
100
11
4
3
R
S
T
1

FIG. 1

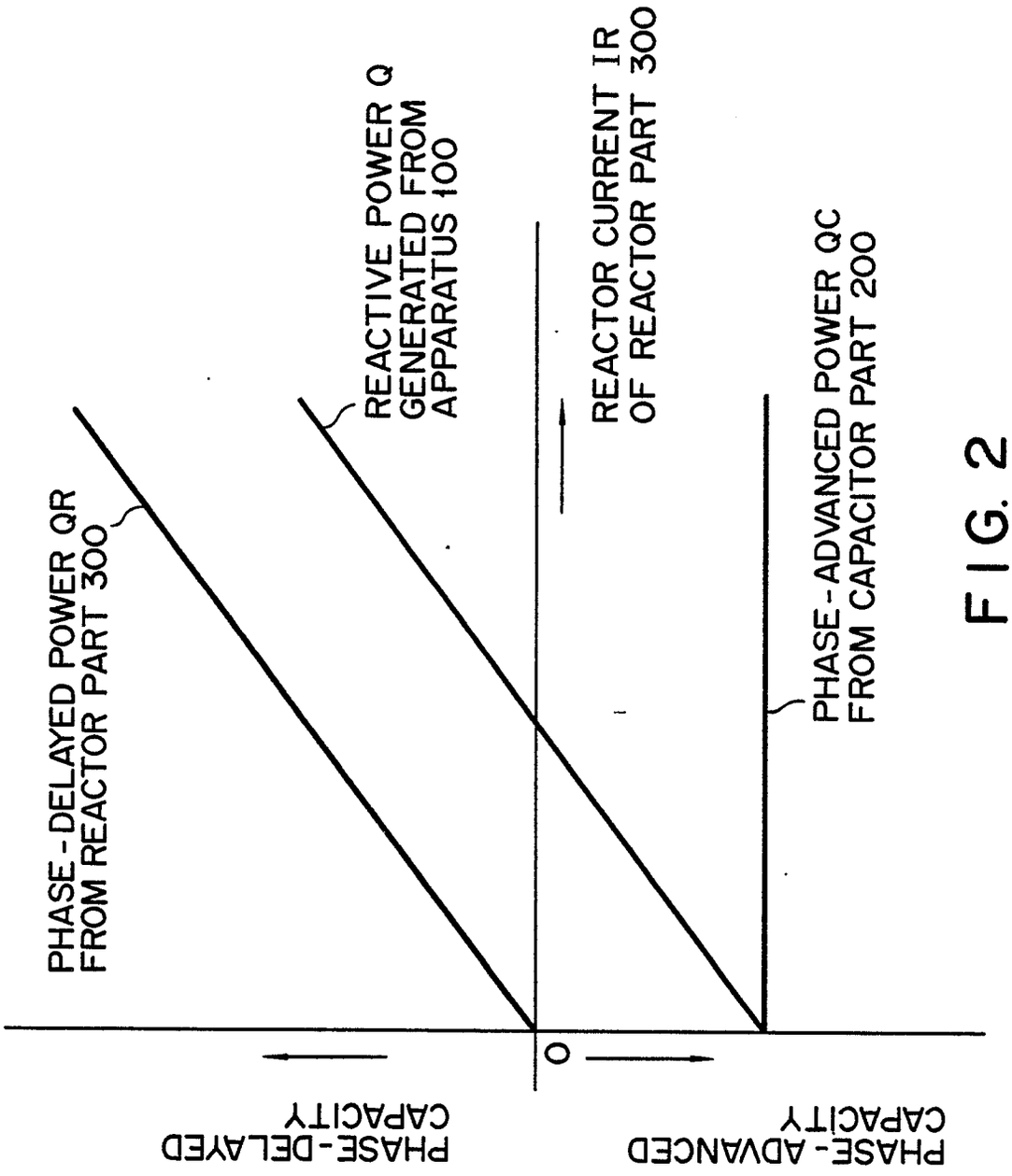
PHASE-DELAYED POWER QR
FROM REACTOR PART 300
REACTIVE POWER Q
GENERATED FROM
APPARATUS 100
REACTOR CURRENT IR
OF REACTOR PART 300
PHASE-ADVANCED POWER QC
FROM CAPACITOR PART 200
0
PHASE-DELAYED
CAPACITY
PHASE-ADVANCED
CAPACITY

FIG. 2

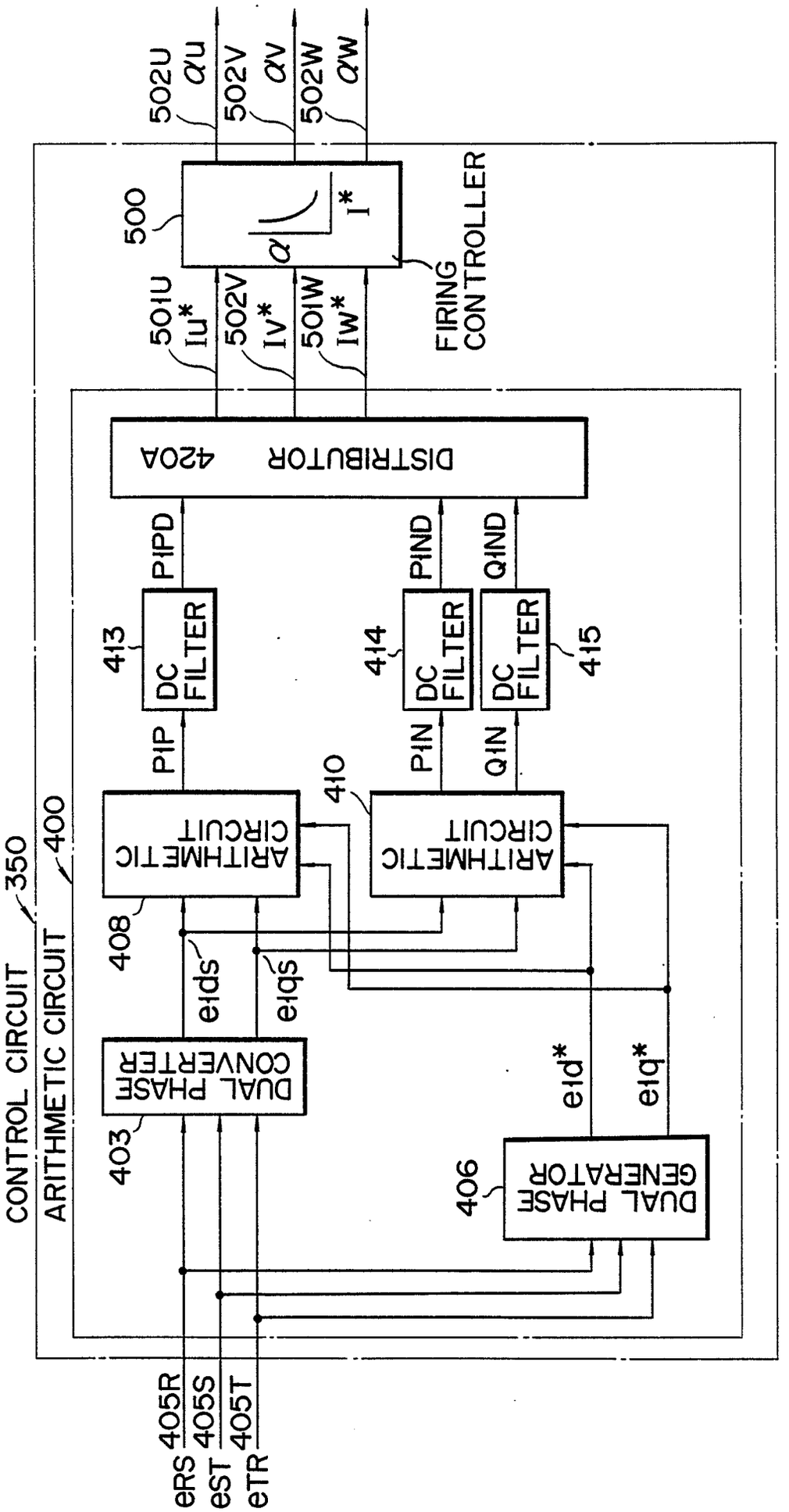
CONTROL CIRCUIT
350
ARITHMETIC CIRCUIT
400
405R
405S
405T
eRS
eST
eTR
DUAL PHASE CONVERTER
403
408
e1ds
e1qs
ARITHMETIC CIRCUIT
410
P1P
Q1P
P1N
Q1N
DC FILTER
413
414
415
P1PD
P1ND
Q1ND
DISTRIBUTOR
420A
DUAL PHASE GENERATOR
406
e1d*
e1q*
500
FIRING CONTROLLER
501U
Iu*
502V
Iv*
501W
Iw*
502U
αu
502V
αv
502W
αw

FIG. 3

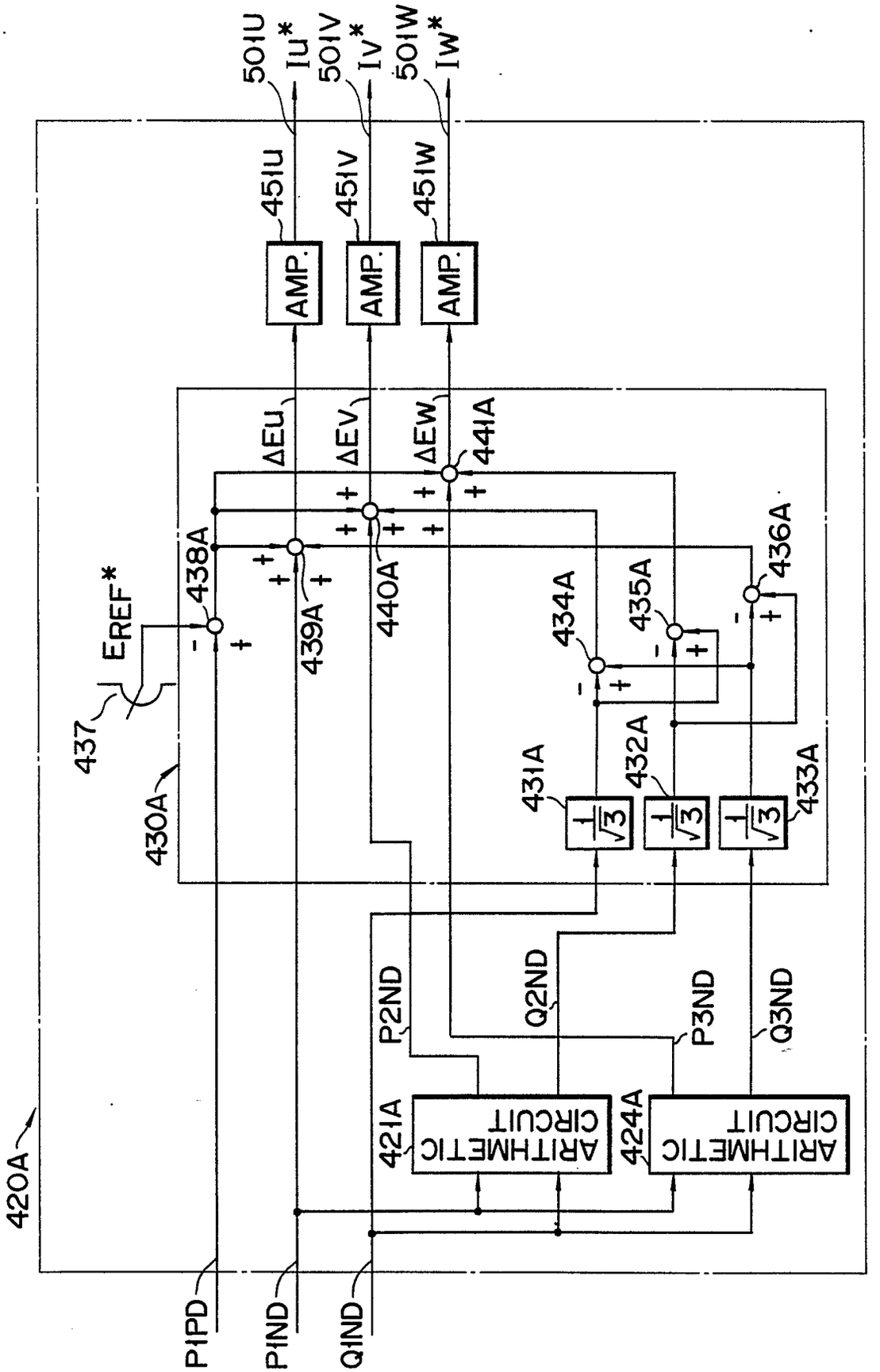
501U
Iu*
501V
Iv*
501W
Iw*
451U
451V
451W
AMP.
AMP.
AMP.
ΔEu
ΔEV
ΔEW
441A
438A
439A
440A
EREF*
437
430A
434A
435A
436A
431A
432A
433A
1/√3
1/√3
1/√3
P2ND
Q2ND
P3ND
Q3ND
420A
421A
424A
ARITHMETIC CIRCUIT
ARITHMETIC CIRCUIT
P1PD
P1ND
Q1ND

FIG. 4

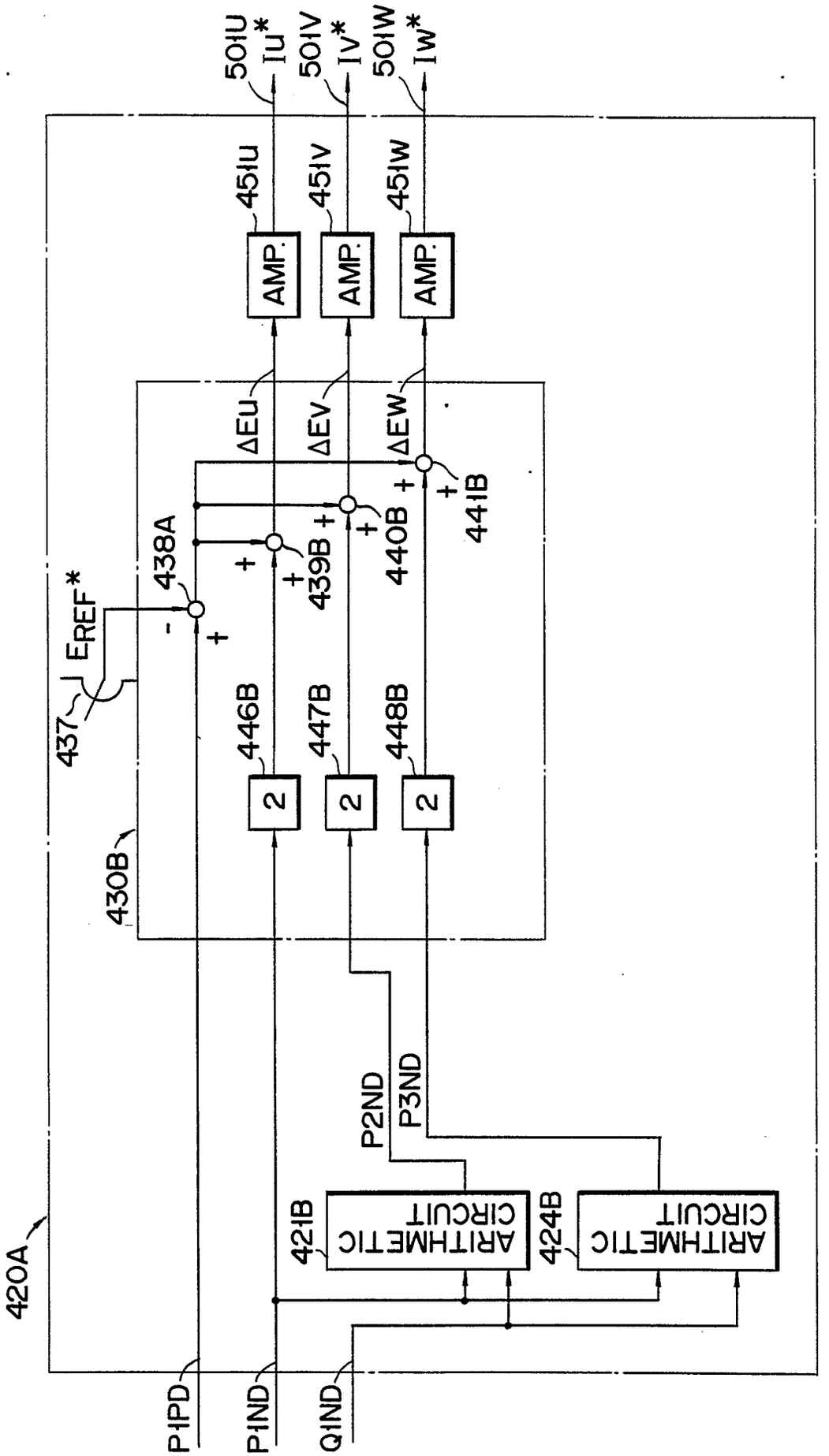
501U
Iu*
501V
Iv*
501W
Iw*
451U
451V
451W
AMP.
AMP.
AMP.
ΔEU
ΔEV
ΔEW
441B
440B
439B
438A
EREF*
437
446B
447B
448B
2
2
2
430B
420A
P2ND
P3ND
421B
ARITHMETIC CIRCUIT
424B
ARITHMETIC CIRCUIT
P1PD
P1ND
Q1ND

FIG. 5

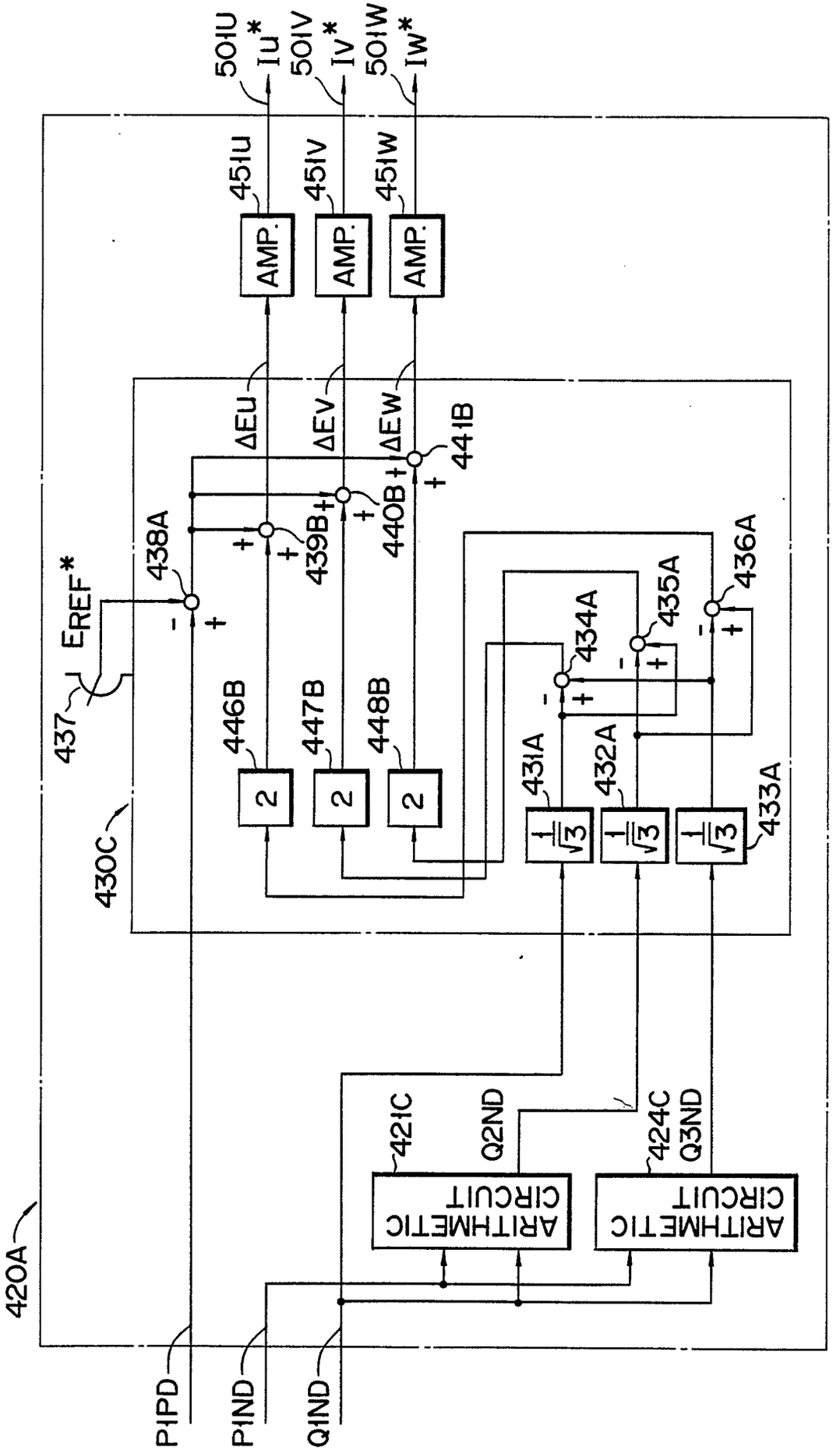
501U
Iu*
501V
Iv*
501W
Iw*
451U
451V
451W
AMP.
AMP.
AMP.
ΔEU
ΔEV
ΔEW
441B
440B
439B
438A
EREF*
437
446B
447B
448B
2
2
2
430C
431A
432A
433A
434A
435A
436A
421C
Q2ND
424C
Q3ND
ARITHMETIC CIRCUIT
ARITHMETIC CIRCUIT
420A
P1PD
P1ND
Q1ND

FIG. 6

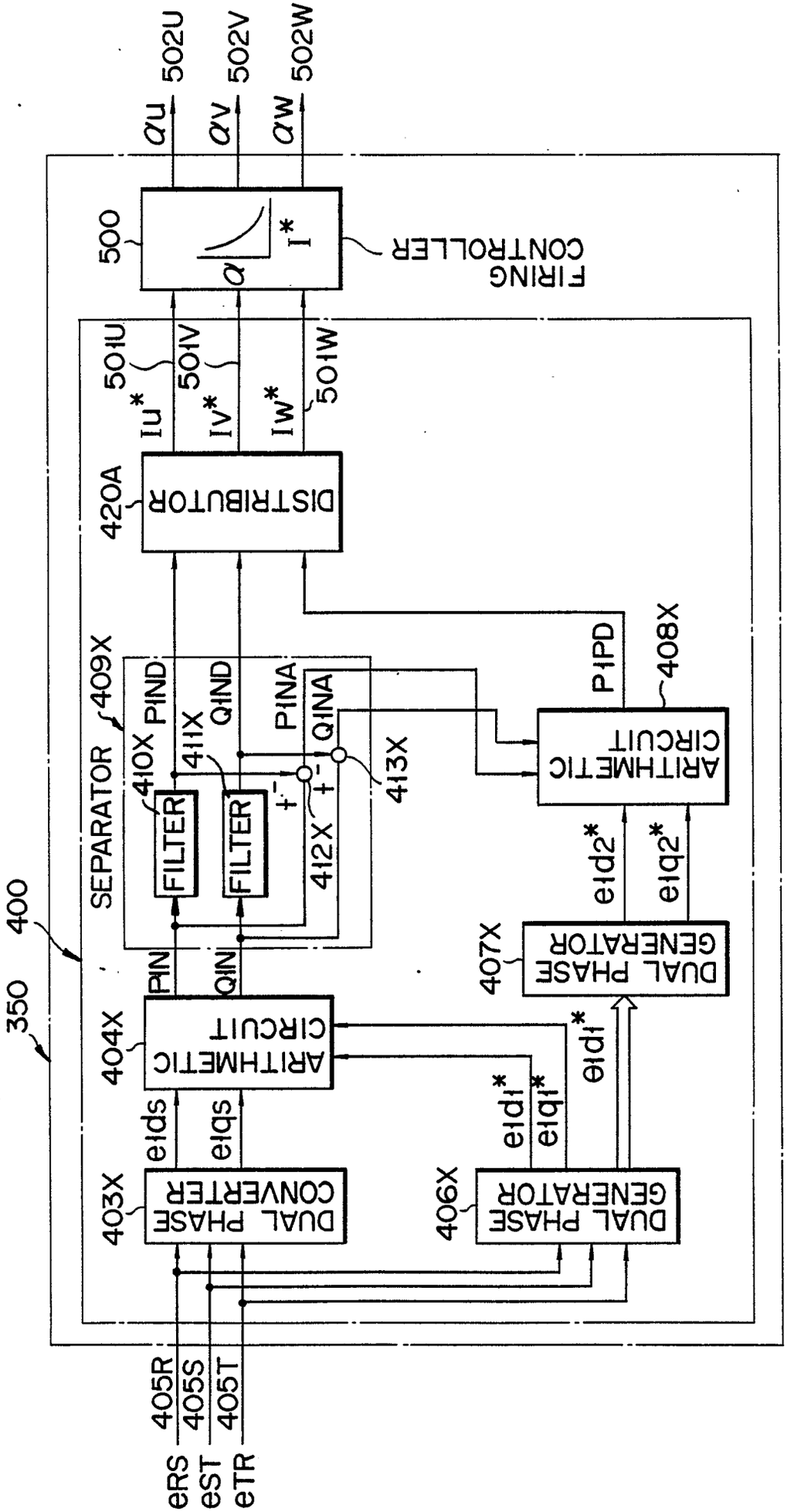
αU
αV
αW
502U
502V
502W
500
FIRING CONTROLLER
α
I*
501U
501V
501W
Iu*
Iv*
Iw*
420A
DISTRIBUTOR
409X
SEPARATOR
410X
411X
412X
413X
PIND
QIND
PINA
QINA
FILTER
FILTER
+
-
+
-
P1PD
408X
ARITHMETIC CIRCUIT
e1d2*
e1q2*
407X
DUAL PHASE GENERATOR
400
350
PIN
QIN
404X
ARITHMETIC CIRCUIT
e1di*
e1di*
e1qi*
e1ds
e1qs
403X
DUAL PHASE CONVERTER
406X
DUAL PHASE GENERATOR
405R
405S
405T
eRS
eST
eTR

FIG. 7