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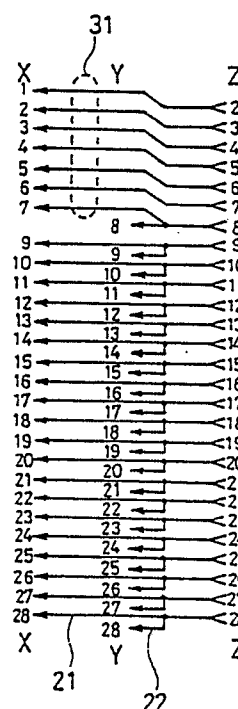
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54 **Coupling-type connector.**

57 In a coupling-type connector having three multiple contact connection plugs (6, 10, 16) on different sides (2, 7, 13) of the connector housing the interconnection of the three groups of contact elements (3, 8, 14) is provided such that a first group (31) of conductors connects the first k contact elements (X1 to X7) of the first plug (6) to the contact elements (Z2 to Z9) of the opposite plug (10) which are offset by one step with respect to the contact elements of the first plug. A second group of conductors connects the remaining contact elements (X9 to X28) of the first plug to the corresponding contact elements (Z9 to Z28) of the second plug.

FIG. 3



Coupling-Type Connector

The invention relates to an electrical connector of the type as described in the general portion of claim 1 as it is known from Figure 4 of US-A 44 77 862. Such connectors are used for mounting and mutually connecting units of various types of electronic devices on a panel or the like when those units are to be mounted on such panel. In those prior coupling-type connectors the respective contact elements of the same order provided at the first, second and third connection plugs are connected to each other. If a controller and a plurality of peripheral units are interconnected together by means of a common bus, respective lines constituting the bus must be sequentially shifted by the controller for a predetermined number of steps in a predetermined direction in accordance with the order of the peripheral units. It is the object of the invention to improve and to facilitate the establishing of a common bus for interconnecting several peripheral units and a controller which together form a data processing system. More specifically the invention looks for a coupling-type connector which facilitates the addition of further peripheral units and their connection to the common bus.

These and other objects are achieved by the invention as characterized in claim 1. Improvements thereof and particular embodiments of their structure and use in a communication system are described in the dependent claims.

The invention will now be described with reference to the accompanying drawings in which

Figure 1 shows the external shape of the connector;

Figure 2 is an enlarged sectional view taking along line X-Z of Figure 1;

Figure 3 shows the internal wiring of the contact elements of the three connecting plugs;

Figure 4 shows several connectors fixed to a common panel;

Figure 5 shows the resulting wiring diagram of the group of connectors shown in Figure 4;

Figure 6 is the block diagram of a bus system constituted by connectors according to the invention; and

Figure 7 is a flow chart describing the package state checking operation in a data processing system by means of a bus system according to Figure 6.

Figure 1 shows different views on a coupling-type connector in which Figure 1A is a top view, Figure 1B is a side view when looking from the right side onto Figure 1A and Figure 1C is another side view when looking from the bottom side onto Figure 1A. A first connection plug 6 having a projection 5 is provided at one side 2 of a main body

1. A plurality of jack-like contact elements 3 are arranged within projection 5 and through holes 4 aligned with contact element 3 are provided in the end portion of projection 5. A recess 9 is formed on the other side 7 of main body 1 opposite side 2. A plurality of pin-like contact elements 8 is arranged to project into recess 9, thus forming a second connection plug 10. The shape of projection 5 fits into recess 9 of plug 10 so that recess 9 of a first connector can be engaged with projection 5 of a second connector.

A plurality of pin-like contact elements 14 are arranged on an upper surface 13 of main body 1 that intersects with the one and the other sides 2 and 7 to project therefrom in a similar manner as second connection plug 10. In the shown embodiment the angle of intersection is 90°, but it could be different from 90° as well. A wall 15 surrounds the contact elements 14, therewith forming a third connection plug 16. A resilient projecting element 18 is formed to project from a lower surface 17 of main body 1 in order to fix the connector to a panel or the like.

Figure 2 is an enlarged sectional view taken along line X-Z of Figure 1. Conductors 21 are provided for connecting contact elements 3 and 8, and separate conductors 22 connect contact elements 3 and 14. At least the carrier portions for contact elements 3, 8 and 14 and for the conductors 21 and 22 and the projections 5 and 15 are made of an electrically insulating material.

Figure 3 is an internal wiring diagram showing the connections between the groups of contact elements. Reference symbol X indicates the contact elements 8 at the left side 7 symbol Y is associated with the contact elements 14 at the top side 13 and symbol Z is assigned to the contact elements 3 at the right side 2 of connector 1. A first group 31 of conductors connects contact elements X1-X7 to contact elements Z2-Z8 and constitutes an address bus. A third group 21 of conductors connecting contact elements X9-X28 to contact elements Z9-Z28 constitutes a data bus. Among contact elements X9-X28 and contact elements Y9-Y28 those of the same order corresponding to each other are connected via conductors 21 and 22 to contact elements Z9-Z28. In contrast to this regarding conductors 31, contact elements X1-X7 are regarded as the reference side, and their connections to contact elements Z are shifted by one or another predetermined number "j" in a predetermined direction from a low to a high order and are connected to contact elements Z2-Z8 via a conductor group 31 consisting of conductors of the type of conductor 21 (see Figure 2). Contact ele-

ments Y8 and Z8 of the last order in the predetermined direction are interconnected by means of conductor 22. Figure 3 shows one first group 31 of conductors, but if required, there could be more than one group with shifted interconnection. In the same manner there can be one or more third groups 21 interconnecting contact elements X and Z of the same order. A second group 22 of conductors connects contact elements Y9-Y28 to contact elements X9-X28 and Z9-Z28, respectively.

Figure 4 shows several connectors of the type as described with reference to Figures 1 and 2 now mounted on a flat panel 41 with Figure 4A and 4B showing front and side views, respectively. Connectors 42.1 to 42.n are fixed on a panel 41, and first connections plugs 6 of adjacent connectors 42.1 to 42.n are engaged with second connection plugs 10 of the same type. Regarding the left most connector 42.1, its connection plug 10 is connected to a control unit directly or via a connector cable. When units having appropriate connectors and comprising peripheral circuits are mounted to third connection plugs 16 of connectors 42.1 to 42.n, the third connection plugs 16 are commonly connected to the respective peripheral units and the control unit via corresponding buses because of the connections as shown in Fig. 3.

Connectors 42.1 to 42.n are fixed to the panel 41 by cutting out of panel 41 locking portions 43.1 to 43.n and 44.1 to 44.n and bending the end portions 45 of those locking portions to engage the upper and lower end walls of connectors 42.1 to 42.n. End portions 45 of the locking portions are bent such that they clamp connectors 42 to the panel 41. When connectors 42 are inserted between the locking portions 43 and 44 in a direction parallel to the surface of panel 41, they are urged against the end portions 45 of locking portions 43 by the elastic force of projecting elements 18 and are thus fixed to the panel.

In the address bus connection to a contact element Y8 of each of the connectors 42.1 to 42.n is shifted by one contact element as shown in Figure 3, and a circuit is obtained as shown in Figure 5. It shows the total interconnection provided by connectors 42.1 to 42.5. Connections of contact elements X1 to X7, to which the control unit of connector 42.1 is to be connected, are sequentially shifted one by one from a low to a high order in a predetermined direction to correspond to the contact elements Z2 to Z8 in accordance with the order of the connectors 42.1 to 42.5. Among these connections lines the line of the final order connected to contact element Z8 is connected to the contact element Y8 of a specific order of each of the connectors 42.1 to 42.5. Therefore, contact elements X7 to X3 of connector 42.1 are connected to only contact elements Y8 of

connectors 42.1 to 42.5, respectively. When further connectors 42.6 and 42.7 having similar arrangements are connected to the right side of connector 42.5, the contact elements X2 and X1 of connector 42.1 are connected only to contact elements Y8 of connectors 42.6 and 42.7, respectively.

As a result, when ID (Identification) request signals are sequentially transmitted from the control unit contact elements X1 to X7 of connector 42.1, these signals are sequentially supplied via contact elements Y8 of connectors 42.5 to 42.1 to the peripheral units mounted on connectors 42.5 to 42.1. When the peripheral circuit, having received the ID request signal, transmits ID corresponding codes via contact elements Y8 of the corresponding connectors, the control unit can perform package confirmation of the corresponding peripheral units by reception of these signals, and can designate a peripheral unit in a similar manner.

Figure 6 is a block diagram of a data processor constituted by the above connections. An address bus 51 consisting of contact elements X1 - X7 and Z2 - Z8 as shown in Figure 5, and a data bus 52 consisting of contact elements X9 - X28 and Z9 - Z28 are detachably connected to a control unit CNT 53 comprising a processor, a memory and other components, and to interface units I/Fs 54.1 to 54.n serving as the peripheral units via connectors 42.1 to 42.n as shown in Figure 4. Interfaces 54.1 to 54.n may comprise analog input circuits, analog output circuits, digital input circuits, digital output circuits, receivers connected to transmission lines, etc. in accordance with specific conditions and are packaged in a required number.

The processor CPU within control unit 53 executes the instruction of the memory and performs packaging state checking of the interfaces 54.1 to 54.n, data fetching through these interfaces, arithmetic operation and a determination based on data fetching, data transmission to the I/Fs 54.1 to 54.n in accordance with the result of the arithmetic operation and determination, and so on. The CPU also controls devices connected to the I/Fs 54.1 to 54.n and performs data transmission/reception with other devices via transmission lines.

Figure 7 is a flow chart showing the packaged state checking operation of the I/Fs 54.1 to 54.n using the CPU in CNT 53. In the "INITIALIZE" step 101, the respective portions are initialized and "SET UNIT PACKAGING CHECK MODE" step 102 is executed. Subsequently, a counter provided in the CPU in order to count the number of the I/Fs 54.1 to 54.n is set by "i = 1" in step 103. TRANSMIT ID REQUEST SIGNAL TO Xi" step 111 of the address bus is executed. When Y (YES) is obtained for "ID CODE RECEIVED?" in step 112 from corresponding I/Fi in response to this inquiry, "STORE I/Fi PACKAGE DATA IN MEMORY" step

121 is executed, and the count of the counter checks "i = n?". If "i = n?" is N (NO), counting up is performed by the counter in accordance with "i = i + 1" in step 123, and the steps after step 111 are repeated. When Y is obtained in step 122, "RESET UNIT PACKAGING CHECK MODE" step 131 is executed.

In the above procedure when N is obtained in step 112, step 121 is not executed but the procedure immediately advances to step 122.

As a result, it can be discriminated from the content of the memory corresponding to step 121 without using an address number whether or not the I/Fs 54.1 to 54.n are packaged. Any one of the I/Fs 54.1 to 54.n can be designated by signal transmission via the contact elements X1 to X7. Setting of an address number at the time of packaging of the I/Fs 54.1 to 54.n can be omitted, and abnormal data processing based on erroneous address number setting is completely eliminated.

Connectors 42.1 to 42.n are used, thus the number of the units can be increased easily and arbitrarily, thus increasing expandability of the system.

The number of contact elements X1 - X7 and Z1 - Z8 used for the address bus 51 can be determined in accordance with specific conditions. The same effect can be obtained if the shift of mutual connection is more than one, i.e. $j > 1$. The specific order of the contact element Y8 can be determined in accordance with the number of the contact elements X1 - X7 to Z1 - Z8 and the number of shift of the mutual connection.

The connectors 42 can have any shape as far as they can be connected to each other, and their shape can be determined in accordance with the shape of the units or the printed circuit boards. The contact element 14 of the third connection plug 16 could be of a jack type. The shape of each contact element can be arbitrarily selected.

The means for fixing the connectors on a panel or the like, and the means 43 for locking the unit and the connectors can be selected and shaped in accordance with the situation, and the shape of each of the connection plugs 6, 10, and 16 can be selected to meet local requirements. In this manner, various modifications can be made. As apparent from the above description, an interconnection is provided for independently designating the respective peripheral unit without using a particular address number. The expandability of the system is increased, thus providing an apparent effect in packaging of data processing units of various types.

Claims

1. A coupling-type connector comprising
 - a) a first connection plug (6) provided at a first side (2) of said connector and having a plurality of contact elements (3);
 - b) a second connection plug (10), engageable with said first type of connection plug (6), having a plurality of contact elements (8) and provided at the opposite side (7) of said connector;
 - c) a third connection plug (16) provided on a surface (13) intersecting with said first and said opposite sides and having a plurality of contact elements (14);
 - d) groups (21, 22) of conductors for interconnecting contact elements of said first, second and third connection plugs;
characterized in that
 - e) at least one first group (31) of conductors connecting contact elements X1 to Xk of the second plug (10) to contact elements $z(1+j)$ to $z(k+j)$ of the first plug (6) with ($j > 0$);
 - f) at least one second group (22) of conductors connecting contact elements $z(k+j)$ to Zn, with ($n > k+2$), of the first plug (6) to contact elements $Y(k+j)$ to Yn of the third plug (16);
 - g) at least one third group (21) of conductors connecting contact elements $Z(k+j+1)$ of the first plug (6) to contact elements $Y(k+j+1)$ of the second plug (10).
2. A Connector according to claim 1, **characterized in that** $j = 1$.
3. A connector according to claim 1 or 2, **characterized in that** $k = 7$ and $n = 28$ (Fig. 3).
4. A communication system for data processing, wherein a controller (53) and a plurality of peripheral units (54.1 to 54.n) are detachably interconnected via a common bus (51, 52) by means of connectors (42) according to claim 1, 2 or 3, and whereat data transmission is performed between said controller and said peripheral units under the control of said controller,
characterized in that respective lines (X1 - Z2 to X7 - Z8) constituting said bus (51) are connected from said controller (53) to be sequentially shifted by a predetermined number (j) in a predetermined direction in accordance with the arranging order of said respective peripheral units (54.1 to 54.n), and a line (Z8 - Y8) of the last order in the predetermined direction for each peripheral unit is connected to a contact element of a specific order (8) of said connector.
5. A system according to claim 3, **characterized in that**
 - h) an address bus (51) comprises the first group (31) of conductors and
 - i) a data bus (52) comprises the third group (21) of conductors.

FIG. 1

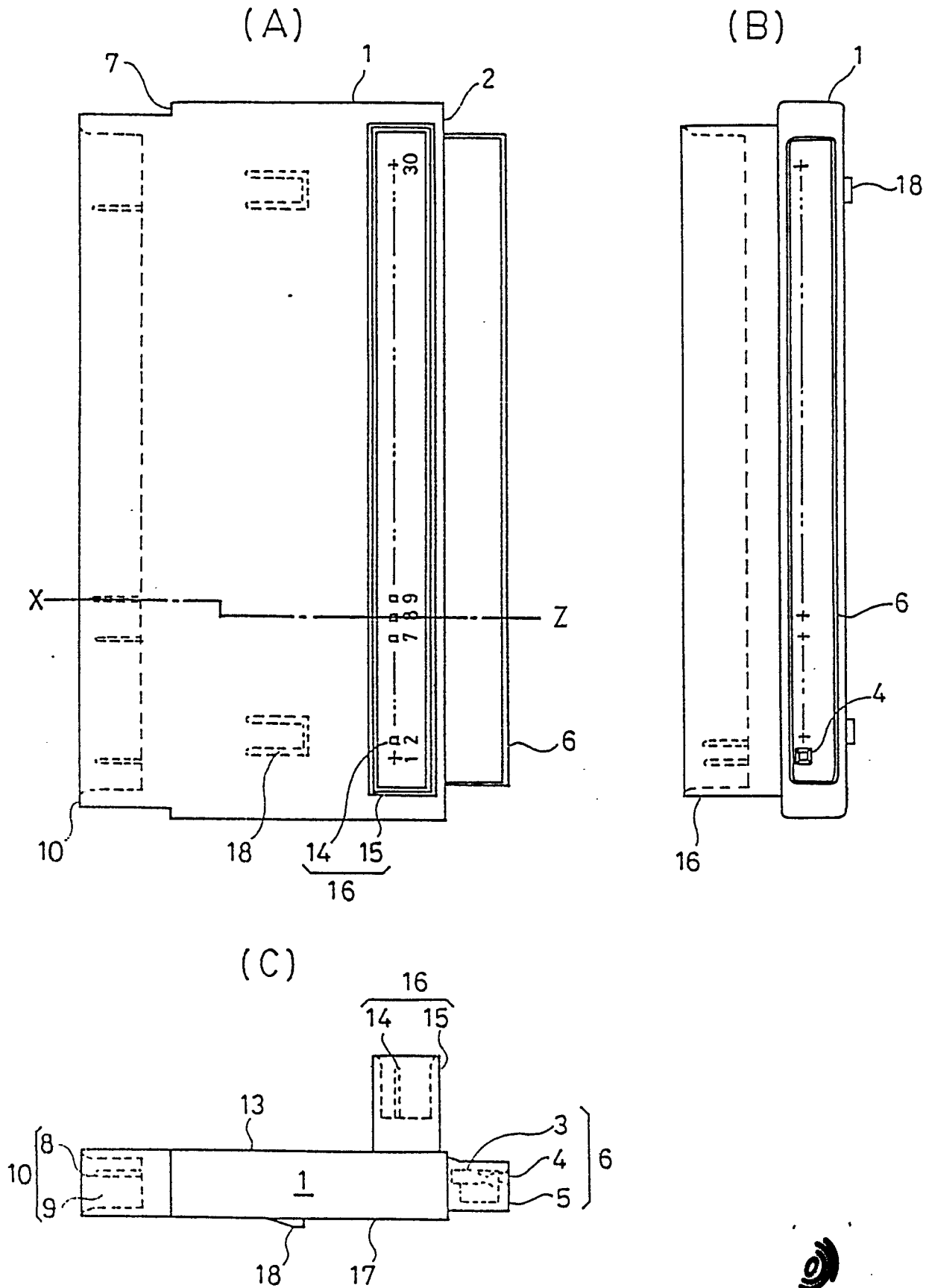


FIG. 2

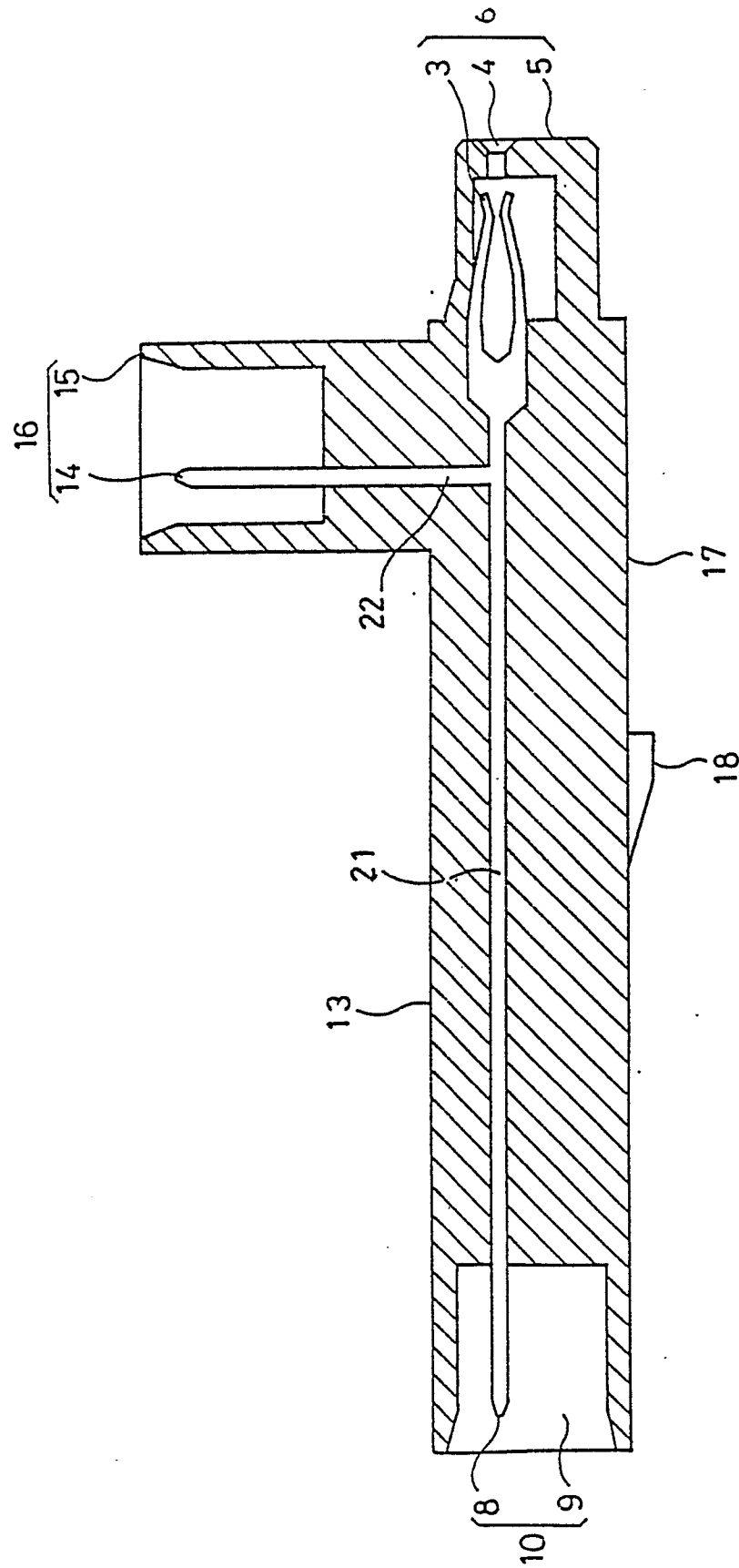
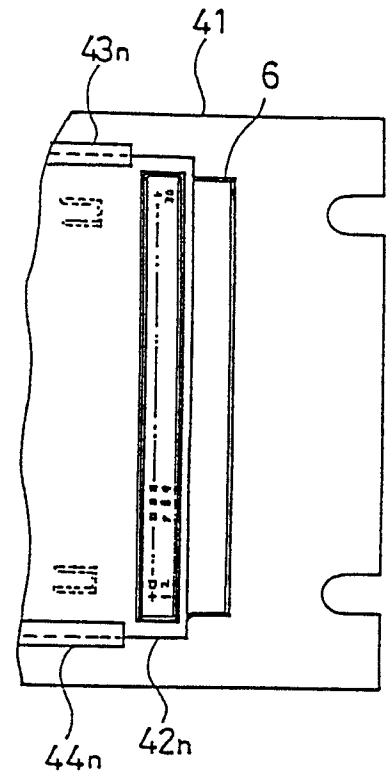
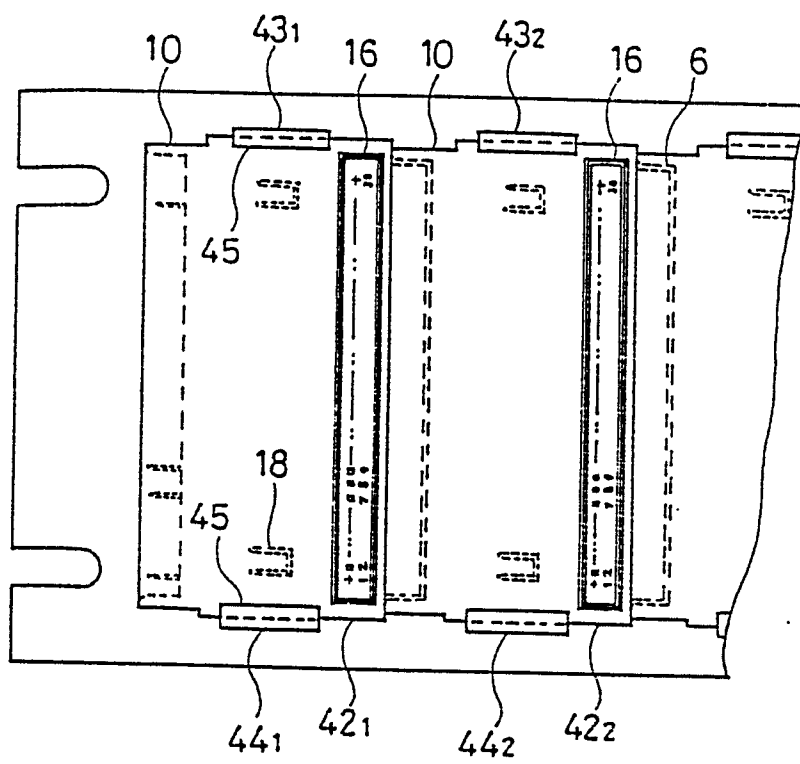


FIG. 4

(A)



(B)

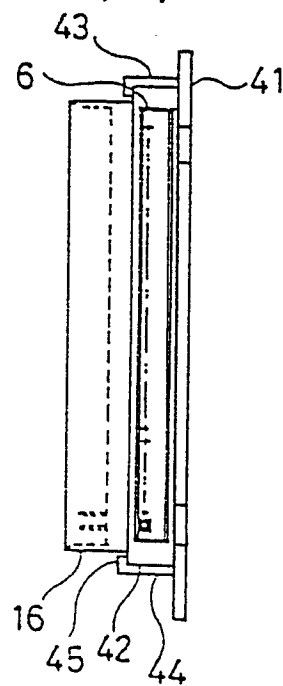


Figure 1 is a schematic diagram of a 28-bit parallel adder. It consists of four 8-bit adders, labeled 421, 422, 423, and 424, connected in series. Each adder takes an 8-bit input (X, Y, Z) and produces an 8-bit output (Y, Z). The output of one adder is the input for the next. The final output is a 28-bit result (X, Y, Z).

FIG. 6

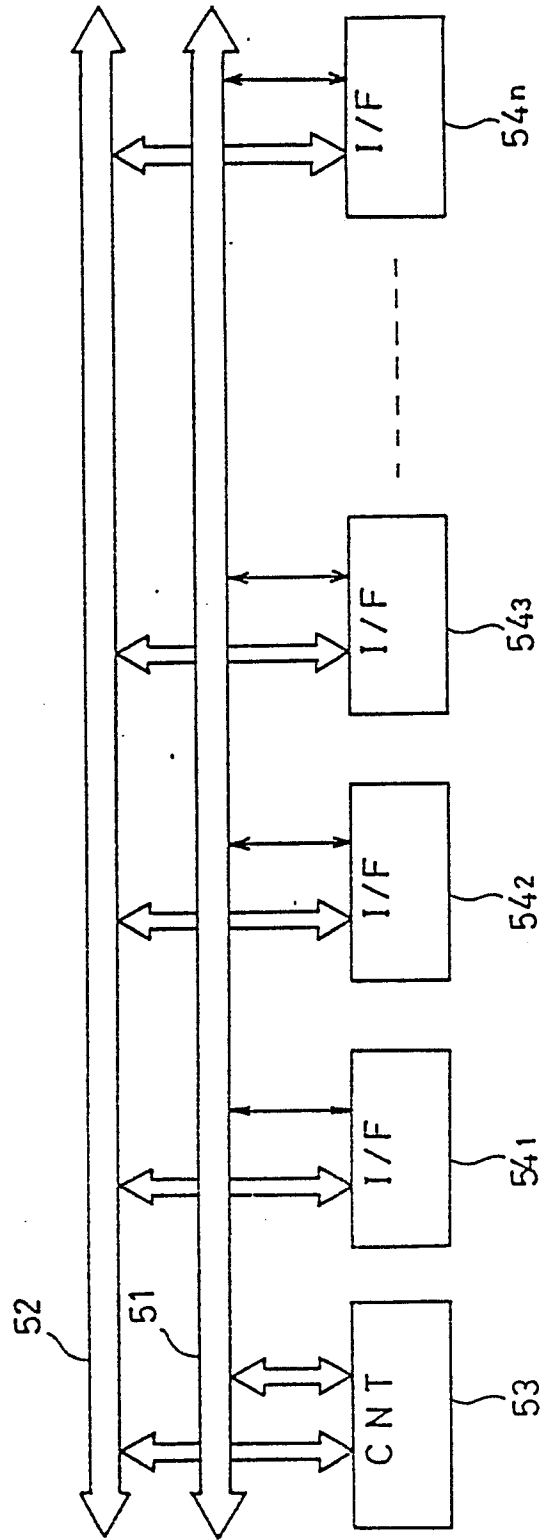


FIG. 7

