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Description

The present invention relates to a two-wire signal transmission system according to the preamble of claim 1.

In order to transmit outputs from a differential pressure transmitter, an electromagnetic flowmeter or the like representing measured values to a remote location according to conventional industrial measurement techniques, a unique signal having a current level within a range of 4-20 mA is used. Thus, an analog signal having a current level selected from this range represents a measured value. Such differential pressure transmitters, electromagnetic flowmeters and the like are normally arranged in a distributed manner to monitor industrial process states in a wide physical area. Maintenance personnel must travel extensively to maintain and inspect the distributed measuring instruments so as to perform adjustments and check the operating conditions thereof. In order to eliminate such time-consuming maintenance or the like, existing equipment is utilized to achieve remote control operation of the measuring instruments, as described in U.S. Patent No. US-A-4,520,488.

As shown therein, a transmitter is bridged to a two-wire transmission line to transmit a digital signal. After the digital signal is received by a receiver, the transmitter stops transmitting an analog measured value signal and responds to a digital signal from a communicator. The response signal is then received by the communicator. A similar mode of operation is achieved for digital signal communication between the communicator and the transmitter.

Since when the transmitter communicates with the communicator by means of the digital signal, the transmitter stops transmitting the analog signal, i.e., stops transmitting the measured value, if the measured value concurrently changes, the changed measured value cannot be immediately transmitted to the receiver. Therefore, the receiver cannot perform an immediate control operation according to the changed measured value. This impairs the ability of the state of equipment to be controlled to follow changes in the measured value.

It is, therefore, the object of the present invention to provide a transmission system capable of transmitting at least one measured value within a predetermined period determined in association with control operations so that an operating state of equipment to be controlled can always follow changes in measured value, even while the transmitter communicates with a communicator to exchange digital signals representing various types of data and with said transmission system being further capable of receiving only a measured value without adding an address code or the like repre-

senting a destination to each signal with signals other than the measured value being not acceptable.

This object is achieved according to the characterizing features of claim 1. Further advantageous embodiments of the system may be taken from the subclaims.

With respect to the figures of the attached drawings the transmission system according to the invention shall be further described, where

Fig. 1

is a block diagram showing an overall two-wire transmission system configuration,

Fig. 2

is a block diagram of a receiver for use in the system shown in Fig. 1 according to a first embodiment of the present invention,

Fig. 3

is a timing chart of a waveform showing changes in current for the two-wire transmission system,

Fig. 4

is a block diagram of a communicator used in the system shown in Fig. 1,

Fig. 5

is a circuit diagram of a current controller used in the system shown in Fig. 2,

Fig. 6

is a perspective pictorial view showing an outer physical appearance of the communicator shown in Fig. 5,

Fig. 7

is a block diagram of a transmitter used in the system shown in Fig. 1,

Figs. 7(A) and 7(B)

are flow charts for explaining the communicating and transmitting control operations,

Figs. 8(A) and 8(B)

are flow charts for explaining the reception control operations, and

Figs. 9(A) to 9(C)

are timing charts for explaining a second embodiment of the present invention.

Fig. 1 is a block diagram showing an overall two-wire transmission system configuration utilizing the present invention. A direct current (DC) power source (referred to as a PS hereinafter) 2 is connected to one end of a two-wire transmission line (referred to as a transmission line) 1 consisting of signal lines I_1 and I_2 to supply a current thereto. A transmitter (referred to as a TX hereinafter) 3 such as a pressure difference transmitter and an electromagnetic flowmeter is connected to the other end of the transmission line. The TX3 controls a current I in the transmission line 1 to generate signal pulses. The signal pulses are sent as a digital signal representing a measured process variable value onto the transmission line 1.

A resistor RL as a voltage dropping element is inserted in series with the transmission line I. A voltage across the resistor RL is supplied to a receiver (referred to as an RX hereinafter) 4 whereby the RX 4 receives the transmitted signal. An output signal from the RX 4 is sent to a main controller (referred to as an MC hereinafter) 6 such as a computer through a bus 5. Control operations by the MC 6 are performed on the basis of the measured value represented by the digital output signal supplied from the RX 4. Control data is sent to controlled equipment (not shown) through the bus 5, thereby controlling the equipment.

An operation unit (referred to as an OP hereinafter) 7, which can include a CRT display and a keyboard, is connected to a bus 5' through an interface (referred to as an I/F hereinafter) 9, for displaying a controlled state of the equipment and inputting a command to the MC 6 and the RX 4. A portable communicator (referred to as a CT hereinafter) 8 is bridged in the transmission line nearer to the TX 3 than the resistor RL. The CT 8 converts the current I into signal pulses and sends them as a digital command signal to the TX 3. The TX 3 receives the command signal and converts the current I into signal pulses as a response signal which is sent to the CT 8 in response to the command signal.

Fig. 3 shows a waveform of changes in current I supplied through the resistor RL as a function of time "t". In this case, the digital signal is a pulse code, the current of which changes in the range of I_1 to I_2 , e.g., 4-20 mA. A measured process value word WPV determined by the measured value from the TX 3 comprises 4-byte data consisting of bytes BY0 to BY3 (each byte consists of eight bits). If the length of time for each of the bytes BY0 to BY3 is "t1", e.g., 50 msec, the length of time of the measured value word WPV is "4t1", and the disable period following the word WPV is "t1". The measured value word WPV is repeatedly transmitted by changes in current "It" supplied across the lines of the TX 3, thereby always transmitting the newest measured value to the RX 4.

In this state, a command signal REQ as a pulse code is transmitted within a reception wait period "t2" shorter than the disable period "t1" by changing of a current I_c supplied from the CT 8 to line terminals T1 and T2 at the end of transmission of the measured value word WPV. The change in current causes a change in voltage across the resistor RL. The change in voltage across the resistor RL is sent as a change in voltage between the signal lines I_1 and I_2 to the TX 3. Therefore, the command signal REQ is received by the TX 3.

The TX 3 stops transmitting the measured value word WPV in response to the command signal REQ and sends back a 2-byte response word WRE

corresponding to the command signal REQ by means of the current I_t . In this case, the TX 3 transmits at least one measured value word within a predetermined period t1 which is determined in accordance with the system's control and safety requirements. If the response word WRE is long, it is divided into WRE1, WRE2, WRE3, ... which are then sequentially time-divisionally sent. Referring to Fig. 3, the period t2 shorter than the predetermined period t1 is monitored. If the short period t2 exceeds the predetermined period t1, the response word WPV is partially sent to assure the system control and safety measures, and the remaining portion of the response word WPV is then sent. After transmission of the response word WPV, the period t2 is monitored. If the period t2 exceeds the period t1, the response word WPV is transmitted. The relationship between the periods t1 and t2 is determined to transmit one WPV within t1. Thus, the voltage between the lines I_1 and I_2 is changed, and this change is received by the CT 8.

A start bit B0 of bits B0 to B31 in the start byte BY0 in the measured word WPV represents status ST indicating whether the TX 3 is normally operated. The bit B1 represents a proportional relationship L, i.e., a linear relationship between the measured value and the control value according to sensor characteristics, or a squared proportional relationship S, i.e., a relationship representing that the measured value is a square of the control value. The bit B2 represents the number NB of continuous bytes, i.e., that the number of continuous bytes is four or six. The bits B4 to B7 represent the type DA of the measured value transmitted by the bytes BY1 to BY3. In the bytes after byte BY0, the bytes BY1 to BY3 represent a measured value DPV. When the measured value is sent together with the response signal in the form of WPV + WRE, the response word WRE is transmitted continuously after the measured value word WPV. The number of bytes of each word and the number of bits of each byte can be determined according to the control states. The periods "t1" to "t3" are also properly determined according to the bit rate.

Fig. 4 is a block diagram of the CT 8. A digital processor (referred to as a CPU hereinafter) 11 such as a microprocessor is used in the CT 8. The CPU 11 is connected to a permanent memory (referred to as a ROM hereinafter) 12, a program-mable memory (referred to as a RAM hereinafter) 13, a keyboard (referred to as a KB hereinafter) 14, a display (referred to as a DP) 15 such as a numerical display, a universal asynchronous reception and transmission unit (referred to as an UART hereinafter) 16 and an interface unit (referred to as an I/F hereinafter) 17. The above components are connected to each other through a bus 18. A program stored in the ROM 12 is used under the

control of the CPU 11, and a control operation is performed while predetermined data is accessed to the RAM 13.

If desired input data is supplied at the KB 14, the CPU 11 controls the UART 16 and sends a gate pulse "Pcgl" as an "H" (high level) signal to the I/F 17. The AND gate 19 is turned on to gate the "H" pulse from the UART 16 to a current controller (referred to as a CC hereinafter) 20. Therefore, a current I_c is supplied from the terminal T1 to the terminal T2.

A voltage between the lines I_1 and I_2 is supplied to a filter (referred to as an FL hereinafter) 21 for filtering only a frequency component of the digital signal. The filtered signal is then supplied to one input terminal of a comparator (referred to as a CP hereinafter) 22. The filtered signal is compared by the CP 22 with a reference voltage E_{cs} supplied to the other input terminal thereof. The CP 22 extracts as an output a level exceeding the reference voltage E_{cs} .

For this reason, after the transmission of the command signal REQ, a gate pulse "Pcg2" is sent out as an "H" pulse from the I/F 17 when the output representing the start bit B0 of the measured value word WPV is supplied through the I/F 17. The AND gate 23 is turned ON, and then the output representing the bit B1 and the subsequent bits is sent to the UART 16. The resulting data is displayed on the DP 15 in response to this output. Even if the TX 3 repeatedly transmits the measured value word WPV, the reception is normally performed. Therefore, the measured value can be displayed on the DP 15.

Fig. 5 is a circuit diagram of the CC 20. A transmission pulse from the AND gate 19 through a noise reduction low-pass filter consisting of a resistor R1 and a capacitor C1 is amplified by a differential amplifier (referred to as an A hereinafter) 31 to turn on a transistor Q1 such as a field effect transistor. The current I_c is supplied through resistors R2 and R3. A voltage across the resistor R3 is negatively fed back to the A 31 through a resistor R4 so that the current I_c is maintained at a predetermined value.

Fig. 6 is a perspective pictorial view showing the outer physical appearance of the CT 8. The DP 15 and the KB 14 are arranged on a portable case 41. At the same time, a cord 42 extends outside the case 41. Clips 43 are line terminals T1 and T2 connected at the distal end of the cord 42. Therefore, the CT 8 can be detachably connected to transmission lines I_1 and I_2 .

Fig. 7 is a block diagram of the TX 3. In the same manner as in Fig. 4, a CPU 51 is connected to a ROM 52, a RAM 53, a UART 54, and an I/F 55 through a bus 56. The CPU 51 performs the control operation in the same manner as in Fig. 4. In

addition, the TX 3 further includes a multiplexer (referred to as an MPX hereinafter) 59 for selecting a pressure sensor (referred to as a PSS hereinafter) 57 for detecting a pressure difference or the like, or a temperature sensor (referred to as a TSS) 58 for detecting a temperature of the PSS 57, and an analog-to-digital converter (referred to as an ADC hereinafter) 60 for converting an output from the MPX 59 into a digital signal.

A direct current power source circuit (referred to as a PSC hereinafter) 61 is connected to the terminal T1. In this case, a current of 4 mA from the line I_1 is received and stabilized as a local power source E_t . The source E_t is supplied to the respective components by electrical connection lines which have been omitted for the sake of clarity. The voltage between the transmission lines I_1 and I_2 is filtered through a FL 62 such as a band-pass filter for filtering only the frequency component of the digital signal therethrough. The filtered output is supplied to a CP 63 in the same manner as in Fig. 4. The filtered output is compared with a reference voltage E_{ts} and the CP 63 generates a reception output. The reception output is supplied to the UART 54 through an AND gate 64.

If the "H" gate pulse "Ptgl" is sent in the reception mode after the measured value word WPV is completely sent, the AND gate 64 is turned ON. During the ON state of the AND gate 64, the command signal REQ is sent. In response to the command signal REQ, the reception output from the CP 63 is sent to the UART 54 to receive the command signal REQ. Thereafter, the CC 65 is turned off, and repetitive transmission of the measured value word WPV is interrupted.

Upon reception of the command signal REQ and the lapse of the predetermined period t_3 , the CPU 51 sends the "H" gate pulse "Ptg2" through the I/F 55 and at the same time controls the UART 54. The transmission pulse is sent to the CC 65 through the AND gate 66. The current corresponding to the word WRE is supplied through the CC 65.

When transmission of the words WPV and WRE representing the measured value and the response signal as described with reference to Fig. 3 is completed, the CPU 51 repeats sending out the transmission pulse in response to the measured value word WPV, thereby repetitively sending the measured value. The arrangement of the CC 65 is the same as that in Fig. 5. The TX 3 includes a nonvolatile memory 52 such as an EAR-OM whereby required data is stored in the nonvolatile memory 52. Even if a power failure occurs, the data can be retained in the nonvolatile memory 52.

The CPU 51 controls the MPX 59 to alternately

fetch the outputs from the PS 57 and the TS 58 at every predetermined interval. The fetched data is stored in the RAM 53. The CPU 51 then performs conversion operations of the detection output from the PS 57 and encodes the measured value. The coded measured value is sent to the UART 54 so that the measured value word WPV is sent. However, depending on the contents of the command signal REQ, the detection output from the TS 58 is sent out in the same manner as described above, or the outputs from the PS 57 and the TS 58 are sent alternately or in a combination thereof.

Fig. 2 is a block diagram of the RX 4. The RX 4 comprises a CPU 71 similar to the CPU 11 of Fig. 4, a ROM 72, a RAM 73, and I/Fs 74 and 75. These components are connected to each other through a bus 76. The CPU 71 performs the same operation as that of the CPU 11 so as to achieve reception operation. Inputs IN1 to INn from a plurality of transmission lines are supplied to the I/F 74. Digital signals based on changes in currents of the inputs IN1 to INn are sequentially received, and the CPU 71 performs predetermined processing. The processed results are sent out to the MC 6 through the I/F 75. The CPU 71 stores various types of data in the RAM 73 according to instruction contents and performs processing in response to an instruction supplied from the MC 6 or the OP 7 through the I/F 75. Therefore, the CPU 71 performs processing of digital signals.

Figs. 7(A) and 7(B) are flow charts showing the operations of the CPUs for controlling the CT 8 and the TX 3, respectively. More specifically, Fig. 7(A) shows the control operation of the CPU 11 in the CT 8, and Fig. 7(B) shows the control operation of the CPU 51 in the TX 3. Referring to Fig. 7(A), the CPU 11 determines in step 101 whether a transmission request is present. If YES in step 101, the CPU 11 determines in step 102 whether WPV is received. If YES in step 102, a counter incorporated in the CPU 11 for defining the transmission timing is restarted to perform "Setting of Synchronous State with WPV". The CPU 11 determines whether the next WPV has been received. If YES in 111 according to the transmission timing on the basis of a frequency-divided output of the clock pulse by means of this counter, the command signal REQ is sent out in step 112. The program flow advances to "Exit" and other routines and then returns to step 101. The command signal REQ is transmitted as soon as the measured value word WPV is completely transmitted, as shown in Fig. 3.

Referring to Fig. 7(B), the CPU 51 performs "Timer Clear (t)" for clearing the timer for monitoring a predetermined period and for causing the timer to start counting in step 201. The CPU 51 then sends the measured value word WPV in step 202 and sets the reception mode in step 211. The

CPU 51 then determines in step 212 whether the reception wait period "t2" (Fig. 3) has elapsed after the end of step 201. If NO in step 212, the CPU 51 determines in step 222 whether the command signal REQ is received. If NO in step 222, the operations in step 212 and the subsequent steps are repeated. However, if YES in step 222 while NO in step 212, the program flow advances to step 231. The CPU 51 determines in step 231 whether the reception is completed. If YES in step 231, the CPU 51 performs "n = 1" in step 241. The CPU 51 then sends the response signal word WREn in step 242, as described with reference to Fig. 3. The CPU 51 performs "n = n + 1" in step 251. The CPU 51 determines in step 252 whether the response is completed. While NO in step 252, the CPU 51 determines in step 261 whether the timer time "t" exceeds "t2". If NO in step 261, the flow returns to step 242. However, if YES in step 261, the word WPV is sent in step 262 so as to completely send the word WPV within the predetermined period t1. After the word WPV is sent, the timer is cleared in step 271. The CPU 51 then monitors the period t2, and the flow returns to step 242. If YES in step 212 while NO in step 222, the program flow advances to step 232. If the CPU determines that the disable period t1 has elapsed, i.e., if YES in step 232, the operations in step 201 and the subsequent steps are repeated.

The start of reception of the command signal REQ is allowed for a short reception wait period "t2" after the end of transmission of the measured value word WPV. During this period, if the command signal REQ is received, the gate pulse "Ptgl" is continuously sent out until the reception is completed. However, if reception is not performed within the reception wait period "t2", the gate pulse "ptgl" is disabled after the lapse of the period "t2". The reception mode is cancelled to prevent an operation failure caused by reception of noise or the like.

The insertion of the disable period "t1" allows the RX 4 to detect the start of each word following the reception wait period "t2" upon detection of the disable period "t1". The number NB of bytes in Fig. 3 counted from this timing are fetched as significant bytes. Therefore, only the measured value word WPV can be accurately received.

An address code or the like for designating a destination need not be added to each word and each signal, and communication between the TX 3 and the RX 4 can be accurately performed while system disturbance is properly eliminated during measured value transmission between the TX 3 and the RX 4. At the same time, the RX 4 causes a simple means such as timer to selectively receive the measured value word WPV.

Figs. 8(A) and 8(B) are flow charts of the

control operations of the CPU 71. More specifically, Fig. 8(A) shows interrupt processing, and Fig. 8(B) shows normal processing. Referring to Fig. 8(A), interrupt processing is repeated for a predetermined period shorter than the predetermined period t_1 in Fig. 3. The CPU 71 determines in step 301 whether the reception of the signal is completed. If YES in step 301, the "t1" timer incorporated in the CPU 71 is started in step 302. The CPU 71 determines in step 311 whether the timer time has elapsed. If YES in step 311, a reception ready flag is set in memory in step 312.

Referring to Fig. 8(B), the CPU determines in step 401 whether the reception ready flag is set so as to correspond to step 312. If YES in step 401, the reception signal is received from the I/F 74. The CPU 71 then determines in step 402 whether BY0 reception (Fig. 3) is completed. If YES in step 402, the respective bits are read out from the RAM 73. The CPU 71 then decodes NB (i.e., the number of bytes represented by the bit B2 as a specific bit). The CPU 71 then fetches specific bytes BY1 to BYn in step 411. The byte BY1 and the subsequent bytes are sequentially stored in the RAM 73 for a designated predetermined period. The stored data is regarded as valid data. Other data is not fetched and is regarded as invalid data. In correspondence with step 312, the CPU 71 sets the reception ready flag in step 412. The reception signal is no longer received, and the program flow advances to "Exit". The operations in step 401 and the subsequent steps are repeated through other routines.

The lapse of the disable period "t1" of Fig. 3 or the nonsignalling state for the predetermined period t_3 is detected in steps 302 and 311. The program flow then advances to steps 403 and 411 so that bytes BY0 to BYn are regarded to be valid for the specific period. However, other bytes are regarded as invalid bytes. Only the measured value word WPV is accurately discriminated and received. The measured value word WPV is transferred to the MC 6 and is used for control operation, thereby preventing the reception control state from disturbance.

The transmission status of the command signal is defined by inequality " $t_1 < t_2$ ". The CPU 71 does not affirm step 311. In response to this decision, step 401 is determined to be NO. In this case, the independent measured value word WPV cannot be obtained and is naturally regarded as an invalid word. This control is not associated with the RX 4. However, if the number of bytes of the measured value word WPV is given in advance, step 403 may be omitted. The specific period given as an integer multiple of the byte period t_1 may be used, and a predetermined number of bytes may be fetched in step 411. Without adding

an address code or the like for designating a destination to each word and signal, a measured value can be transmitted from the TX 3 to the RX 4. The control state in the RX 3 is not disturbed. In the RX 4, a simple means such as a timer is used to selectively receive the measured value word WPV.

Figs. 9(A) to 9(C) are timing charts showing another embodiment of the present invention. Fig. 9(A) shows a case wherein a measured value word WPV and a response word WRE are sent together as 14-byte data within a time period "14t1". Fig. 9(B) shows a case wherein the measured value word WPV based on the newest measured value is transmitted twice after reception of the command signal REQ, and then the measured value word WPV and the response signal word WRE are sent as 14-byte data in the same manner as in Fig. 9(A).

If the measured value word TPV based on the newest measured value is always sent to the RX 4, it is suitable to allow the TX 4 to perform a control function. However, for allowable variations in measured values, the immediately preceding value may be repeatedly sent. If a variation exceeding the allowable range occurs, the newest measured value may be sent.

Referring to Fig. 9(C), the TX 3 interrupts transmission of the measured value word WPV in response to the command signal REQ. When a predetermined period " t_3 " has elapsed after the end of the command signal REQ, 4-byte measured value word WPV and 2-byte response word WRE in response to the command signal REQ are sent together by means of a current It. This transmission for a period "6t1" from a start word WRE(S) to an end word WRE(E) is repeatedly performed through the disable period "t1". The measured value word WPV is repeatedly sent again.

Transmission of data including the measured value word WPV guarantees transmission of the measured value while the RX 4 can always follow the changes in measured value and the response time of the control state is improved. The measured value word WPV and the response signal word WRE are sent together when the predetermined period t_3 has elapsed, thereby easily discriminating the measured value word WPV and preventing control disturbance in the RX 4.

The predetermined period " t_3 " can be defined not only by a timer but also by various time defining means. For example, a transmission timing definition pulse may be generated by frequency-dividing a clock pulse, and the timer time may be defined by a transmission timing pulse after reception of the control signal REQ.

In the above embodiment, the CPU 51 is used as a control means. However, the control means

may be a control circuit constituted by a combination of various logic circuits. Referring to Fig. 3., a parity check bit may be added to each byte or an identification code or the like of the TX 3 may be added. The period "t1" may be equal to the period t3 according to given conditions.

Claims

1. A two-wire signal transmission system comprising at least a transmitter (3) for repeatedly transmitting a measured value (WPV) through a two-wire transmission line (I_1, I_2) by a change in current supplied to said transmission line, at least a receiver (4) connected to said transmission line for receiving a signal from said transmitter, and a communicator (8) connectable to said two-wire transmission line for communicating with said transmitter, whereat said transmitter (3) comprises:
means for receiving (62-64) a digital command signal (REQ) from said communicator (8) through said two-wire transmission line, and control means (51-56,65,66) for sending out a response signal (WRE) onto said two-wire transmission line in response to said command signal upon reception thereof, and whereat said communicator (8) comprises:
means for receiving (21-23) said response signal from said transmitter (3) through said two-wire transmission line, and control means (11-17,19,20) for sending out said command signal onto said two-wire transmission line, **characterized in that**
said transmitter (3) not only transmits the response signal (WRE) but also the measured value (WPV) in the form of a digital signal and that said transmitter control means (51-56,65,66) serves to add the measured value (WPV) to said response signal (WRE) generated in response to said digital command signal (REQ) and for transmitting a resultant signal (WPV+WRE) onto said two-wire transmission line; and
said receiver (4) comprises:
time defining means (71-73) for discriminating that a non-signaling state of said transmission line has continued for a predetermined period of time and
further control means (71) for validating a specific period ($4t_1$) of a reception signal received after the discrimination operation of said time defining means in order to selectively receive said measured value (WPV) from said resultant signal (WPV+WRE).
2. A system according to claim 1, **characterized in that** the measured value (WPV) is sent

using a newest measured value after repetitive transmission of the measured value is interrupted.

3. A system according to claim 1, **characterized in that** the reception of the command signal is performed by a change in interline voltage of the two-wire transmission line.
4. A system according to claim 1, **characterized by** means (51-56, 64) for monitoring a predetermined period of time with said means comprising a timer (51).
5. A system according to claim 1, **characterized in that** said control means comprises a digital processor (51).
6. A system according to one of claims 1 to 5, **characterized in that** said control means is arranged (51-56, 65, 66) so as to transmit at least one measured value within a predetermined period.
7. A system according to one of claims 1 to 6, **characterized in that** the reception signal is a digital signal obtained by change in current supplied through said transmission line.
8. A system according to claim 7, **characterized in that** said time defining means comprises a timer (71-73).
9. A system according to claim 7, **characterized in that** said further control means comprises a digital processor (71).
10. A system according to claim 7, **characterized in that** the predetermined period is an integer multiple of the number of bytes to be transmitted or received, respectively.

Patentansprüche

1. Zweidraht-Signal-Übertragungssystem mit wenigstens einem Übertrager (3) zur wiederholten Übertragung eines Meßwertes (WPV) über eine Zweidraht-Übertragungsleitung (I_1, I_2) mittels einer auf die Übertragungsleitung gegebenen Stromänderung, mit wenigstens einem Empfänger (4), der an die Übertragungsleitung angeschlossen ist, um ein Signal von dem Übertrager zu empfangen, und einem Dialoggerät (8), das an die Zweidraht-Übertragungsleitung angeschlossen ist, um mit dem Übertrager einen Dialog zu führen, wobei der Übertrager (3) umfaßt:
Eine Einrichtung (62-64) für dem Empfang ei-

nes digitalen Befehlsignales (REQ) von dem Dialoggerät (8) über die Zweidraht-Übertragungsleitung, und

eine Steuereinrichtung (51-56,65,66) für das Aussenden eines Antwortsignales (WRE) auf der Zweidraht-Übertragungsleitung auf Grund des Befehlsignales bei dessen Empfang, und wobei das Dialoggerät (8) umfaßt:

Eine Einrichtung (21-23) für den Empfang des Antwortsignales von dem Übertrager (3) über die Zweidraht-Übertragungsleitung, und eine Steuereinrichtung (11-17,19,20) für das Aussenden des Befehlsignales auf der Zweidraht-Übertragungsleitung, **dadurch gekennzeichnet**, daß

der Übertrager (3) nicht nur das Antwortsignal (WRE), sondern auch den Meßwert (WPV) in Form eines Digitalsignals überträgt und daß die Übertrager-Steuereinrichtung (51-56,65,66) der Addition des Meßwertes (WPV) zu dem Antwortsignal (WRE) dient, das auf Grund des digitalen Befehlsignales (REQ) erzeugt wird und das resultierende Signal (WPV + WRE) auf der Zweidraht-Übertragungsleitung überträgt; und

daß der Empfänger (4) aufweist:

Eine zeitbestimmende Einrichtung (71-73) zur Feststellung, daß ein Nicht-Signal-Zustand auf der Übertragungsleitung während einer vorbestimmten Zeitperiode vorliegt, und eine weitere Steuereinrichtung (71) zur Überprüfung einer spezifischen Periode ($4t_1$) eines Empfangssignales nach der Feststelloperation der zeitbestimmenden Einrichtung, um selektiv den Meßwert (WPV) aus dem resultierenden Signal (WPV + WRE) zu empfangen.

2. System nach Anspruch 1, **dadurch gekennzeichnet**, daß der Meßwert (WPV) unter Verwendung des neuesten Meßwertes gesendet wird, nachdem eine wiederholte Übertragung des Meßwertes unterbrochen ist.

3. System nach Anspruch 1, **dadurch gekennzeichnet**, daß der Empfang des Befehlsignales durch Verändern der Spannung zwischen den Leitungen der Zweidraht-Übertragungsleitung erfolgt.

4. System nach Anspruch 1, **gekennzeichnet durch** eine Einrichtung (51-56,64) zur Überwachung einer vorbestimmten Zeitperiode, wobei die Einrichtung einen Zeitgeber (51) umfaßt.

5. System nach Anspruch 1, **dadurch gekennzeichnet**, daß die Steuereinrichtung einen digitalen Prozessor (51) umfaßt.

6. System nach einem der Ansprüche 1 bis 5, **dadurch gekennzeichnet**, daß die Steuereinrichtung (51)-56,65,66) so ausgebildet ist, daß sie wenigstens einen Meßwert innerhalb einer vorbestimmten Periode überträgt.

7. System nach einem der Ansprüche 1 bis 6, **dadurch gekennzeichnet**, daß das Empfangssignal ein digitales Signal ist, das durch Stromänderung auf der Übertragungsleitung erhalten wird.

8. System nach Anspruch 7, **dadurch gekennzeichnet**, daß die zeitbestimmende Einrichtung einen Zeitgeber (71-73) umfaßt.

9. System nach Anspruch 7, **dadurch gekennzeichnet**, daß die weitere Steuereinrichtung einen digitalen Prozessor (71) umfaßt.

10. System nach Anspruch 7, **dadurch gekennzeichnet**, daß die vorbestimmte Periode ein ganzzahliges Vielfaches der Anzahl von Bytes ist, die zu übertragen bzw. zu empfangen sind.

Revendications

1. Système de transmission de signal à deux fils comprenant au moins un émetteur (3) pour transmettre de manière répétée une valeur mesurée (WPV) au travers d'une ligne de transmission à deux fils (l_1 , l_2) au moyen d'une variation du courant appliqué à ladite ligne de transmission, au moins un récepteur (4) raccordé à ladite ligne de transmission pour recevoir un signal en provenance dudit émetteur et un communicateur (8) qui peut être raccordé à ladite ligne de transmission à deux fils pour communiquer avec ledit émetteur, dans lequel ledit émetteur (3) comprend :

des moyens (62-64) pour recevoir un signal de commande numérique (REQ) en provenance dudit communicateur (8) au travers de ladite ligne de transmission à deux fils, et

des moyens de commande (51-56, 65, 66) pour émettre un signal de réponse (WRE) sur ladite ligne de transmission à deux fils en réponse audit signal de commande suite à la réception de ce dernier,

dans lequel ledit communicateur (8) comprend :

des moyens (21-23) pour recevoir ledit signal de réponse en provenance dudit émetteur (3) au travers de ladite ligne de transmission à deux fils et des moyens de commande (11-17, 19, 20) pour émettre ledit signal de commande sur ladite ligne de transmission à deux fils, caractérisé en ce que

ledit émetteur (3) transmet non seulement le signal de réponse (WRE) mais également la valeur mesurée (WPV) sous la forme d'un signal numérique et en ce que lesdits moyens de commande d'émetteur (51-56, 65, 66) servent à ajouter la valeur mesurée (WPV) audit signal de réponse (WRE) généré en réponse audit signal de commande numérique (REQ) et à transmettre un signal résultant (WPV + WRE) sur ladite ligne de transmission à deux fils ; et ledit récepteur (4) comprend :

des moyens de définition temporelle (71-73) pour discriminer qu'un état de non-signalisation de ladite ligne de transmission se poursuit pendant une période temporelle prédéterminée ; et

un autre moyen de commande (71) pour valider une période spécifique ($4t_1$) d'un signal de réception reçu après l'opération de discrimination dudit moyen de définition temporelle afin de recevoir de manière sélective ladite valeur mesurée (WPV) à partir dudit signal résultant (WPV + WRE).

2. Système selon la revendication 1, caractérisé en ce que la valeur mesurée (WPV) est émise en utilisant une valeur mesurée la plus nouvelle après qu'une transmission répétitive de la valeur mesurée est interrompue. 25
3. Système selon la revendication 1, caractérisé en ce que la réception du signal de commande est effectuée au moyen d'une modification de la tension interligne de la ligne de transmission à deux fils. 30
4. Système selon la revendication 1, caractérisé par des moyens (51-56, 64) pour surveiller une période temporelle prédéterminée, lesdits moyens comprenant une minuterie (51). 35
5. Système selon la revendication 1, caractérisé en ce que lesdits moyens comprennent un processeur numérique (51). 40
6. système selon l'une quelconque des revendications 1 à 5, caractérisé en ce que lesdits moyens de commande (51-56, 65, 66) sont agencés de manière à transmettre au moins une valeur mesurée comprise dans une période prédéterminée. 45
7. Système selon l'une quelconque des revendications 1 à 6, caractérisé en ce que le signal de réception est un signal numérique obtenu en faisant varier le courant appliqué au travers de ladite ligne de transmission. 50
8. Système selon la revendication 7, caractérisé en ce que lesdits moyens de définition temporelle comprennent une minuterie (71-73). 55
9. Système selon la revendication 7, caractérisé en ce que ledit autre moyen de commande comprend un processeur numérique (71).
10. Système selon la revendication 7, caractérisé en ce que la période prédéterminée est un multiple entier du nombre de multiplets ou d'octets qui doivent être respectivement transmis ou reçus.

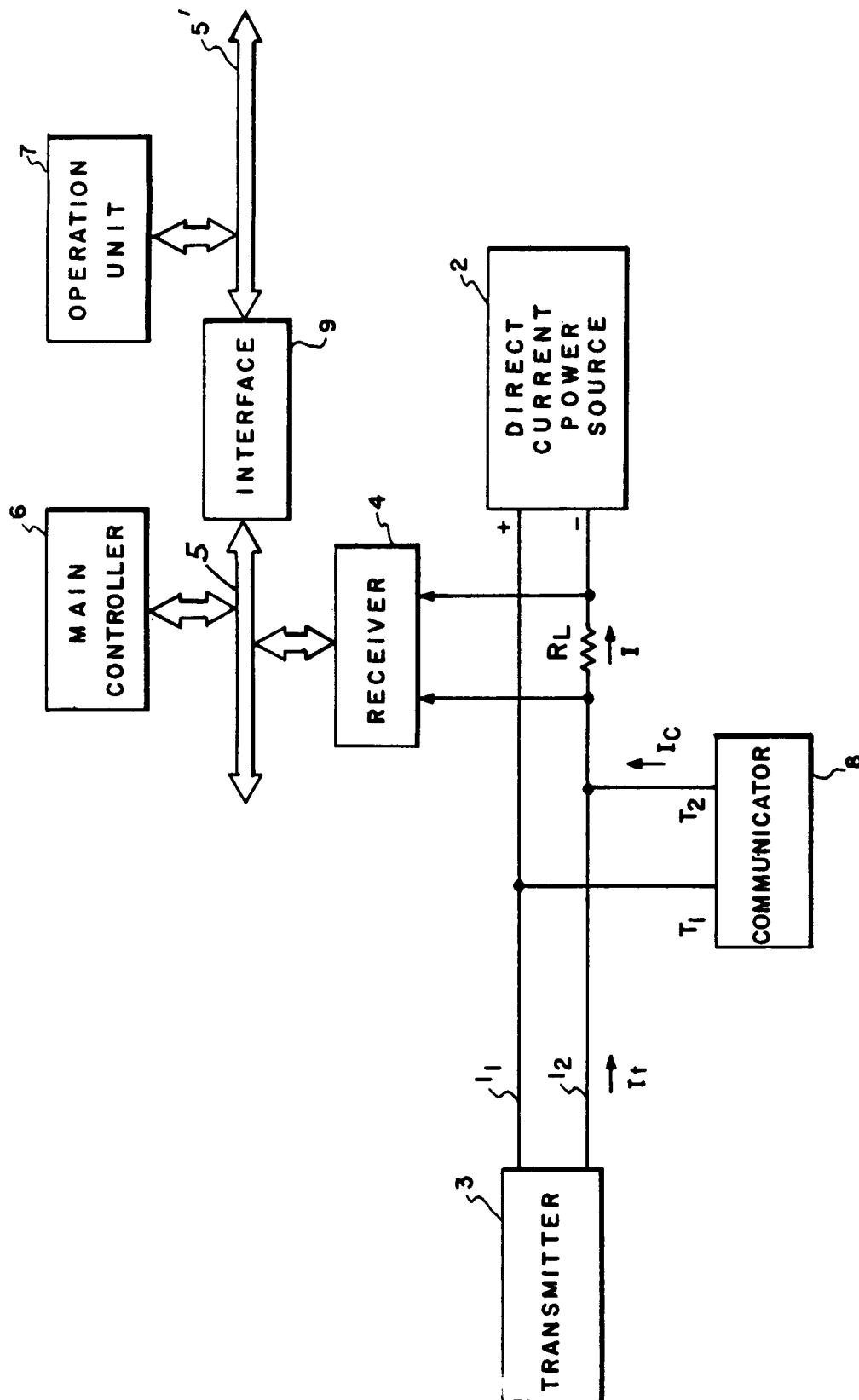


FIG. 1

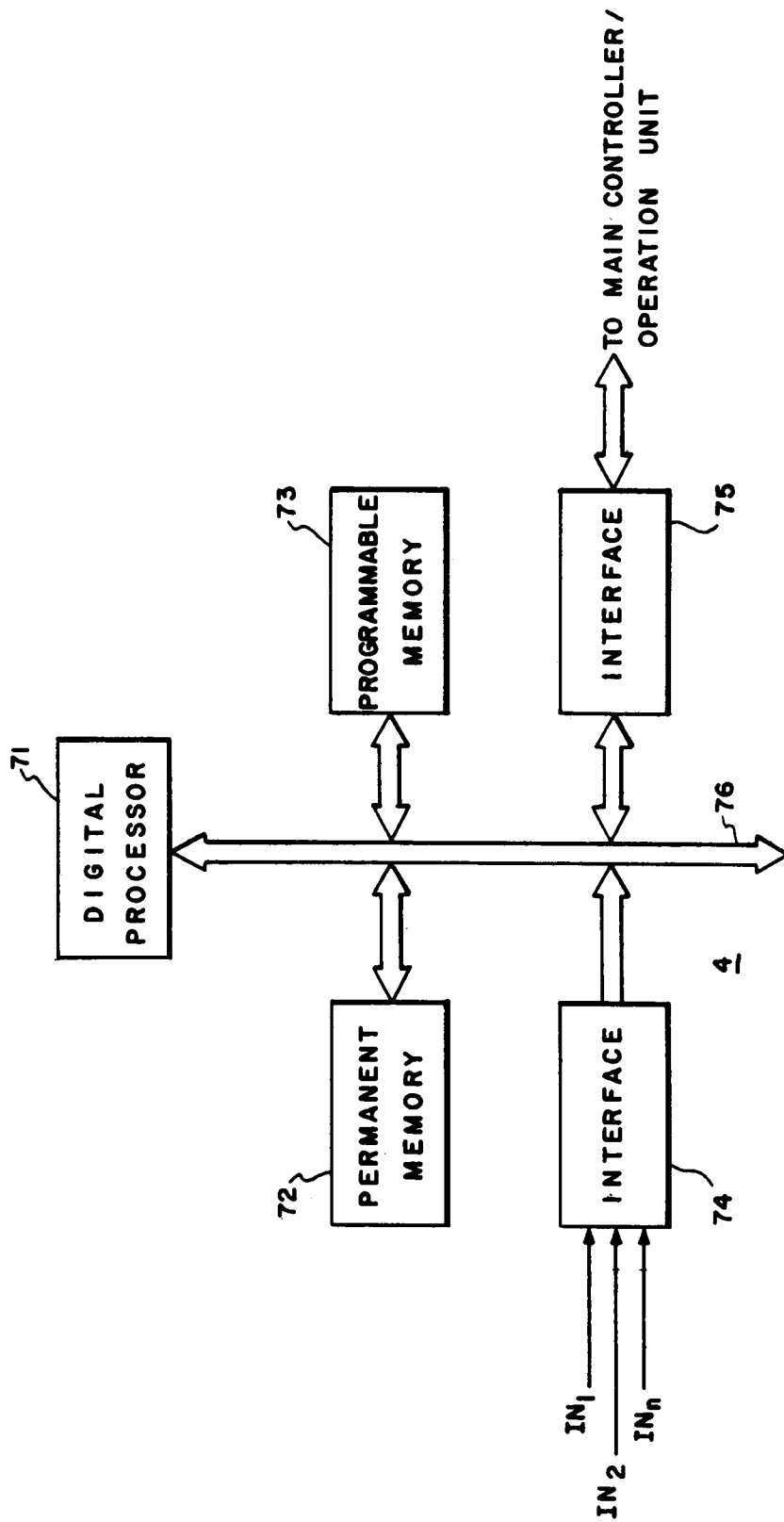
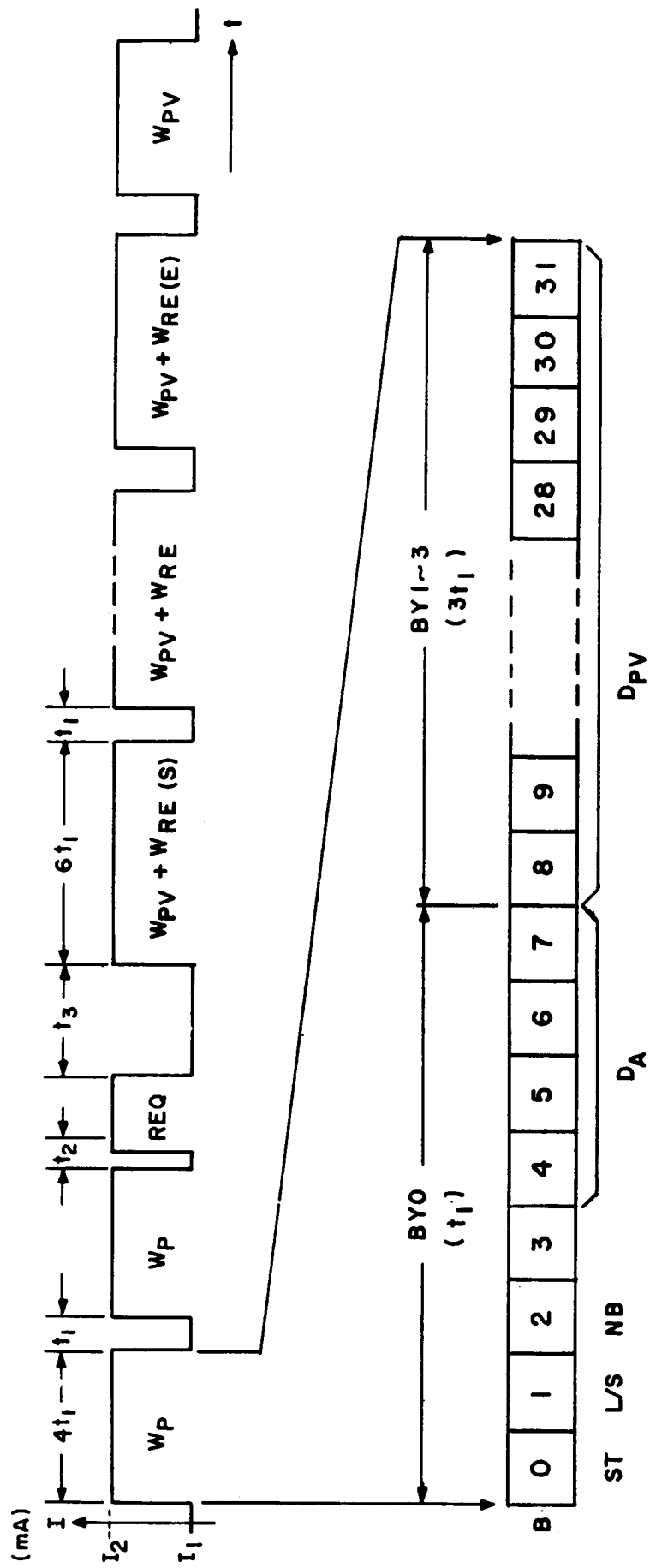


FIG. 2



F I G. 3

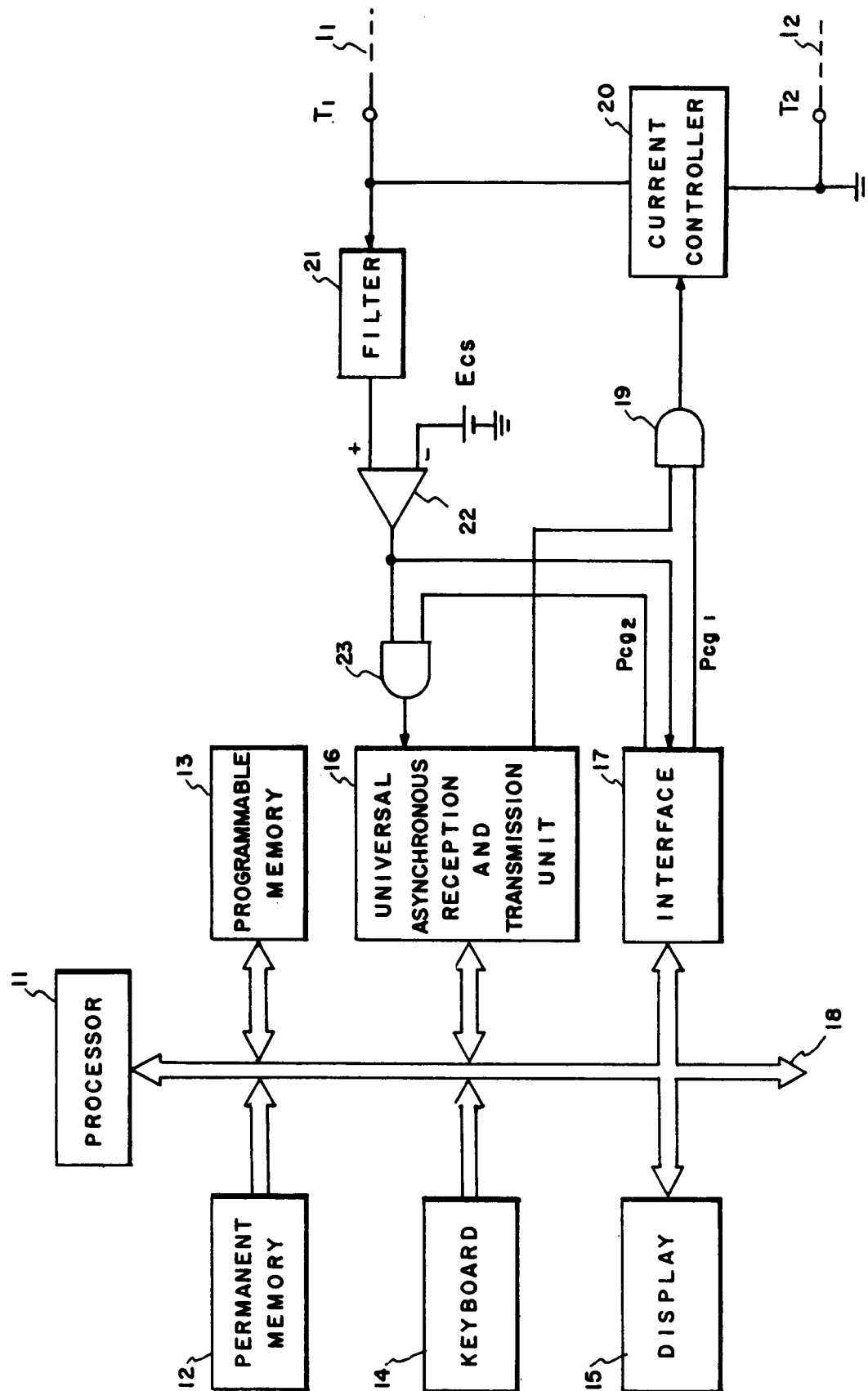


FIG. 4

FIG. 5

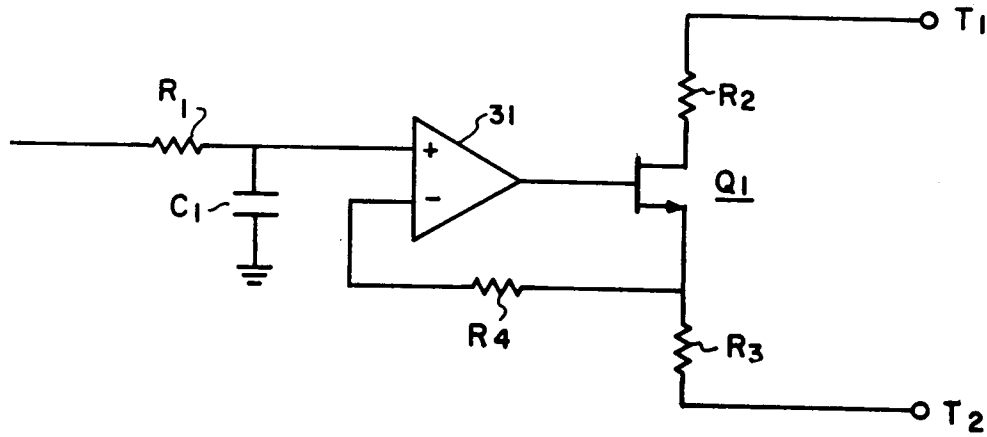
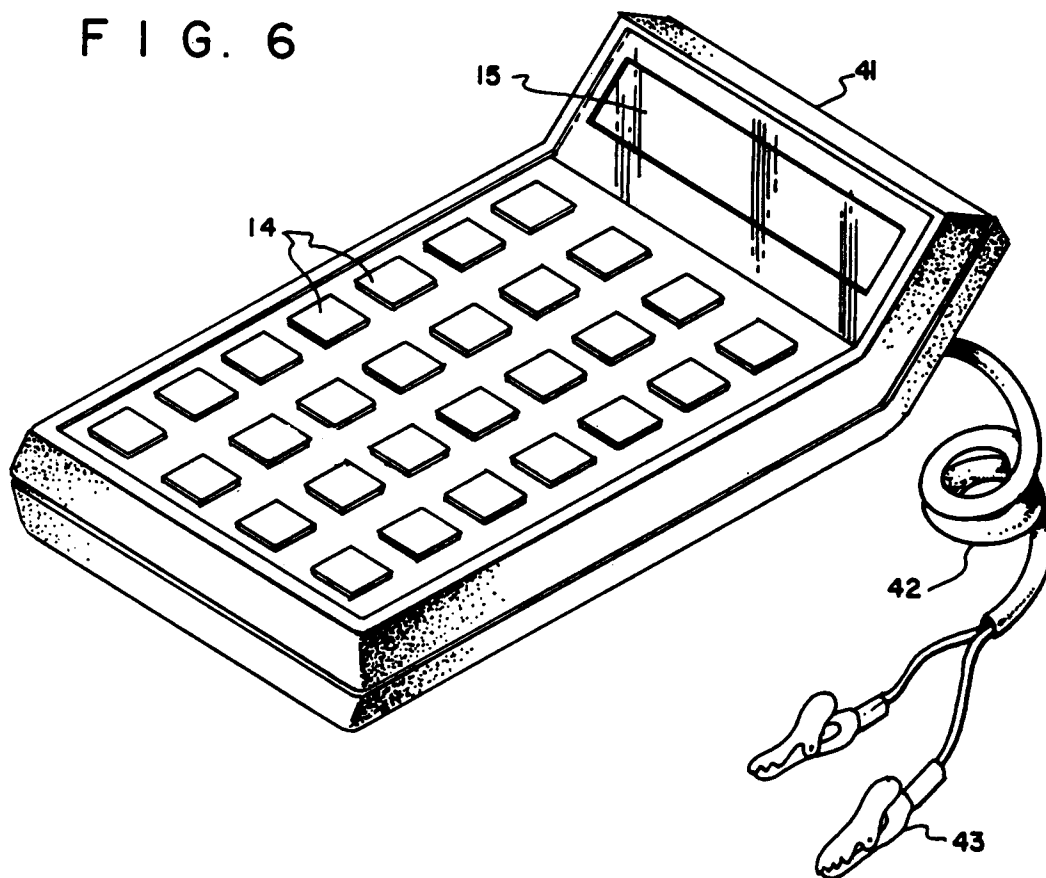


FIG. 6



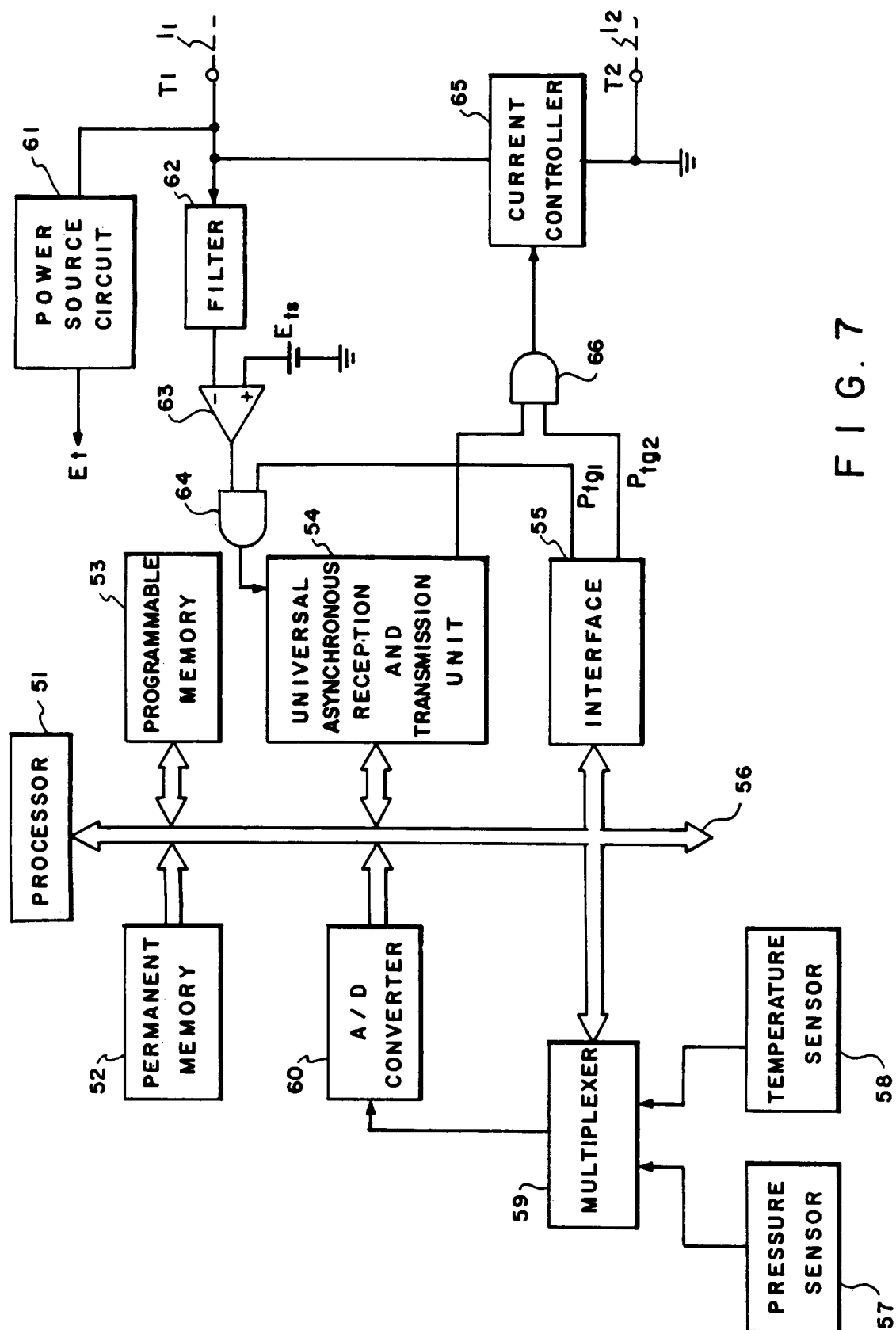


FIG. 7

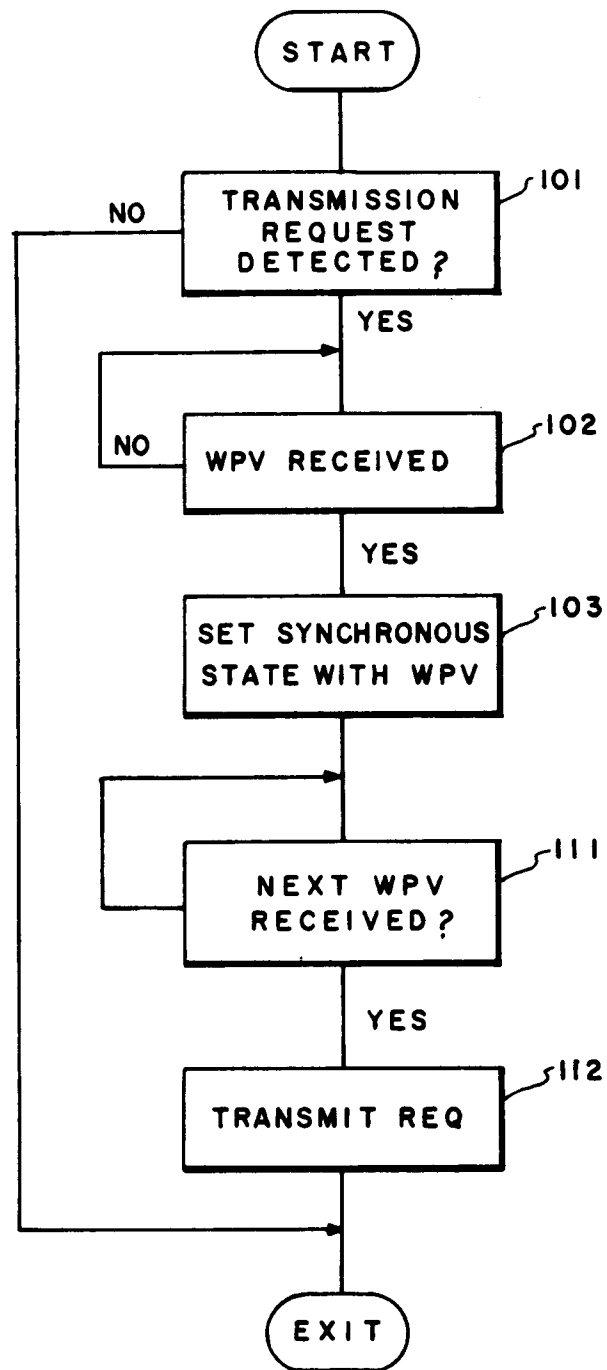


FIG. 7(A)

FIG. 7(B)

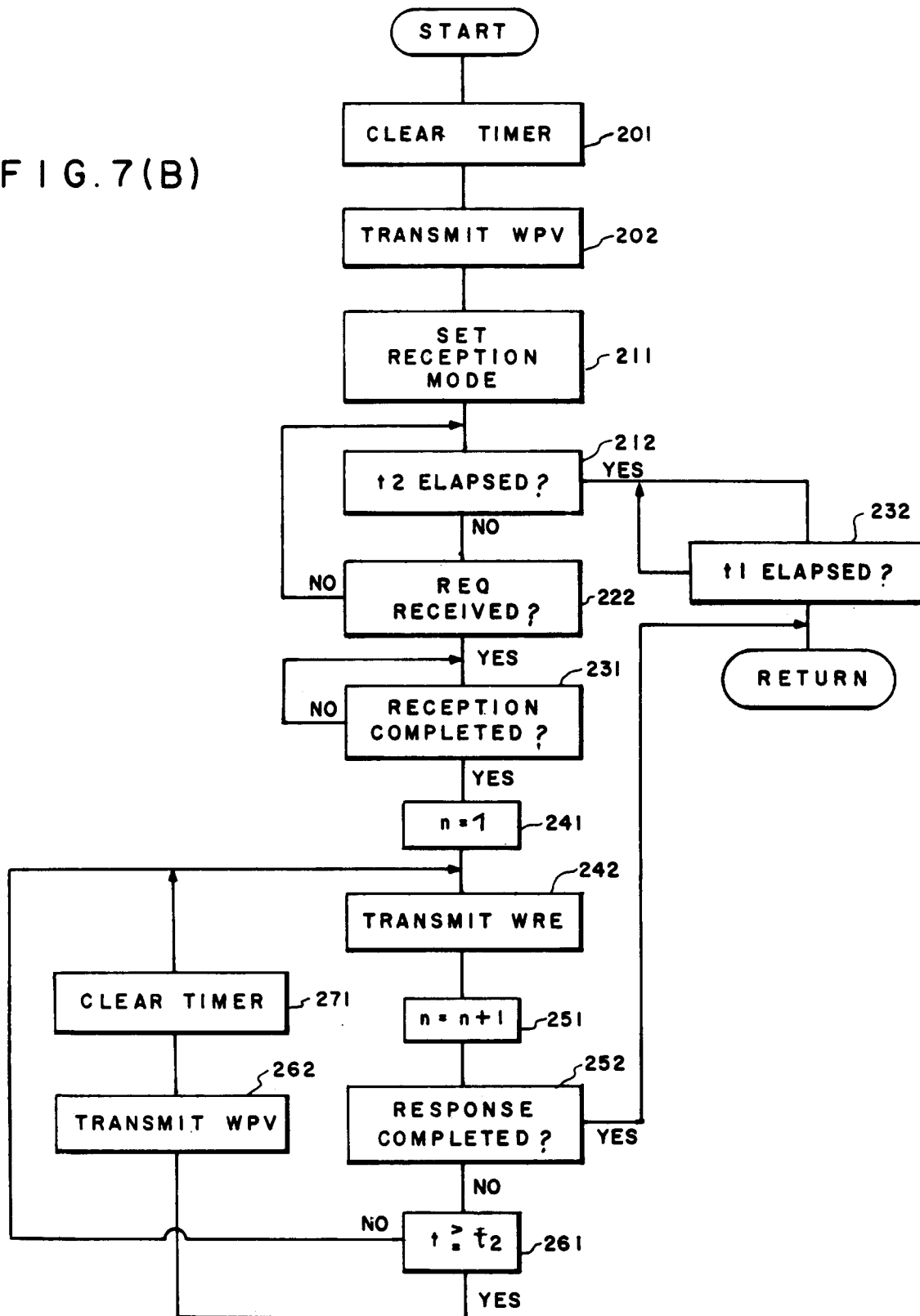


FIG. 8(A)

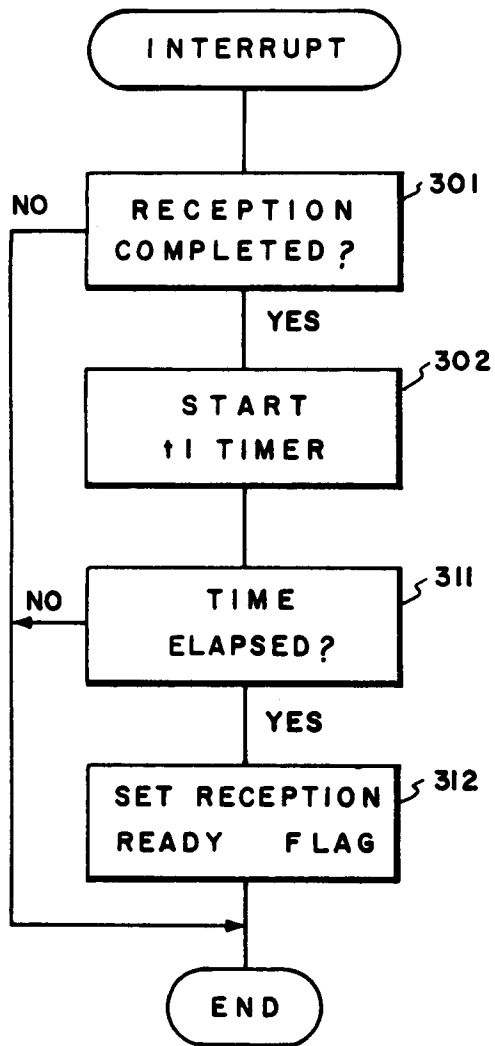


FIG. 8(B)

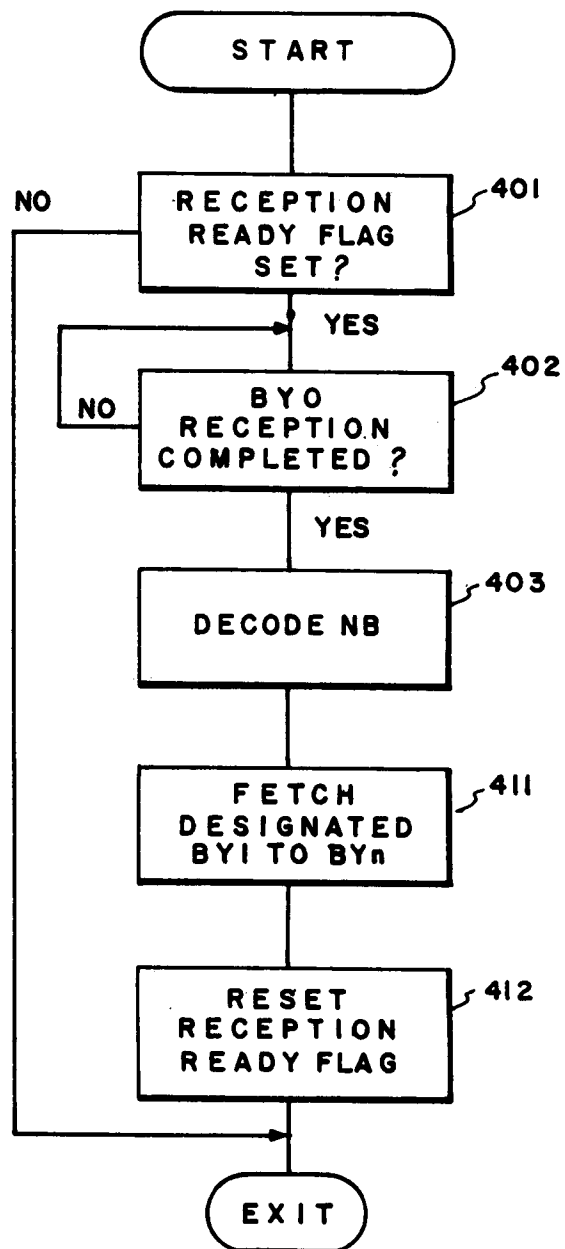


FIG. 9(A)

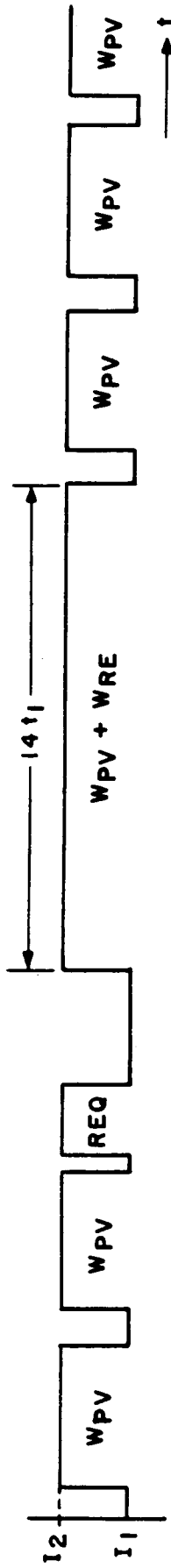


FIG. 9(B)

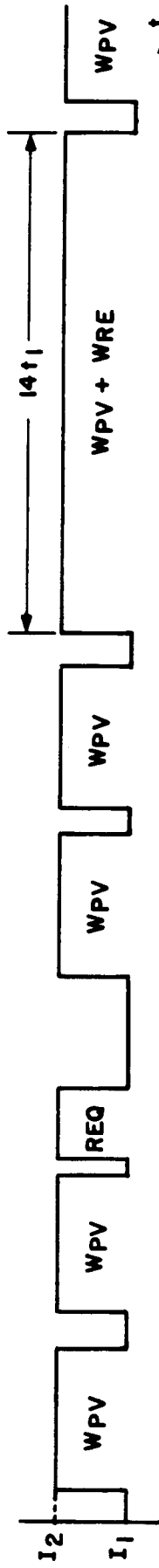


FIG. 9(C)

