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54 Receiver.

57 A receiver for receiving a signal representing a measured value and transmitted through a two-wire transmission line (1_{11} , 1_{21} to 1_{1n} , 1_{2n}), a comparator (81_1 to 81_n) for comparing a received signal with a reference voltage (E_{ref}), extracting a component exceeding the reference voltage, and producing a pulse signal representing the component, and a capacitor (C_{11} to C_{1n}) inserted in series between the input of the comparator and the transmission line for passing only an alternating current (AC) component of the received signal.

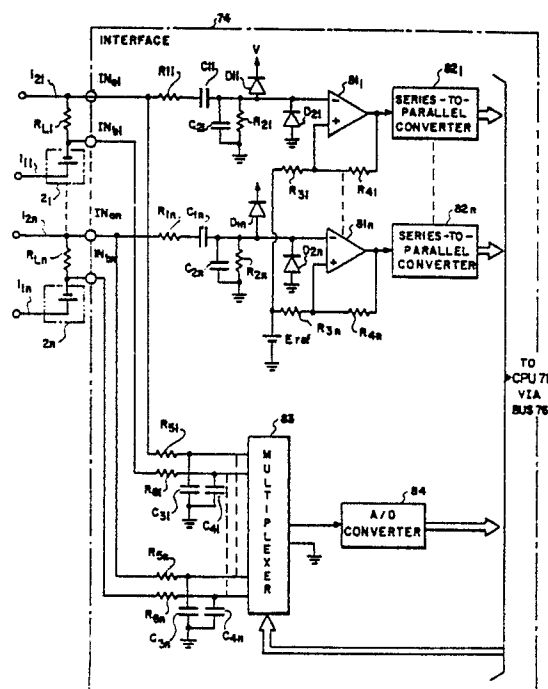


FIG. 3

Receiver

The present invention relates to a receiver according to the preamble of claim 1 suitable for receiving signals supplied through a two-wire transmission line. More specifically, the present invention relates to a receiver for receiving analog and digital signals from a two-wire transmission line.

In order to transmit measured outputs from a process sensor, e.g., a differential pressure transmitter, an electromagnetic flowmeter or the like, to a remote location according to conventional industrial measurement techniques, a unique signal having a current range of 4-20 mA is used. An analog signal having a current selected from this range represents a measured value. Further, a measured value may be transmitted not in the form of analog signal but as a digital signal using the 4-20 mA current, as is disclosed in U.S. Patent No. 4,520,488. Since the use of digital signals improves the transmission speed or bit rate and the reliability of the transmission contents, digital transmission systems have been popular.

A direct current (DC) potential of a transmission line varies according to the conditions for supplying a current onto the transmission line or for transmitting signals. Further, the potential of the transmission line must be compatible with that of a receiver when the transmission line is connected to the receiver.

It is the object of the present invention to provide a receiver which may be used even if a relationship between the DC potentials on a transmission line connected to the receiver is not specified and which is capable of receiving digital data regardless of the magnitude of the data's peak value.

This object is achieved according to the characterizing features of claim 1. Further advantageous embodiments of the receiver according to the invention may be taken from the subclaims.

According to the present invention, there is provided a receiver capable of receiving a signal representing a measured value and transmitted through a two-wire transmission line, comprising a comparator for comparing a received signal with a reference voltage, extracting a component exceeding the reference voltage, and producing a pulse signal representing the component, and a capacitor inserted in series between the input of the comparator and the transmission line for filtering only an alternating current (AC) component of the received signal. In addition to the aforesaid arrangement, there is provided an analog-to-digital converter for converting the received signal into a digital signal.

The capacitor inserted between the input of the comparator and the transmission line blocks the DC component whereby the relationship between the DC potentials at both ends of the capacitor need not be considered. In addition, the AC component of the received signal is extracted so that it can be received regardless of the peak value of the received signal. Furthermore, according to the second aspect of the present invention, the analog signal is converted into the digital signal by the analog-to-digital converter. The digital signal, on the other hand, is extracted by the comparator. Therefore, either signal can be received, and the receiver can be commonly used in the digital and analog systems.

With respect to the figures of the attached drawings the inventive receiver shall be described in detail, where

Fig. 1 is a block diagram showing an overall two-wire transmission system configuration utilizing the present invention,

Fig. 2 is a block diagram of a receiver suitable for use in the system shown in Fig. 2, and

Fig. 3 is a circuit diagram of a receiver according to an embodiment of the present invention suitable for use as the receiver shown in Figs. 1 and 2.

Fig. 1 is a block diagram showing an overall system configuration according to the present invention. A power source (referred to as a PS hereinafter) 2 is connected to one end of a two-wire transmission line (referred to hereinafter as a transmission line) 1 consisting of signal lines 1₁ and 1₂ to supply a current thereto. A transmitter (referred to as a TX hereinafter) 3, such as a pressure differential transmitter or an electromagnetic flowmeter, is connected to the other end of the transmission line 1. The TX 3 controls a current I which is used to generate either an analog signal or a digital signal pulse representing a measured value onto the transmission line 1.

A resistor RL used as a voltage dropping element is inserted in series with the transmission line 1. A voltage drop across the resistor RL is supplied to a receiver (referred to as an RX hereinafter) 4. An output signal from the RX 4 is sent to a main controller (referred to as an MC hereinafter) 6, such as a computer, through a bus 5 whereby control operations are performed on the basis of the measured value represented by the digital signal supplied from the RX 4. An operation unit (referred to as an OP hereinafter) 7, which may include a CRT display and a keyboard, is connected to a bus 5'

and through an interface (referred to as an I/F hereinafter) 9 to bus 5, thereby displaying a controlled state of the equipment and enabling the inputting of a command to the MC 6 and the RX 4.

A portable communicator (referred to as a CE hereinafter) 8 is bridged across the transmission line 1 nearer to the TX 3 than the resistor RL. The CE 8 converts the current I into signal pulses and sends them as a command signal in the form of a digital signal to the TX 3. The TX 3 receives the command signal and converts the current I into signal pulses as a response signal to the command signal. The response signal is then set to the CE 8 over the transmission line 1. A change in the measuring state of the TX 3 can be effected upon a transmission of command data from the CE 8 to the TX 3. Communication between the CE 8 and the TX 3 can also cause a check of the operating state of the TX 3. The detected states can be displayed on a display device incorporated in the CE 8.

Fig. 2 is a block diagram of the RX 4. The RX 4 comprises a processor such as a microprocessor (referred to as CPU hereinafter) 71, a permanent memory (referred to as a ROM hereinafter) 72, a programmable memory (referred to as a RAM hereinafter) 73, and interfaces (referred to as I/Fs hereinafter) 74 and 75. These components are connected to each other through a bus 76. The CPU 71 executes instructions in the ROM 72 and controls reception operation from the bus 76 while accessing predetermined necessary data to the RAM 73. Inputs IN1 to INn from a plurality of transmission lines are supplied to the I/F 74. Digital signals based on changes in currents of the inputs IN1 to INn are sequentially received through I/F 74, and the CPU 71 stores them in the RAM 73 and performs predetermined signal processing. The processed results are sent out to the MC 6 and the OP 7 through the I/F 75. The CPU 71 also stores various other types of data in the RAM 73 according to instruction contents and processes it in response to instructions supplied from the MC 6 or the OP 7 through the I/F 75.

Fig. 3 is a circuit diagram of the I/F 74. Voltages across line resistors RL1 to RLn inserted in a plurality of transmission lines consisting of signal lines 1₁₁ and 1₂₁ to 1_{1n} and 1_{2n} are supplied to input terminals IN_{a1} and IN_{b1} to IN_{an} and IN_{bn}, respectively. The input terminals IN_{a1} to IN_{an} are connected to inverting input terminals of comparators (referred to as CPs hereinafter) 81₁ to 81_n through series-connected resistors R₁₁ to R_{1n} and capacitors C₁₁ to C_{1n}, respectively. Capacitors C₂₁ to C_{2n} and resistors R₂₁ to R_{2n} are connected between the respective inverting inputs of the CPs 81₁ to 81_n and a common circuit. Clamping diodes D₁₁ to D_{1n}

are inserted between the respective inverting input terminals and a power source V so as to clamp input signal overvoltages to the voltage of the power source V.

The resistors R₁₁ to R_{1n}, the capacitors C₂₁ to C_{2n}, and the resistors R₂₁ to R_{2n} constitute noise reduction low-pass filters. At the same time, the capacitors C₁₁ to C_{1n} allow transmission of only AC components of the received signals therethrough and block the DC components of the received signals. Therefore, components of changes in voltages across the resistors R_{L1} to R_{Ln} caused by changes in currents supplied onto the transmission lines are removed by PS₂₁ to PS_{2n}, so that only the AC components are supplied to the inverting input terminals of the CPs 81₁ to 81_n, respectively.

The noninverting input terminals of the CPs 81₁ to 81_n are connected to receive a reference voltage Eref through resistors R₃₁ to R_{3n}, respectively. Positive feedback resistors R₄₁ to R_{4n} are connected between the noninverting input terminals and the output terminals of the CPs 81₁ to 81_n, respectively, thereby providing hysteresis characteristics to the comparison operation.

If currents supplied to the corresponding transmission lines are digital signals as pulse codes, their AC components are compared with the reference voltage Eref by the CPs 81₁ to 81_n. Components exceeding the reference voltage Eref are extracted as pulse signals. These pulse signals are sequentially stored in serial-to-parallel converters (referred to as SPCs hereinafter) 82₁ to 82_n, respectively. The resulting parallel bit digital signals are sent to the CPU 71 through the bus 76.

The potentials at the input terminals IN_{a1} to IN_{an} vary according to the voltages at the PSs 2₁ to 2_n or the ground points. If the pulsed changes in currents supplied to the respective transmission lines fall within 4-20 mA or a different range, their peak values differ from each other and if the reference voltage Eref is not optimally set according to the conditions of the transmission lines and the states of the reception signals, extraction of the pulse signals could be inaccurate and reception errors may occur. However, since only the AC components are filtered through the capacitors C₁₁ to C_{1n}, the constant reference voltage Eref allows an accurate extraction of the pulse signals.

The input terminals IN_{a1} and IN_{b1} to IN_{an} and IN_{bn} are connected to the input terminals of a multiplexer (referred to as an MPX hereinafter) 83 through variation/noise reduction low-pass filters consisting of resistors R₅₁ to R_{5n} and R₆₁ to R_{6n} and capacitors C₃₁ to C_{3n} and C₄₁ to C_{4n}, respectively. The MPX 83 sequentially and repeatedly selects the inputs under the control of the CPU 71 via bus 76. The voltages across the resistors R_{L1} to R_{Ln} are sequentially supplied to an analog-to-digital

converter (referred to as an ADC hereinafter) 84. If the received signals are analog signals, they are converted into digital signals by the ADC 84. The resultant digital signals are sent to the CPU 71 through the bus 76.

In response to an instruction from the OP 7 at the time when the power switch is turned on or a system is modified, maintenance and inspection are performed, i.e., the CPU 71 fetches the outputs from the SPCs 82₁ to 82_n and decodes these input signals. If the measured value is obtained by this decoding, reception processing is performed using the subsequent outputs from the SPCs 82₁ to 82_n. Otherwise, the CPU 71 controls the MPX 83 and receives the outputs from the ADC 84. Upon detection of the measured value, the CPU 71 then performs reception processing using the outputs from the ADC 84. Thus, if the source TX 3 transmits an analog or digital signal, the receiver can perform accurate reception. Even if the source TXs 3 include both analog and digital transmitters, the receiver can alternately use corresponding outputs from the SPCs 82₁ to 82_n and the outputs from the ADC 84 which are selected by the MPX 83.

The number of transmission lines connected to the receiver may be one. In this case, the MPX 83 can be omitted, and at the same time, input/output circuits may be respectively inserted between the SPCs 82₁ to 82_n and the bus 76, and between the ADC 84 and the bus 76. The reference voltage Eref may be an output from a constant voltage element such as a Zener diode.

Claims

1. A receiver (4) capable of receiving a signal representing a measured value and transmitted through a two-wire transmission line (1₁, 1₂), **characterized by** a comparator (81₁-81_n) for comparing a received signal with a reference voltage (Eref) extracting a component from the received signal exceeding the reference voltage, and producing a pulse signal representing the component, and a capacitor (C₁₁-C_{1n}) inserted in series between the input of said comparator and the transmission line for filtering only an AC component of the signal transmitted on the transmission line to produce the received signal for said comparator.

2. A receiver according to claim 1, **characterized in that** the received signal is a digital signal obtained by a change in current supplied onto said two-wire transmission line.

3. A receiver according to claim 1, **characterized in that** the received signal is obtained by utilizing a change in voltage across a voltage drop element (R_{L1}-R_{Ln}) inserted in series in the two-wire transmission line.

4. A receiver according to claim 1 to 3, **characterized by** an analog-to-digital converter (84) connected in parallel to said two-wire transmission line (1₁, 1₂).

5. A receiver according to claim 4, **characterized by** a plurality of two-wire transmission lines (1₁₁, 1₂₁ to 1_{1n}, 1_{2n}) and a multiplexer (83) connected between said transmission lines and said analog-to-digital converter (84).

6. A receiver according to claim 5, **characterized by** low-pass filters (C₂₁, R₂₁ to C_{2n}, R_{2n}; R₅₁, C₃₁; R₆₁, C₄₁ to R_{5n}, C_{3n}; R_{6n}, C_{4n}) at the inputs of said comparators (81₁ to 81_n) and said multiplexer (83).

7. A receiver according to claim 6, **characterized in that** said comparators (81₁ to 81_n) and said multiplexer (83) and said analog-to-digital converter (84) forming part of an interface (74) being connected to and under control of a processor (71) by means of a bus (76).

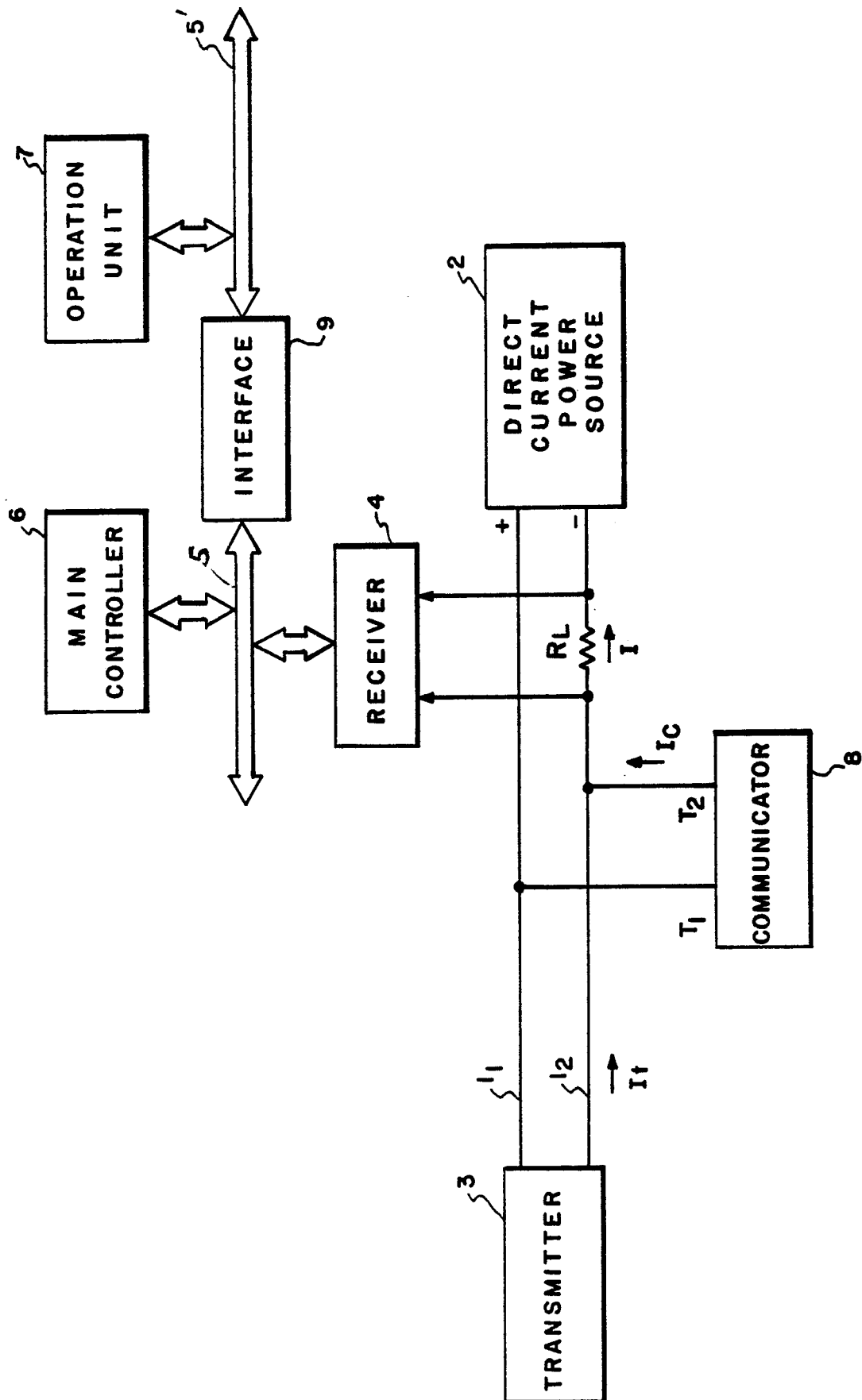


FIG. 1

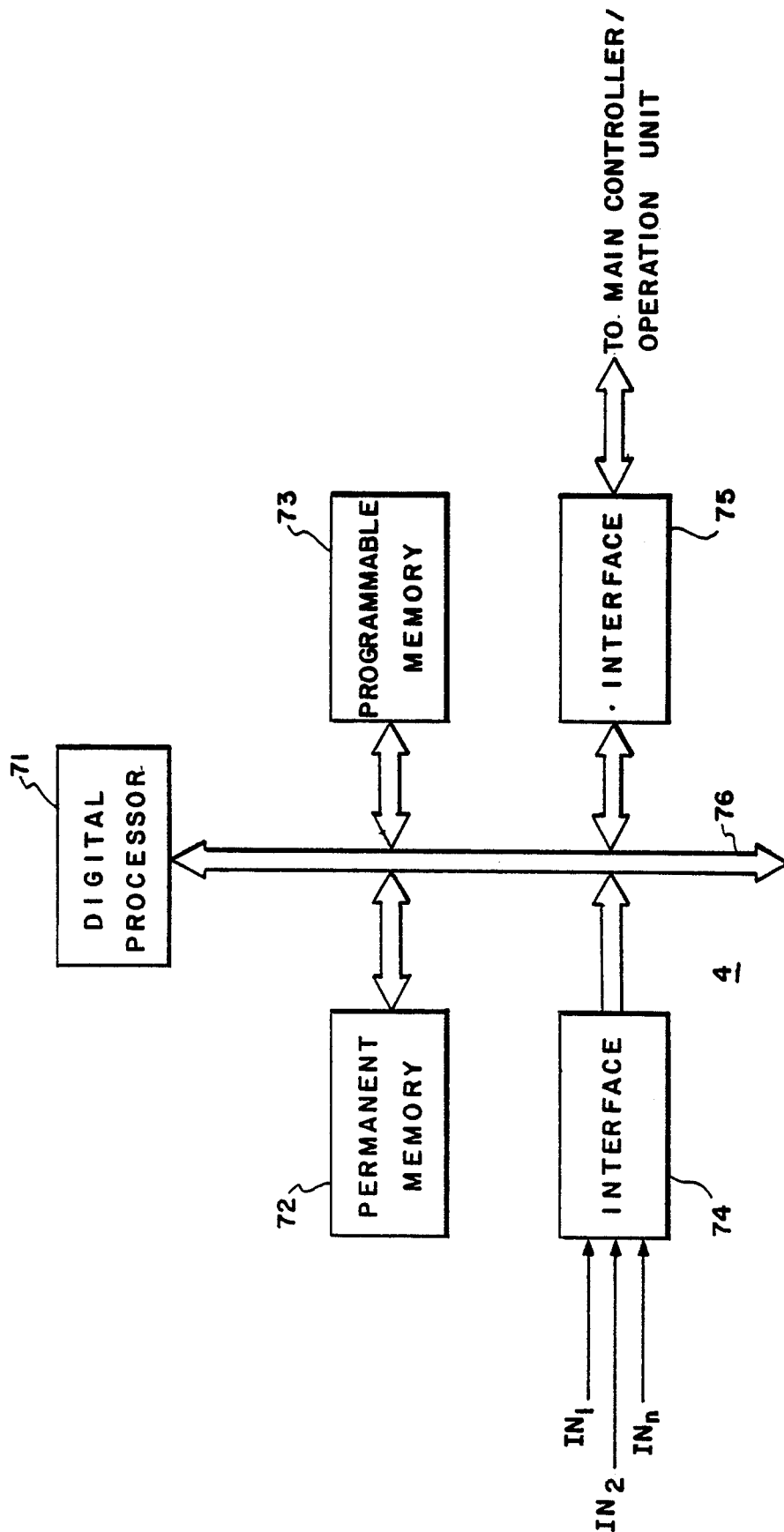


FIG. 2

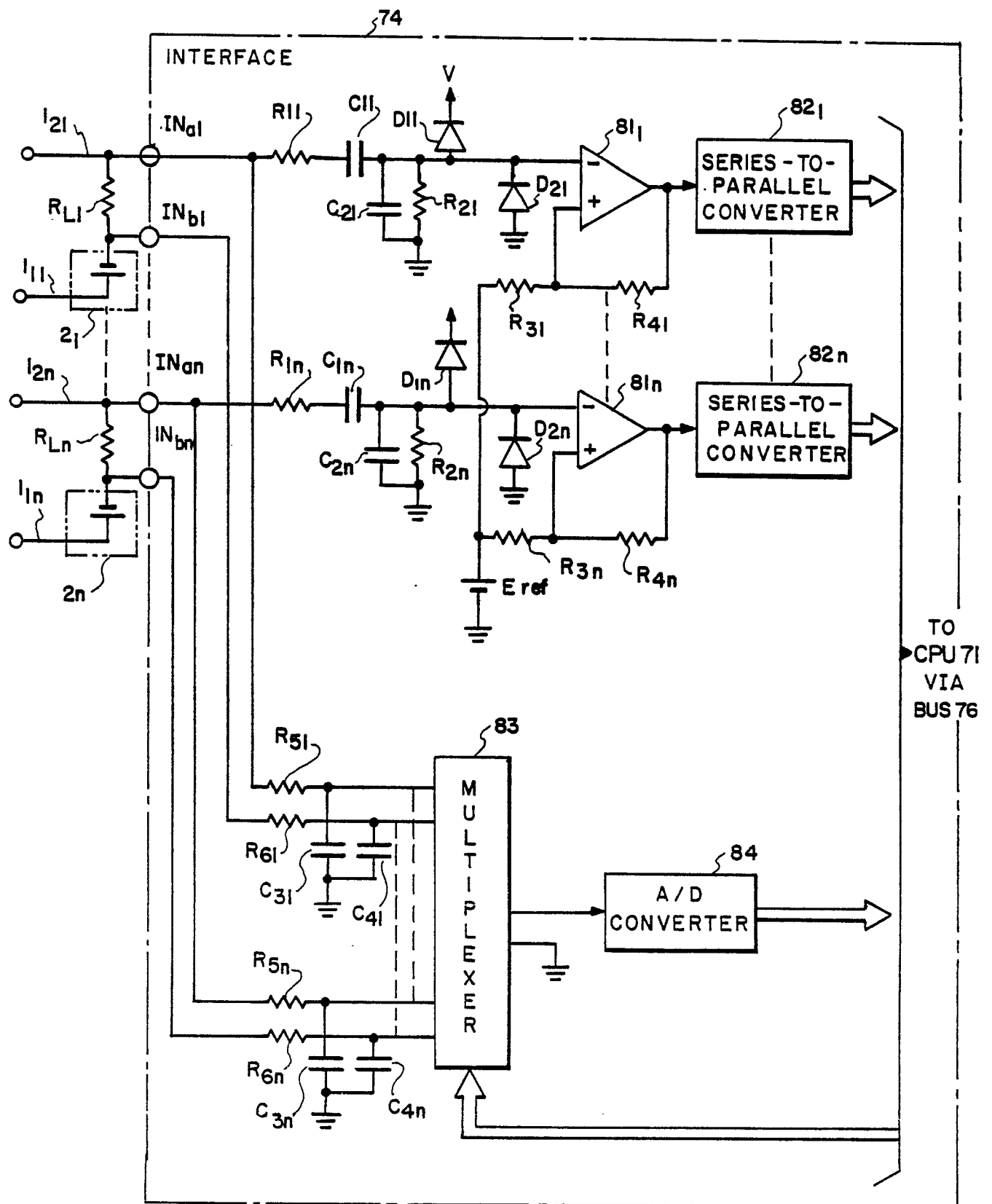


FIG. 3