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(54) Image data processing apparatus and method with display image control function.

(57) A first memory (37) temporarily stores image data. A display (21) displays the image data stored in the first memory. A displayed image change commanding unit (12) applies a command to selectively change and display part of the image data displayed on the display (21). A first controller (31) reads out the part of image data to be selectively changed and displayed from the first memory (37) according to the command. A second controller (31) writes the part of image data read-out by the first controller (31) into a second memory (39).

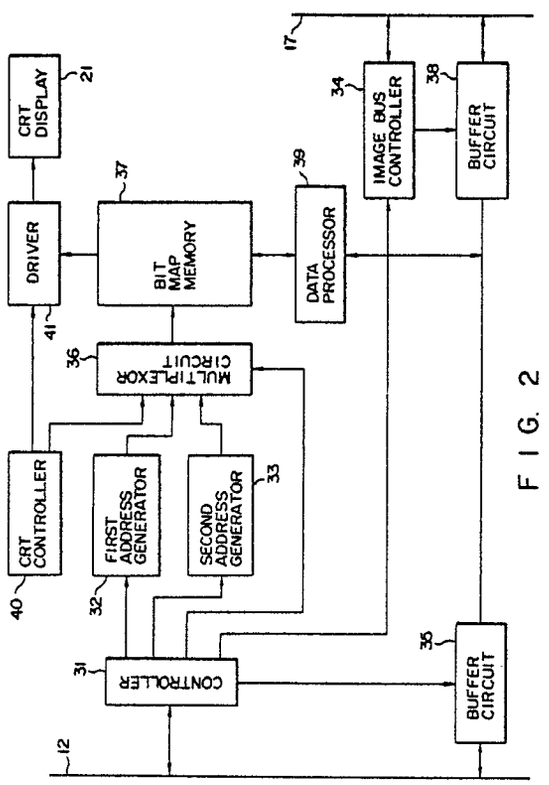

FIG. 2

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Image data processing apparatus and method with display image control function

This invention relates to an image data processing apparatus and method with a display image control function, and more particularly, to an image data processing apparatus and method capable of displaying plural types of superposed image data in a single-window manner or a multi-window manner.

In a known image data processing apparatus, the image data is stored in an optical memory, the stored image data is retrieved when necessary, and the retrieved data is displayed on the CRT display. This type of image data processing apparatus can display a single type or plural types of image data, read out of the optical memory through a page memory and a display memory, on the CRT display.

In the single-window or multi-window display, another image data is displayed overlaid on the currently displayed image data. In this case, the old, or overlaid image data is erased from the display memory, and the new, or overlaying image data is written into the memory. When the overlaying image data is removed, to display the old image data again, that data must be read out of the page memory and written into the display memory. Therefore, a relatively long time is taken for the old image data to be displayed again.

Such a disadvantage is true not only for the overlay display by the single-window or multi-window manner, but also for other general image data processings, such as the processing in which, when part of displayed image is selectively changed and used, it is inconvenient to erase the old image data in the display memory.

It is, therefore, an object of the present invention to provide a new and improved image data processing apparatus and method with a display image control function, which can save part of the image data to be selectively changed and displayed, without any erasure of the image data in the display memory.

Another object of this invention is to provide an image data processing apparatus and method, which solves the problem relating to the select and change time for the displayed image, and can instantaneously display the old image even if the displayed image is selectively changed.

According to one aspect of the present invention, there is provided an image data processing apparatus comprising first and second memory means for temporarily storing image data, means for displaying the image data stored in the first memory means, means for applying a command to selectively change and display part of the image data displayed on the displaying means, first control means for reading out the part of image data to be selectively changed and displayed, from the first memory means according to the command, and second control means for writing the part of image data read out by the first control means into the second memory means.

These and other objects and features of the present invention can be understood through the following embodiment by reference to the accompanying drawings, in which:

Fig. 1 shows in block form a scheme of an image data processing apparatus and method to which an embodiment according to this invention is applied;

Fig. 2 shows in block form the details of a display controller of Fig. 1;

Fig. 3 shows one window on the display screen, which is for explaining the single-window display operation by the above embodiment;

Fig. 4 illustrates an example of a memory map, which is also for explaining the operation of the embodiment;

Figs. 5A to 5E show timing charts for explaining the operation of the embodiment; and

Figs. 6 and 7 show four windows on the display screen, which are for explaining the multi-window display operation by the above embodiment.

An embodiment of this invention will be described referring to the accompanying drawings.

Fig. 1 shows a scheme of an image data processing apparatus. In the figure, GPU 11 executes the address-controls to find an area in a bit map memory (to be described later) in the single-window display and the multi-window display, the area storing desired image data, and controls the operation of the overall image data processing apparatus. This CPU 11 is connected to keyboard 13 for entering the command data, the retrieval data, and the like via system bus 12, magnetic memory device 15 for storing the retrieval data for optical memory device 14, and memory 16 for storing the program to control the operation of CPU 11, for example.

Coupled with system bus 12 and image bus 17 are optical memory device 14 for the image data, page buffer memory 18 of a memory capacity of several pages of displayed image, display controller 19 to be described later, and image controller 20. Display controller 19 is connected to CRT display 21. Display 21 displays the image data read out from optical memory device 14 and the image data read out from two-dimensional scanner 22.

Image controller 20 is connected to printer 23. Priner 23 prints out the image data read out from optical memory device 14 and two-dimensional scanner 22. Image controller 20 comprises an interface circuit for two-dimensional scanner 22 and printer 23, and a compress/extension circuit for compressing the image data (reducing redundancy), and for extending the same (restoring the reduced redundancy to the original state), and an elongation/reduction circuit.

Fig. 2 shows a scheme of display controller 19. System bus 12 is coupled with controller 31 to execute the sequence control, and the control of data transfer. Control section 31 is connected to first and second address generators 32 and 33. It is further connected to image bus controller 34 to control the read and write operation to image bus 17, and buffer circuit 35 connected to system bus 12.

First and second address generators 32 and 33 are independently operable. Each of the generators generates a given write address signal or a read-out address signal in accordance with an address supplied from CPU 11 through control section 31. The address signals generated by first and second generators 32 and 33 are each appropriately selected by multiplexer 36, which is controlled by controller 31, and applied to bit map memory 37.

Bit map memory 37 has a memory capacity capable of storing the image data of several pages of displayed images. The image data coming from through image bus 17 is stored into bit map 37, via data processor 39 including latch circuits, and the like.

To display the image data stored in bit map memory 37, the image data stored in bit map memory 37 is sequentially read out by the display address signal, which is output from CRT controller 40 and supplied through multiplexer 36. The read out image data is supplied to CRT display 21, via drive circuit 41, which is controlled by CRT controller 40.

The single-window display operation of the image data processing apparatus will be described. A specific example to follow is the case where image data B is displayed in a part of image data A already displayed on the screen of CRT display 21, in a single-window manner, as shown in Fig. 3.

In this case, as shown in Fig. 4, the image data which is contained in the area for image data B is read out from image data A. The read out image data is stored in another memory area of bit map memory 37.

CPU 11 outputs the address data to indicate the location on the display screen of CRT display 21 in which image data B is to be displayed. The address data is supplied to first address generator 32, via controller 31. In turn, this generator generates the write address of image data B, i.e., the read out address for image data A corresponding to this image data B. The address signal is supplied to bit map memory 37, via multiplexer circuit 36. At this time, a RAS (row address strobe) signal, a CAS (column address strobe) signal, and a write signal W of bit map memory 37 are placed in a timing at time point T1, as shown in Figs. 5A to 5C. Further, bit map memory 37 is in a read mode. Therefore, by an address signal supplied from first address generator 32, the image data A is read out from a memory area of bit map memory 37 into which the image data B is written. The read out data (Fig. 5D) is latched in data processor 39. Subsequently, at time point T2 shown in Figs. 5A to 5C, write signal W is enabled. At this time, image data B coming through image bus 17 from optical disc 17, for example, is supplied through buffer circuit 38 to data processor 39, under control of image bus controller 34. Through data processor 39, by the address signal generated from first address generator 32, the image data B is written into the memory area from which the image data in image data A is read out (W1 in Fig. 5D). In Fig. 5E, Ta indicates a period during first address generator 32 generates the address signal.

Then, second address generator 33 generates an address signal for bit map memory 37 to write the image data, which has been latched in data processor 39. This address signal is supplied to bit map memory 37, via multiplexer circuit 36. At time point T3 in Fig. 5, write signal W is enabled. At this time, the image data latched in data processor 39 is stored into the area of the bit map memory as specified by the address signal. See W2 in Fig. 5D. In the figure, To indicates the period during second address generator 33 generates the address signal.

Repeating such an operation, image data B can be inserted, while the image data in the memory area corresponding to the image data B in image data A is being stored in another area of bit map memory 37.

As shown in Fig. 3, when image data B is being displayed overlaid on image data A, image data B is removed, as in the above case, first address generator 32 generates an address signal for reading out the image data stored in the other area of bit map memory 37. By this address signal, the image data is read out from bit map memory 37, and latched in data processor 39. Afterwards, an address signal for the area of the image B in image data A, is generated by second address generator 33. By the address signal, the image data latched by data processor 39 is written into image data A, and image data A is recalled. These image data processings in bit map memory 37 are performed during the fly-back period of CRT display 21.

Figs. 6 and 7 show the multi-window display operation of the image data processing apparatus. The specific example to follow is the case of a display incorporating four-windows (211-214), and the case where a part of image data C already displayed on the second window 212 on the screen of CRT display 21 is displayed overlaid on a part A of image data A and B already displayed on the first window 211 on the screen of CRT display 21. In this case, image data A is stored in the other area of memory 37. The operation of Figs. 6 and 7 can be executed with the same manner that of Fig. 3.

With the above-mentioned embodiment, in the single-window display and the multi-window display, the image data in the area on the screen into which another image data is inserted, is not erased, but read out, and stored into the other area of bit map memory for display. To reproduce the previous image, the image data stored in the other area of the display memory is recalled and written in the original area where the data was previously stored. With this feature, there is no need, unlike the prior art, for reading out the data from the optical disc into the display memory, in order to reproduce the image data. Therefore, the image switching speed is improved.

It should be understood that this invention is not limited to the above-mentioned embodiment, but can be variously changed and modified within the scope of this invention.

For example, in the embodiment, the selective change of display image in the single-window display and the multi-window display has been described. This invention is not only applicable to the single-window display and the multi-window display, but also to the other types of display including the normal display.

Also, for a selective change control of the display image, there is a specific sequence of controls: the previous image data is read into the other memory area after it is read; when the previous display image is recalled, it is written into the original memory area. However, there are other types of image data processings than the above. The function essentially required for the image data processing apparatus with display image control function according to this invention is only to save the original image data, not to erase it in the display memory. Other functions may be used in combination with the above function, when necessary.

As seen from the foregoing, according to this invention, there is provided an image data processing apparatus and method having a display image control function to save the image data to be selected and changed in a specific area on the screen, and not to erase it in the display memory.

Claims

1. An image data processing apparatus comprising:

first and second memory means (37, 39) for temporarily storing the image data; and

means (21) for displaying the image data stored in said first memory means (37);

characterized by further comprising:

means (12, 13) for applying a command to selectively change and display part of the image data displayed on said display means (21);

first control means (31) for reading out said part of image data to be selectively changed and displayed from said first memory means (37), according to said command; and

second control means (31) for writing said part of image data read out by said first control means (31) into said second memory means (39).

2. The image data processing apparatus according to claim 1, characterized in that said first control means (31) includes means (32) for generating a read address corresponding to said part of image data to be selectively changed and displayed, and means (36) for reading out said part of image data from said first memory (37) means by the read address.

3. The image data processing apparatus according to claim 1, characterized in that said second control means includes means (33) for generating a predetermined write address, and means (36) for writing said part of image data into said second memory means (39) by the predetermined write address.

4. The image data processing apparatus according to claim 1, characterized in that said apparatus further comprises means for causing display of other image data by said displaying means in an area selected by said command.

5. An image data processing apparatus comprising:

means for temporarily storing image data, said storing means including first memory area (37) and second memory area (39); and

means (21) for displaying the image data stored in said first memory area (37);

characterized by further comprising:

means (13) for indicating a part of the image data displayed on said displaying means (21);

first control means (31) for reading out the part of image data indicated by said indicating means (13) from said first memory area (37);

second control means (31) for writing the part of image data read out by said first control means into said second memory area (39);

third control means (11) for applying a command for displaying again on said displaying means (21) the part of image data stored in said

second memory area (39); and

fourth control means (31) for reading out the part of image data from said second memory area (37) according to said command, and for writing the part of image data read out from said second memory area (39) into said first memory area (37).

6. The image data processing apparatus according to claim 5, characterized in that said first control means (31) includes means (32) for generating a read address corresponding to said part of image data to be selectively changed and displayed, and means (36) for reading out said part of image data from said first memory area (37) by the read address.

7. The image data processing apparatus according to claim 5, characterized in that said second control means (31) includes means (33) for generating a predetermined write address, and means (36) for writing said part of image data into said second memory area (39) by the predetermined write address.

8. The image data processing apparatus according to claim 5, characterized in that said fourth control means (31) includes means (32) for generating a read address for reading out said image data that has been written into said second memory area (39); means (36) for reading out said part of image data from said second memory area (39) by the read address; means (33) for generating a write address corresponding to the reading out of said part of image address from said first memory area (37) by said first control means (31); and means (36) for writing said read-out part of image data into said first memory area (37) by the write address.

9. The image data processing apparatus according to claim 5, characterized in that said part of image data from said second memory area is written in the same address that of said read-out part of image data from said first memory area by said first control means.

10. The image data processing apparatus according to claim 5, characterized in that said apparatus further comprises fourth control means (31) for reading out said part of image data from said first memory area (39), and for displaying said read-out part of image data from said first memory area (37) on said display means (21).

11. The image data processing apparatus according to claim 5, characterized in that said apparatus further comprises means for causing display of other image data by said displaying means in an area selected by said command.

12. An image data processing method comprising the steps of:

temporarily storing the image data in a first memory; and

displaying the image data stored in said first memory on a display;

characterized by

first, applying a command to selectively change and display part of the image data displayed on said display;

first, reading out said part of image data to be selectively changed and displayed from said first memory according to the command;

first, writing said part of said image data read out from said first memory into a second memory;

second, applying a recall command for displaying again on said display said part of image data which has been changed according to the command;

second, reading out said part of image data from said second memory according to the recall command, and

second, writing said read-out part of image data from said second memory into said first memory.

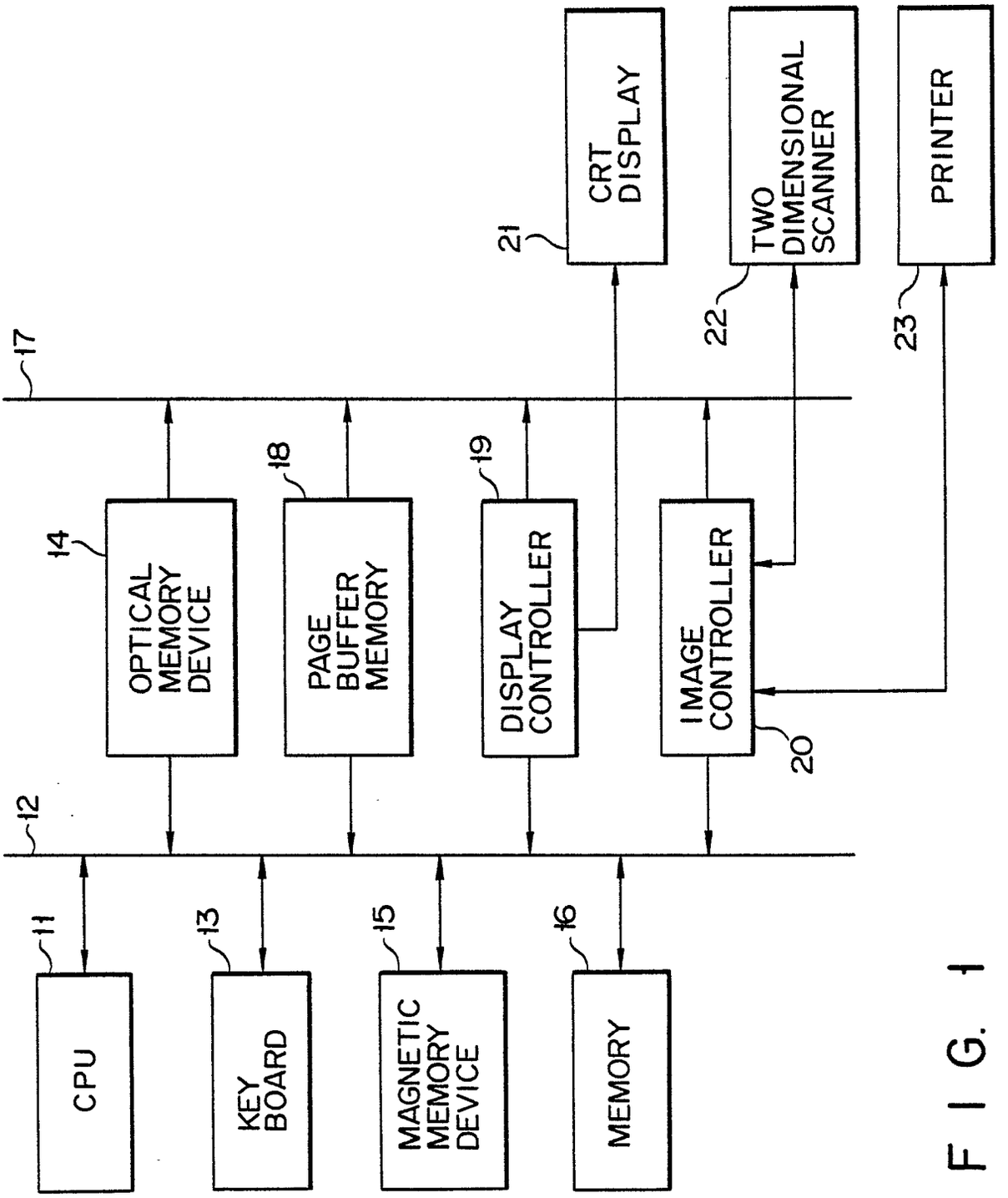

CPU
11
KEY BOARD
13
MAGNETIC MEMORY DEVICE
15
MEMORY
16
12
OPTICAL MEMORY DEVICE
14
PAGE BUFFER MEMORY
18
DISPLAY CONTROLLER
19
IMAGE CONTROLLER
20
17
CRT DISPLAY
21
TWO DIMENSIONAL SCANNER
22
PRINTER
23

FIG. 1

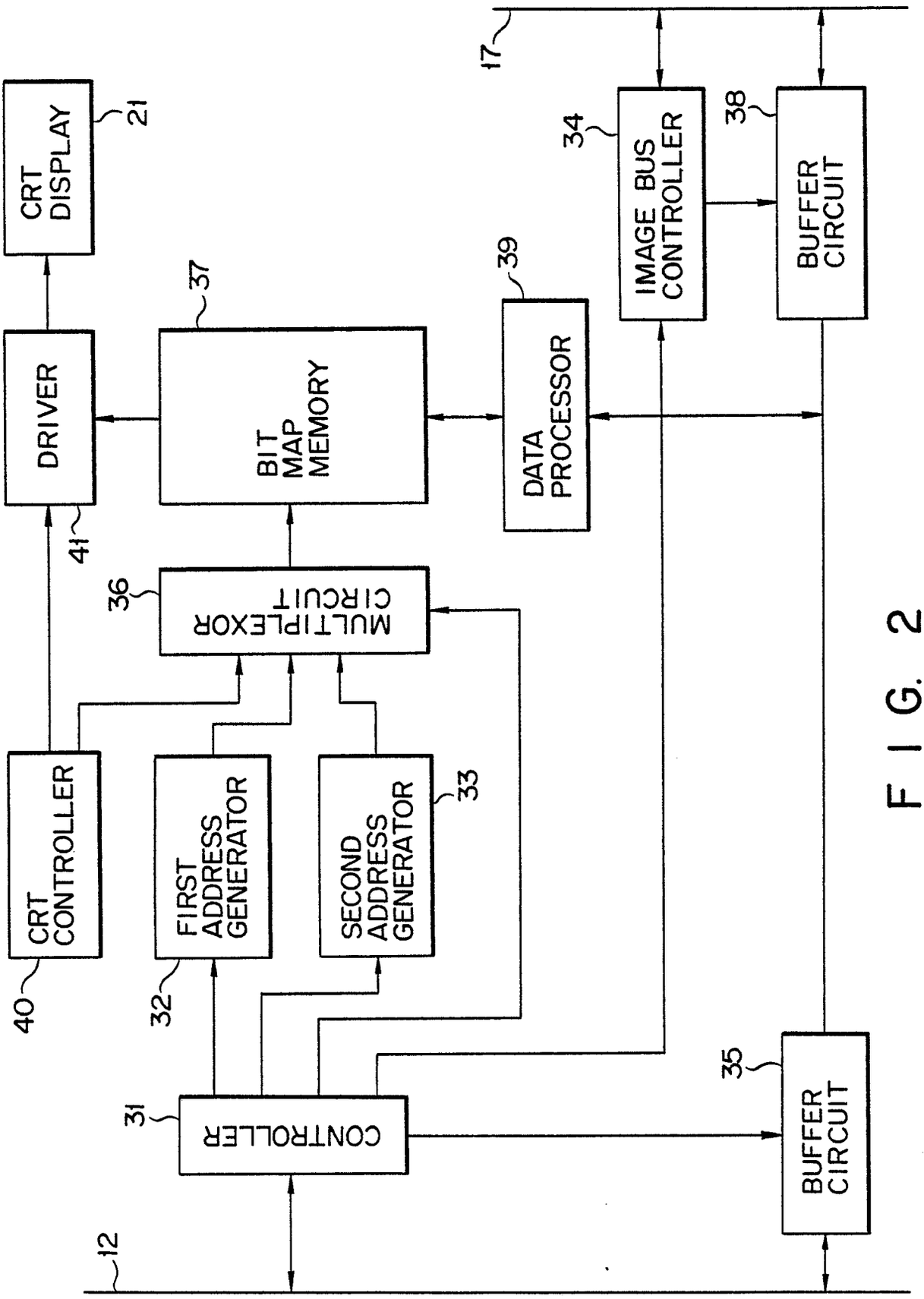
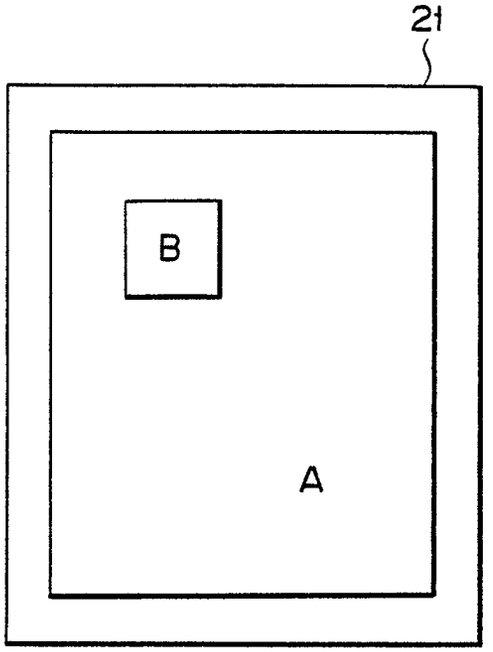
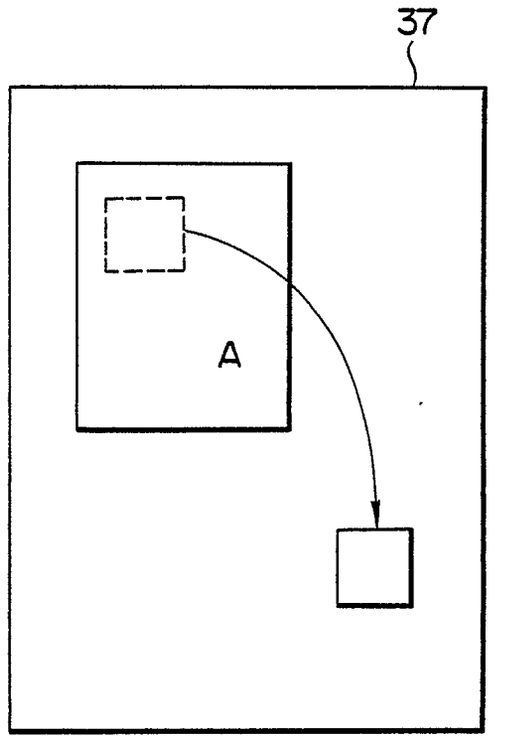

17
CRT DISPLAY
21
IMAGE BUS CONTROLLER
34
BUFFER CIRCUIT
38
DRIVER
37
BIT MAP MEMORY
39
DATA PROCESSOR
41
MULTIPLEXOR CIRCUIT
36
CRT CONTROLLER
40
FIRST ADDRESS GENERATOR
32
SECOND ADDRESS GENERATOR
33
CONTROLLER
31
BUFFER CIRCUIT
35
12

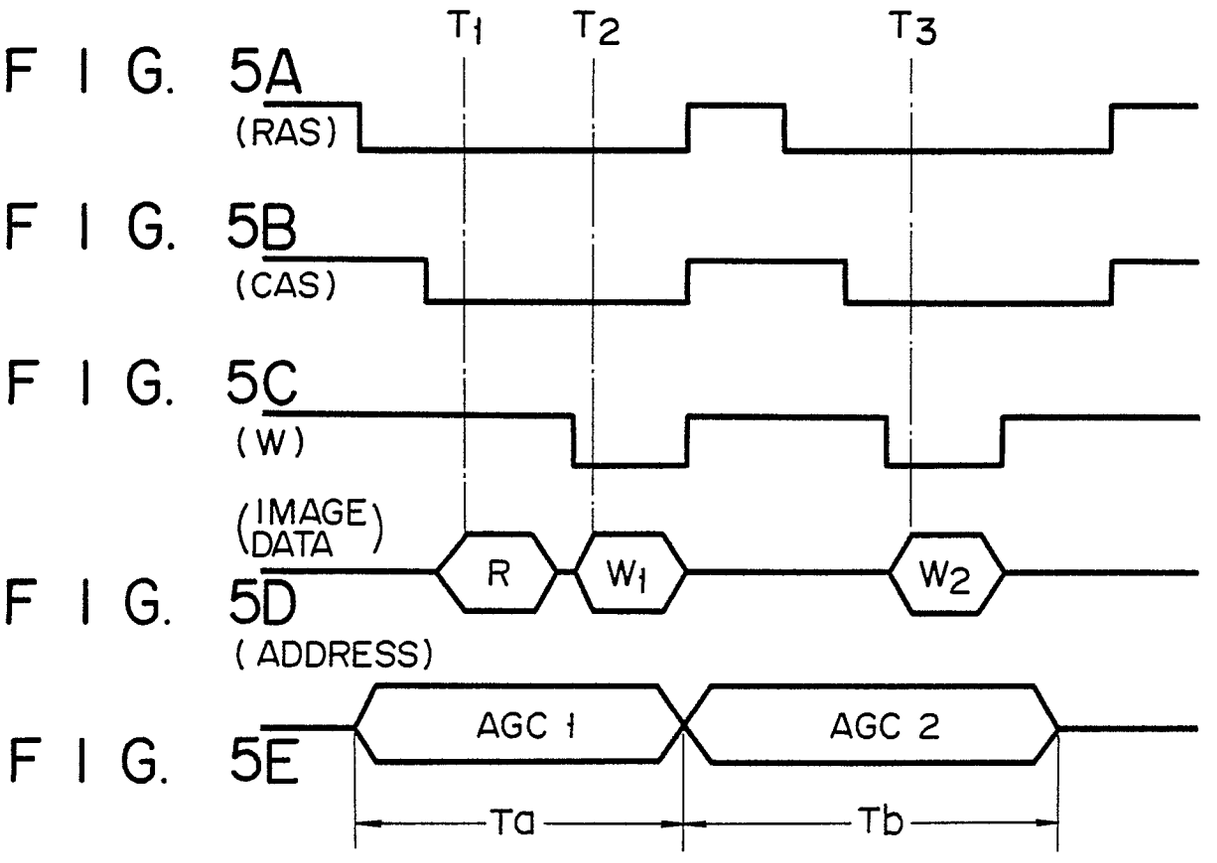
FIG. 2



F I G. 3



F I G. 4



F I G. 5A

F I G. 5B

F I G. 5C

F I G. 5D

F I G. 5E

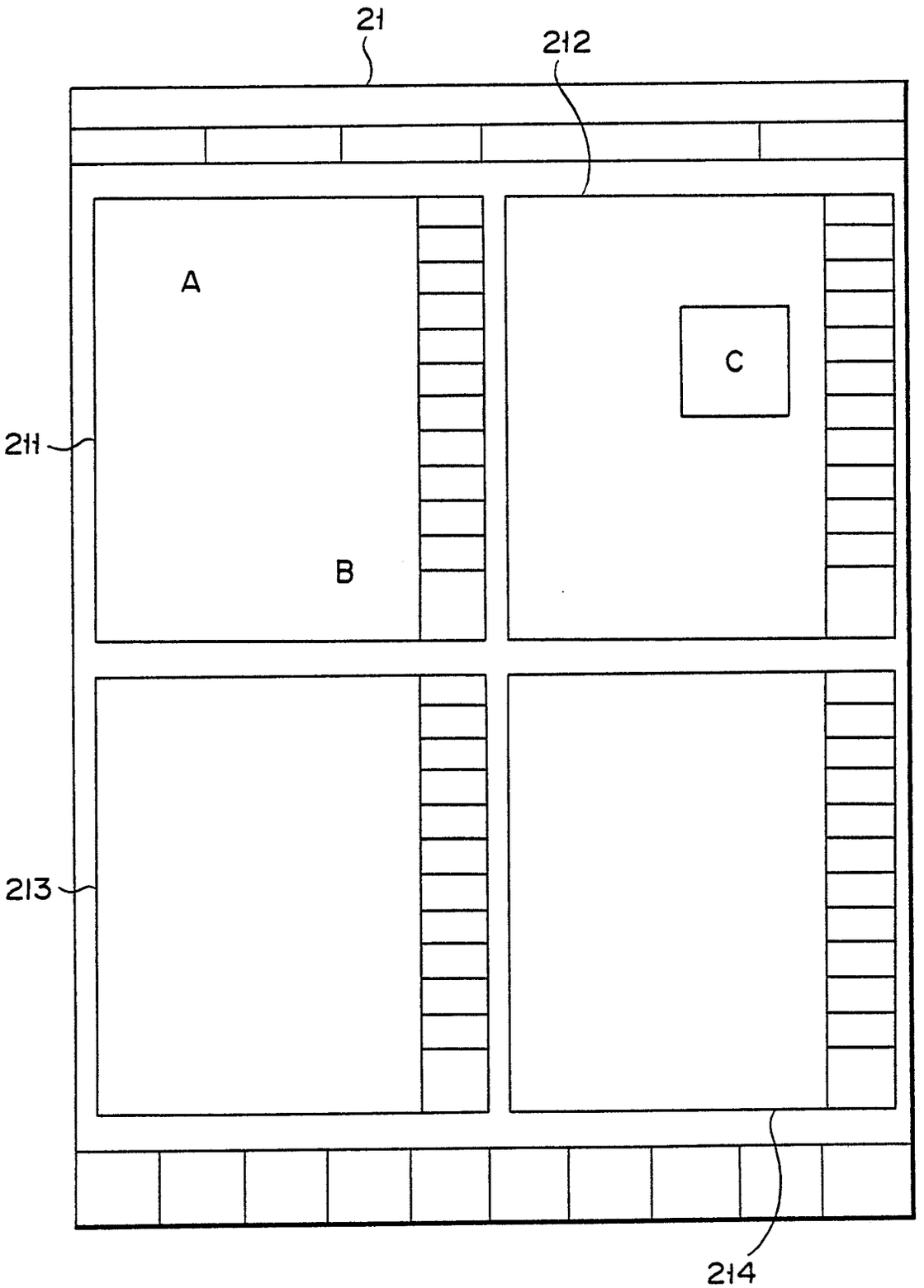


FIG. 6

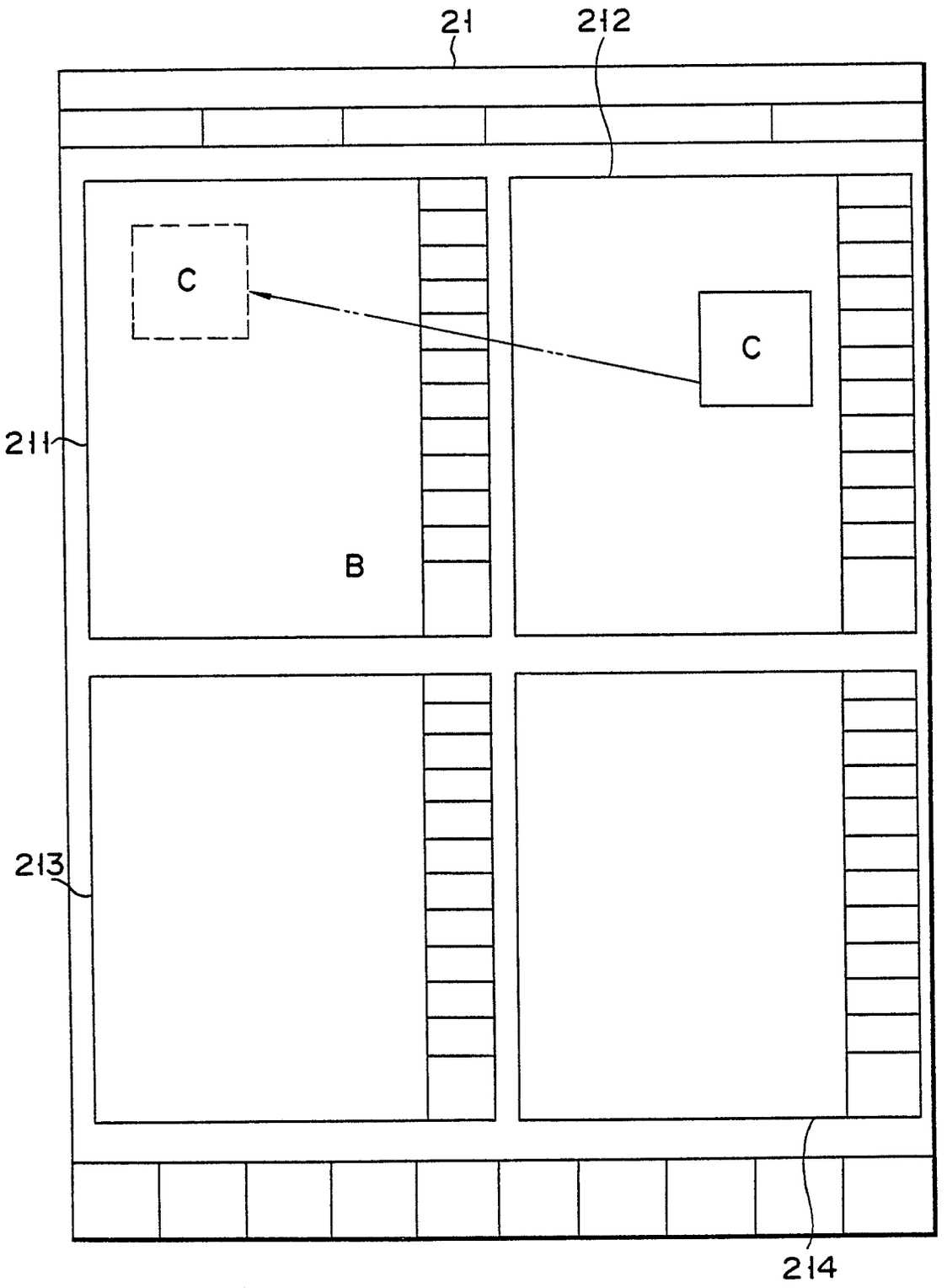


FIG. 7