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(54) **Latching phase shifters.**

(57) A ferrite phase shifter is described in which the switching circuit is arranged to apply a complementary setting pulse to a latching wire (4) of a toroidal ferrite phase shifter (2) before a resetting current pulse is applied by means of a latching wire (6). A new phase state is then set by a normal setting pulse applied to the latching wire (4). The complementary setting pulse is of a voltage sufficient to bring the magnetisation state of the phase shifter to an unsaturated magnetic state. This may be achieved by applying a complementary setting pulse of a voltage which together with the voltage of the previous setting pulse adds up to a constant amount. Alternatively, the magnitude of the complementary setting voltage may be determined on an empirical basis in order to reduce the phase error in any subsequently set phase. This may result in the unsaturated magnetic state varying in dependence on the previously set state.

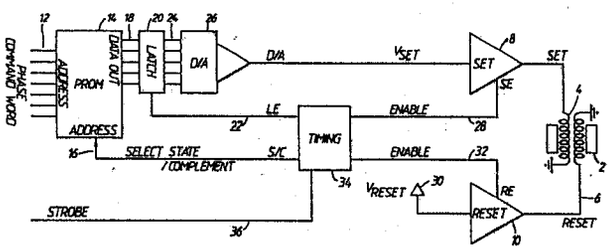

FIG. 2.

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Description

LATCHING PHASE SHIFTERS

The present invention relates to latching phase shifters and, more specifically, to switching circuits used in association with such phase shifters for controlling the phase shift produced.

Latching microwave phase shifters are well known in the art. Typically such a phase shifter comprises a toroid of ferrite or other magnetic material, such as garnet, which defines a closed magnetic flux path. A latching wire passes through the toroid and is connected to a switching circuit. The magnetisation state and therefore the phase shift produced can be changed by applying a voltage pulse to the latching wire in order to produce a magnetising field H, the magnitude of which will depend on the current passing through the latching wire. This results in a change of the magnetisation state and therefore a change of the phase shift produced by the device which depends on the duration of the pulse, the magnitude of the voltage applied and the current drawn in a known manner.

Figure 1 shows diagrammatically a hysteresis loop illustrating how the magnetisation state M will change in response to the application of a magnetising field H.

Supposing the initial magnetisation of the ferrite toroid is the remanent negative magnetisation $-M_r$. The application of a positive-going voltage pulse causes the magnetisation to move along the hysteresis curve in the anti-clockwise direction as shown. The distance moved along the curve will depend on the magnitude and duration of the voltage pulse applied to the latching wire. If the magnetisation state reaches M_a as indicated at the end of the pulse, the magnetisation state will fall back to the value M_b after removal of the pulse since the magnetising field H returns to zero magnitude. The relationship between the magnetisation state and the phase shift which will be produced in a wave propagating in a waveguide containing the toroidal phase shifter is well know. Therefore, by arranging for the switching circuit to produce first a large negative going pulse producing a saturated magnetisation, $-M_r$ and then a setting voltage pulse of known magnitude for a fixed duration, the phase shifter can readily be set to produce an approximation to the required phase shift.

Under normal circumstances, before each set pulse is applied, the switching circuit produces a negative going current resetting pulse to bring the magnetisation state of the ferrite to M_{RS} and, subsequently to $-M_r$ after the resetting pulse is removed. The set pulse is then applied to achieve the desired magnetisation state. However, some remanent memory of the previous magnetisation state is still retained so that if that previous state was lower than the new state, the actual new state achieved will still be less than the desired value. If the new magnetisation state required is less than the previous state then the new state achieved will be higher than the required new state. The actual state will converge towards the required new state after a number of cycles of resetting and setting. However, this introduces a considerable delay before accurate operation of the phase shifter is achieved. Various switching systems have been proposed to improve the accuracy of such ferrite phase shifters by removing the dependence of the set phase shift on the previously set phase shift. For example, it has been proposed to try and eliminate the remanent memory by applying positive-going current to avieve a full set magnetisation state $+M_{FS}$ before applying the resetting pulse and subsequently the required setting pulse. It has been found experimentally that this gives only a partial improvement and some memory of the previous state is still retained. Resetting and Full-setting also result in considerable power consumption by the switching circuit as the reset consistently requires a change of flux equal to $2M_r$.

Reference may be made to EP-A-0 139 800 (Electromagnetic Sciences Inc) which provides a description of a latching phase shifter and prior art switching circuits as outlined above.

In some applications a phase shifter of the described type may be required for use in a waveguide which is operable in both transmit and receive modes. Since the propagation direction is reversed between these modes, the required magnetisation state is opposite in sign in the two modes although the magnitude of the phase shift required remains the same. Therefore, for the transmit mode, the switching circuit connects the latching wire to a positive voltage source, and for the receive mode to a negative voltage source, or vice versa. In existing systems for switching between transmit and receive modes, it has been necessary to fully set the phase shifter before it can be set to the required phase shift for the receive mode. Similarly, to switch between the receive and transmit modes a resetting pulse must be applied by the switching circuit. Such an arrangement produces the same problems as outlined above with regard to the accuracy of the set phase shifts.

The present invention is therefore directed towards providing a switching circuit which will improve the accuracy of a latching phase shifter.

The present invention accordingly provides a latching phase shifter comprising a magnetic material defining a closed magnetic flux path, magnetising means associated with the magnetic material for applying a magnetising field thereto, and a switching circuit connected to said magnetising means and comprising means for controllably switching the magnetic material from a previously set magnetisation state to a selected unsaturated magnetisation state, and means for then switching the magnetic material to a desired new magnetisation state.

The use of an intermediate but unsaturated state of magnetisation is found to achieve a considerable improvement in removing the remanent memory of the previously set state.

The intermediate state is ideally produced by a

pulse "complementary" to that required to produce the previously set state The magnitude of complementary setting pulses may be determined empirically or a voltage pulse of a predetermined duration can be used which has a magnitude which, when added to the magnitude of the voltage pulse of the same duration required to produce the previously set state, adds up to a predefined value. In an alternative embodiment the voltage for switching to an unsaturated intermediate magnetic state is empirically determined so that the same unsaturated magnetic state is achieved independent of the previously set magnetisation state. An empirical determination of the voltage for switching to the unsaturated state can be made using the criterion that the achieved phase error is minimised.

It is found that the phase shifter of the present invention provides considerably greater flexibility than the use of a full set pulse and produces good accuracy with a lesser penalty in power and switching speed.

A latching phase shifter embodying the present invention will now be described, by way of example only, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a plot of a hysteresis loop for explaining prior art switching systems;

Figure 2 is a block diagram of a control circuit for a latching phase shifter in accordance with the present invention;

Figures 3A - 3D are plots of hysteresis loops showing the sequence of changes of magnetisation taking place in the phase shifter switched in accordanc with the present invention;

Figure 4 is a timing diagram illustrating the various signals occuring in the circuit of Figure 2;

Figure 5 is a plot of magnetisation state versus time as the latching phase shifter is cycled through a repeated sequence of setting cycles showing a comparison of the performance of switching strategy of the present invention with that of the prior art; and

Figures 6A and 6B show plots of the voltage pulses required to be produced by a switching circuit of a phase shifter for use alternately in transmit and receive modes, in accordance with the prior art and an embodiment of the invention respectively.

Figure 2 illustrates a switching circuit for a phase shifter which comprises a toroid of ferrite material 2 which is placed in a microwave waveguide. A pair of latching wires 4, 6 pass through the toroid to enable a magnetising field H to be applied. Each of the latching wires 4, 6 comprises a coil having one terminal connected to earth or other fixed DC potential. The other terminal of latching wire 4 is connected to the output of a setting amplifier 8, and the other terminal of latching wire 6, is connected to a resetting amplifier 10.

A set of parallel input lines 12 to a programmable read-only memory (PROM) 14 carry a digital representation of a commanded phase shift to be produced by the phase shifter 2. The input lines 12 together with a further input on a select state/complement line 16 provide the address inputs which select a location in the PROM. For each phase command word, the PROM therefore contains one data word for the required state, and a further data word for the complement. The data stored at the location indicated by the address is output on lines 18 to a latch 20 which has a latch enable input connected to line 22. When the latch enable input goes high, the contents of the latch are passed on lines 24 to a digital to analogue converter 26 which converts the digital representation to an analogue signal of the required magnitude which is passed to an input of the set amplifier 8. The set amplifier 8 has a set enable input connected to line 28. While the set enable input is high, the set amplifier 8 produces a voltage pulse on the latching wire 4 of a magnitude determined by the original phase command word fed to the PROM. The magnitude of the voltage is selected to be sufficient to produce a magnetising field to produce the required magnetisation change in the ferrite phase shifter from its previous magnetisation state.

The reset amplifier 10 is connected to a reset power supply 30 and has an enable input line connected to 32. While the enable input is high, the reset amplifier 10 produces a current pulse in the latching wire 6 in order to produce a negative magnetising field which produces a magnetisation M_{RS}, resulting in a final magnetisation $-M_r$.

A timing circuit 34 has a strobe input 36 on which it receives a series of regular timing impulses The timing circuit 34 produces the required sequence of control signals on lines 16, 22, 28 and 32 as described more fully with reference to Figure 4.

The switching circuit of Figure 2 operates to produce the magnetisation state changes required during a setting cycle of the phase shifter. Figure 3A shows the magnetisation change required to produce the magnetisation state M_1 of a previous setting cycle. At the start of the next setting cycle, a complementary setting pulse is applied via the setting amplifier 8 to produce a magnetisation state $\widetilde{M}_1$. $\widetilde{M}_1$ may be a fixed unsaturated state or may depend on the magnitude of M_1. After the complementary setting step illustrated in Figure 3B, a resetting pulse is applied to latching wire 6 in order to reset the phase shifter to a magnetisation state M_{RS}. The magnetisation state returns to $-M_r$ after the resetting pulse has terminated, and the ferrite toroid is ready for a new setting pulse from the setting amplifier 8 of a magnitude sufficient to produce the next set magnetisation value M_2 as shown in Figure 3D.

Since magnetisation in the switching cycle very nearly follows the same outer path on the hysteresis loop, during each switching cycle, undesirable variability of the set phase is minimised.

The timing diagrams of Figure 4 will now be used to describe the operation of the switching circuit to produce the magnetisation changes of Figure 3 in more detail.

Plot A shows the strobe input signal on line 36. A strobe pulse marks the start of each new setting cycle. Plot B indicates the phase word applied to the input lines 12. If the set phase is to be changed in the

next cycle, the phase word input on lines 12 is changed shortly before the start of the cycle as illustrated in plot B. Although the phase command word on input lines 12 has changed, the latch 20 will still contain the contents of the memory location addressed by the previous command word together with the address bit supplied by the input line 16 until the latch enable input once more goes high to replace the contents of the latch 20 with the data stored at the location indicated by the new phase command word.

Plot C shows the level of the input signal on the address line input 16. The level of this input signal determines whether a state address location in the PROM or a complement address location in the PROM is addressed by the phase command word. When the level of the signal on input 16 is low representing an "0" bit, the phase command word together with this "0" bit provided by input 16 addresses a location at which the value stored represents the magnitude of the voltage pulse required to achieve the magnetisation state needed to achieve the commanded phase. In the complement location addressed by the phase command word together with a "1" bit from input 16, there is stored data representing the magnitude of the voltage pulse required to produce the magnetisation change illustrated in Figure 3B to shift the magnetisation state from the previously set value to a given unsaturated value which is either fixed for all set magnetisation states or made to vary in dependence on the previously set magnetisation state. Since the latch enable signal went high in the previous cycle when the input on line 16 was high, the complement value for the previous set magnetisation state will be stored in the latch 20 at the commencement of the next setting cycle.

Plot D shows the signal on the set enable line 28. When the set enable line goes high, the analogue equivalent of the contents of the latch 20, which is always fed to the input of the amplifier 8, causes the amplifier 8 to produce an output which is a voltage pulse having a magnitude dependent on the contents of the latch and having a duration corresponding to the time for which the set enable pulse is high.

Plot E shows the signal on the reset enable line 32. When the reset enable input is high the reset amplifier 10 produces an output which is a current pulse.

Plot F shows the level of the signal on the latch enable line 22. When the latch enable input goes high, the data presented on lines 18 from the PROM 14 replaces the current contents of the latch.

Plot G shows the output of the digital to analogue converter 26 which is fed to the input of the set amplifier 8.

Plot I shows the output of the set amplifier 8. It will be noted that the amplifier 8 only produces an output when the set enable input as shown in plot D is high. The magnitude of the voltage pulse produced depends on the magnitude of the input to the set amplifier as shown in plot G.

Plot J shows the output from the reset amplifier 10. It will be noted that the reset amplifier only produces an output when the reset enable signal shown in plot E is high.

As discussed above, the contents of the latch 20 at the start of a cycle represent the contents of the complement location of the PROM for the previous phase command word. A predetermined period after receipt of the strobe pulse on line 36, the timing circuit 34 outputs a set enable pulse on line 28 as shown in plot D. This causes a voltage pulse to be applied to the latching wire 4 from the set amplifier 8. This voltage pulse is referred to as a complement pulse since its magnitude is complementary to the magnitude of the set pulse of the previous cycle. In one embodiment the voltage of the complement pulse and the previous set pulse will add up to a fixed value corresponding to a fixed final magnetisation state M_X which is independent of the previously set state. In order to achieve the same final magnetisation state for all previous set states, this may require a somewhat larger or smaller voltage than expected because of the position on the hysteresis loop of the set state.

A predetermined period after producing the set enable pulse, the timing circuit 34 produces a reset enable pulse as shown in plot E. This reset enable pulse causes a reset current to be applied by the amplifier 10 to the latching wire 6 as shown in plot J. This causes the magnetisation of the phase shifter 2 to follow the path indicated in Figure 3C.

At the same time as producing the reset enable pulse, the timing circuit 34 produces a latch enable pulse. It will be noted that there is no need for the synchronism between the reset enable and latch enable pulses. The latch enable pulse must only occur between the set enable pulses in plot D. As a result of the latch enable pulse the contents of the PROM location addressed by the input 12 and 16 is stored in the latch 20. At this time the phase word presented on the address inputs 12 correspond to the phase shift to be set in this cycle. Since the signal on the select state/complement line 16 as shown in plot C is low, the contents of the state location for this phase shift are stored in the latch 20. As illustrated in plot G this causes the output of the D/A converter to change to a voltage level appropriate to the new state. A predetermined period after the latch enable has been completed, the timing circuit 34 produces a further set enable pulse as shown in plot D. This results in the set amplifier producing a set pulse of an appropriate magnitude to cause the magnetisation of the phase shifter 2 to move along the path indicated in Figure 3D.

As shown in Plot C, the signal level on the select state/complement line 16 changes from "0" to "1" between the occurence of the two latch enable pulses in plot F. The exact timing of this change of state is not important provided that it occurs between the two latch enable pulses as shown in plot F. The level of the signal on line 16 must remain high until completion of the second latch enable pulse of the cycle and is then returned to the low level before the first latch enable pulse of the next cycle.

A predetermined period after the second set enable pulse of the cycle, the timing circuit 34 produces a latch enable pulse on line 22 as shown in

plot F. Since at this time the input on line 16 is high and the phase word command input on the address input lines 12 refers to the state to be set during this cycle the location addressed in the PROM will relate to the magnitude of the required complement pulse, and thus value will be stored in the latch.

Prior to the end of the cycle and after completion of the second latch enable pulse, the timing circuit 34 controls the line 16 to return to the low level so that the next phase command word input on lines 12 to the PROM will identify the data stored in the state location. If the phase word is to be changed for the next cycle, this change will take place before completion of the cycle and the receipt of the next strobe pulse on line 36.

Since the phase shifter described is a latching phase shifter, the phase shifting state set by the previously described cycle will be maintained until a further signal is applied to one or other of the latching wires 4, 6. Therefore the time intervals indicated in Figure 4 should not be considered as limiting. In fact, the sequence of a complementary setting pulse, a resetting pulse and a setting pulse will occur in rapid succession and there may be a relatively long interval before the next sequence of pulses. The start of each cycle is determined by the input on the strobe line 36. This may be a regular periodic signal in which case the phase shifter will be periodically set to magnetisation level corresponding to the phase command word on input lines 12. If this phase command word has not changed between cycles then the same complementary and setting pulses will be used since the same address locations in the PROM will be being addressed. This repeated cycling strategy has been necessary in prior art phase shifters because of the inaccuracy of the achievement of the magnetisation setting during the initial cycles after a change in the phase command word. If greater accuracy can be achieved, it may not be necessary to repeat the cyclical operation until the phase command word changes.

Figure 5 illustrates the difference in the switching sequence proposed for use in the present invention and a prior art switching sequence in which only a single reset is provided. The plot of Figure 5 illustrates the phase shift achieved on the ordinate relative to the phase shift produced when the ferrite is in the M_{RS} magnetisation state, versus time on the abscissa. The prior art switching system is shown in solid lines. In this switching system a setting pulse to produce the phase shift B is initially applied. This phase shift B is maintained until the reset pulse is applied shortly before the next B setting pulse. When the phase command word changes to a required phase shift of A, it will be noted in the solid line curves that the first phase shift produced is considerably less than A. After each subsequent reset pulse, the phase shift produced converges closer to A. Again when the phase command word returns to B, the initial phase shift produced is greater than B and again converges to the value B after several cycles.

As shown by the dotted lines in Figure 5, a complementary set pulse is applied just before the reset. This brings the phase shift produced up to a constant value since the magnetisation achieved is always a fixed value M_X. This results in the ferrite always cycling around the same outer hysteresis loop even though at some point on the hysteresis loop the switching circuit allows the magnetisation to fall back to a value corresponding to the commanded phase shift. In an alternative embodiment of the switching circuit the selected unsaturated magnetisation state depends on the previous set state so as to minimise the error in the next set state.

It will be appreciated that the PROM must store two values, a state value and a complement value for each possible phase command word. In the simplest embodiment, the complement value is selected so that the magnitude of the voltage pulse produced by the state value and the magnitude of the voltage pulse produced by the complement value add up to a constant amount. Ideally, however, the two values to be stored in the PROM are selected on an emplrical basis so that the next following state whatever its value is accurately achieved.

The pairs of values can be experimentally determined by coupling the phase shifter to a device which displays the actual phase shift produced versus time on a CRT display. A display similar to that shown in Figure 5 will be produced.

For each possible phase command word, a complementary value is initially selected on the basis that the state and complementary value voltages should add up to a constant amount equivalent to a fixed unsaturated magnetisation state. The phase shifter is then switched from the state under consideration to various different other states. The accuracy of each following state is determined and the following state which is least accurate is selected for adjustment of the complementary value. The ferrite phase shifter is then repeatedly switched between the state under consideration and the "worst case" following state with different values of the complementary pulse voltage until the optimum results are achieved. It is found that by adjusting the complementary set pulse voltages for the worst case, the accuracy of other following states is not significantly reduced and is generally increased.

Figure 6A shows the voltage pulses applied to a latching wire of a phase shifter used in a waveguide which is intended to be used in transmit and receive modes. Since the propagation direction is reversed when the waveguide is switched between transmit and receive modes, an amplifier connected to the latching wire can be selectively connected either to a positive or negative voltage signal in order to drive the phase shifter to produce phase shifts in opposite senses. It will be appreciated that during the transmit and receive mode during one cycle of, say, a radar system, the magnitude of the phase shift required is identical. However, if the frequency used changes between each cycle, it is necessary then to change the magnitude of the phase shift produced in the waveguide.

Figure 6A shows a switching sequence as used in a prior art latching phase shifter for operation in transmit and receive modes. During each cycle the phase shifter is initially fully reset by application of a

maximum negative voltage pulse to a latching wire. This resetting pulse 50 is then followed by a setting pulse 52 of positive voltage of a magnitude to produce the required phase shift for the following transmission mode operation. At the end of the transmission mode a full setting pulse 54 of maximum positive voltage is applied by the switching circuit before the setting pulse 54, which has the same magnitude but opposite sign to the pulse 52, is applied in order to produce a phase shift of the same magnitude but opposite sense during the following reception mode. The cycle is then repeated with the magnitude of the next setting pulse 58 being determined by the then transmitted frequency. It will be appreciated that such a switching sequence, which requires two maximum voltage pulses during each cycle requires considerable power consumption.

The switching sequence according to an embodiment of the invention is illustrated in Figure 6B. During one cycle of operation, a setting pulse 60 is applied to a latching wire of the phase shifter in order to produce the required phase shift for the following transmission mode. At the end of the tranmission mode a voltage pulse 62, which has a magnitude complementary to the setting voltage pulse 60, is applied. The complementary voltage can be determined in any of the ways previously described. In order to switch to the receive mode, a setting pulse 64 of the same magnitude but opposite sense is applied to the latching wire. It has been found unnecessary to apply a full resetting pulse, as described in the previous embodiment, when the phase shifter is operating in this symmetrical fashion. At the end of the reception mode, a complementary voltage pulse 66 is applied to the latching wire. The magnitude of the complementary voltage pulses 62 and 66 will normally be identical although the voltages applied are of opposite sense. After application of the complementary voltage pulse 66, a new setting voltage pulse 68 is applied to produce the required phase shift for the transmit mode of the next cycle.

Since there is no saturation of the phase shifter during the operating cycles, it is necessary to ensure that the phase shifter locks into its major hysteresis loop by applying a simple sequence of maximum magnitude voltage pulses as indicated at 70, on initially switching on the phase shifter.

In order to produce a switching sequence of Figure 6B, a switching circuit similar to that illustrated in Figure 2 may be employed. However, the resetting amplifier 10 and its associated latching wire 6 are no longer required. For each cycle of operation only one phase command word is required since the magnitude of the voltage pulses 60 and 64 is identical as is the magnitude of the complementary voltage pulses 62 and 66. However, the amplifier 8 must be provided with means for selectively providing it with a positive or negative voltage input under the control of the timing circuit 34. For example an inverter may be connected between the digital to analogue converter 26 and the input to the amplifier 8 in the receive mode only.

Although the present embodiment refers to a toroidal ferrite phase shifter, it is equally applicable to phase shifters using other magnetic materials such as garnet and of various shapes provided that a closed magnetic flux path is defined.

Claims

1. A latching phase shifter (2) comprising a magnetic material defining a closed magnetic flux path, magnetising means (4, 6) associated with the magnetic material (2) for applying a magnetising field thereto, and a switching circuit (34, 8, 10, 14, 20, 26) connected to said magnetising means (4, 6) characterised in that the switching circuit comprises means (34, 8, 14, 20, 26) for controllably switching the magnetic material (2) from a previously set magnetisation state to a selected, unsaturated magnetisation state, and means (34, 8, 14, 20, 26) for then switching the magnetic material to a desired new magnetisation state.

2. A latching phase shifter according to claim 1, characterised in that the switching circuit further comprises means (10, 34) for switching the magnetic material (2) to a saturated magnetic state after it has been set to an unsaturated magnetic state and before setting to the desired new magnetisation state.

3. A latching phase shifter according to claim 1 or 2, characterised in that the means for switching to the unsaturated magnetisation state, and for switching to the desired new magnetisation state comprise means (34, 20, 26, 8) for applying voltage pulses of a predetermined duration to said magnetising means (4).

4. A latching phase shifter according to claim 3, characterised in that the magnitude of a voltage pulse for switching to the selected, unsaturated state is determined such that the sum of the magnitude of this voltage and the magnitude of the voltage for producing the previously set magnetisation state add up to a predetermined value.

5. A latching phase shifter according to claim 4, characterised in that the predetermined value is a function of the previously set state.

6. A latching phase shifter according to claim 3, characterised in that the voltage pulse required for switching to the selected, unsaturated magnetisation state is determined by reference to either or both of the previously set magnetisation state and the desired new magnetisation state in order to minimise the phase error in switching therebetween.

7. A switching circuit for driving a latching phase shifter comprising amplifier means (8) for applying voltage pulses of predetermined duration to a latching wire (4) of the phase shifter, a memory device (14) for storing data relating to the magnitude of a voltage pulse required to produce each particular magnetisation state, and the magnitude of a complementary voltage pulse required to produce a subsequent un-

saturated magnetisation state, means (26) connected to an output of said memory means (14) to convert output data into a signal for application to said amplifier means to produce the required voltage pulse, input means (12) connected to said memory device (14) for selecting the required data, and control means (34) connected to said memory means (14) in order to control the output of data therefrom in response to the input (12).

8. A switching circuit according to claim 7, further comprising resetting amplifier means (10) under the control of said control means (34) for selectively applying a resetting pulse to a latching wire (6) of the phase shifter (2).

9. A switching circuit according to claim 7 or 8, wherein the control means (34) comprises means for selectively providing the amplifier means with a positive or negative voltage input in dependence upon whether the phase shifter is to be operable in a transmit or receive mode.

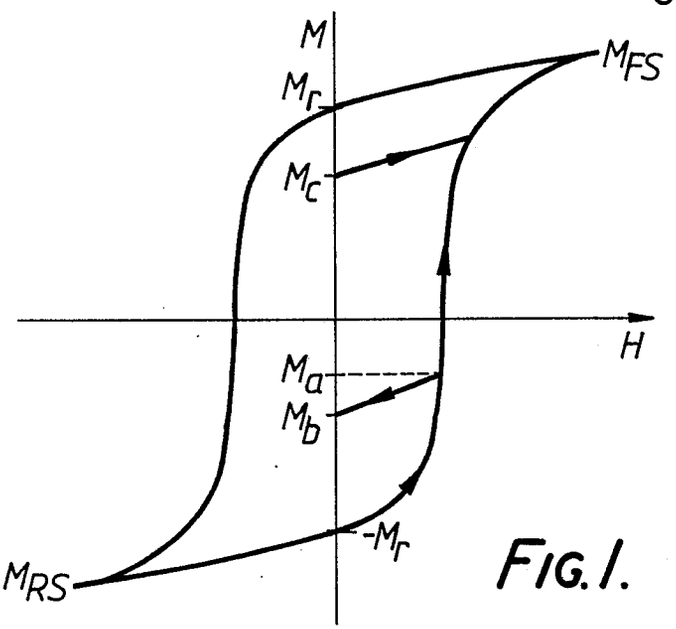

FIG. 1.

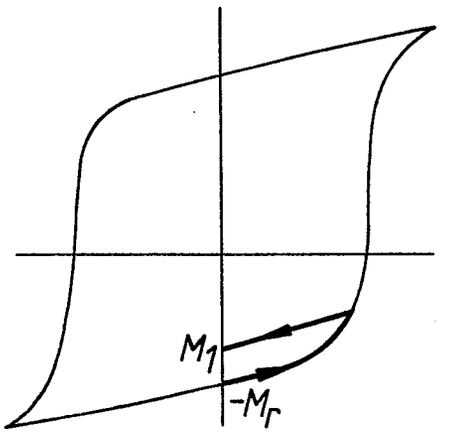

FIG. 3A.

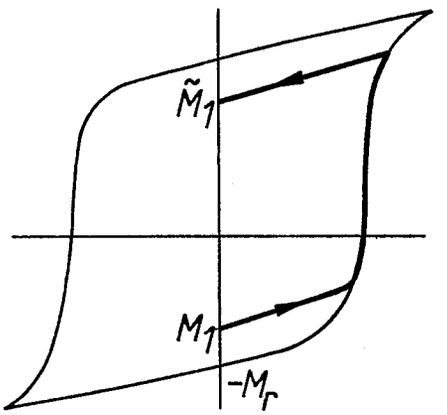

FIG. 3B.

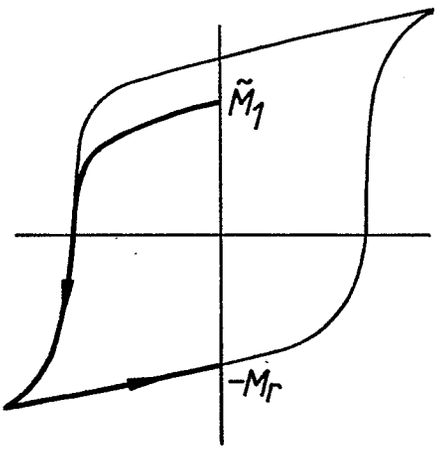

FIG. 3C.

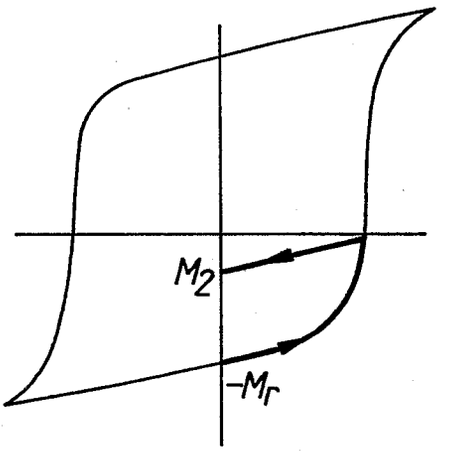

FIG. 3D.

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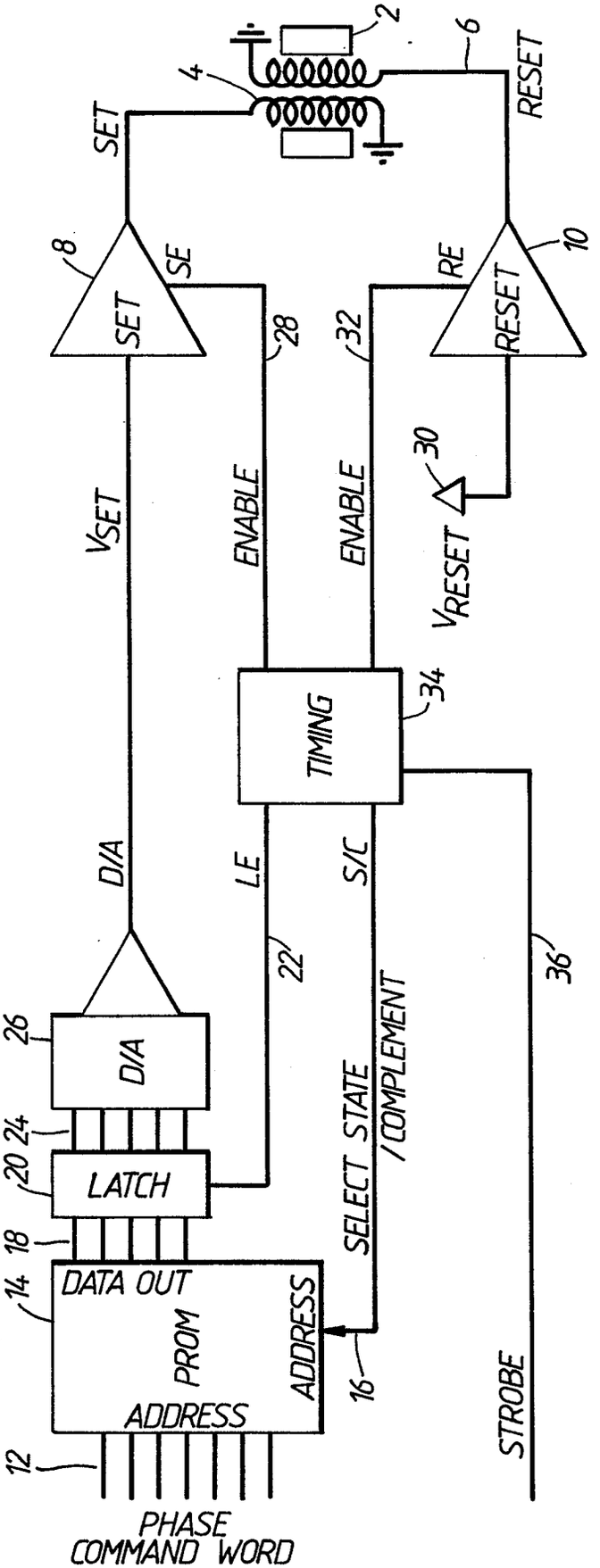
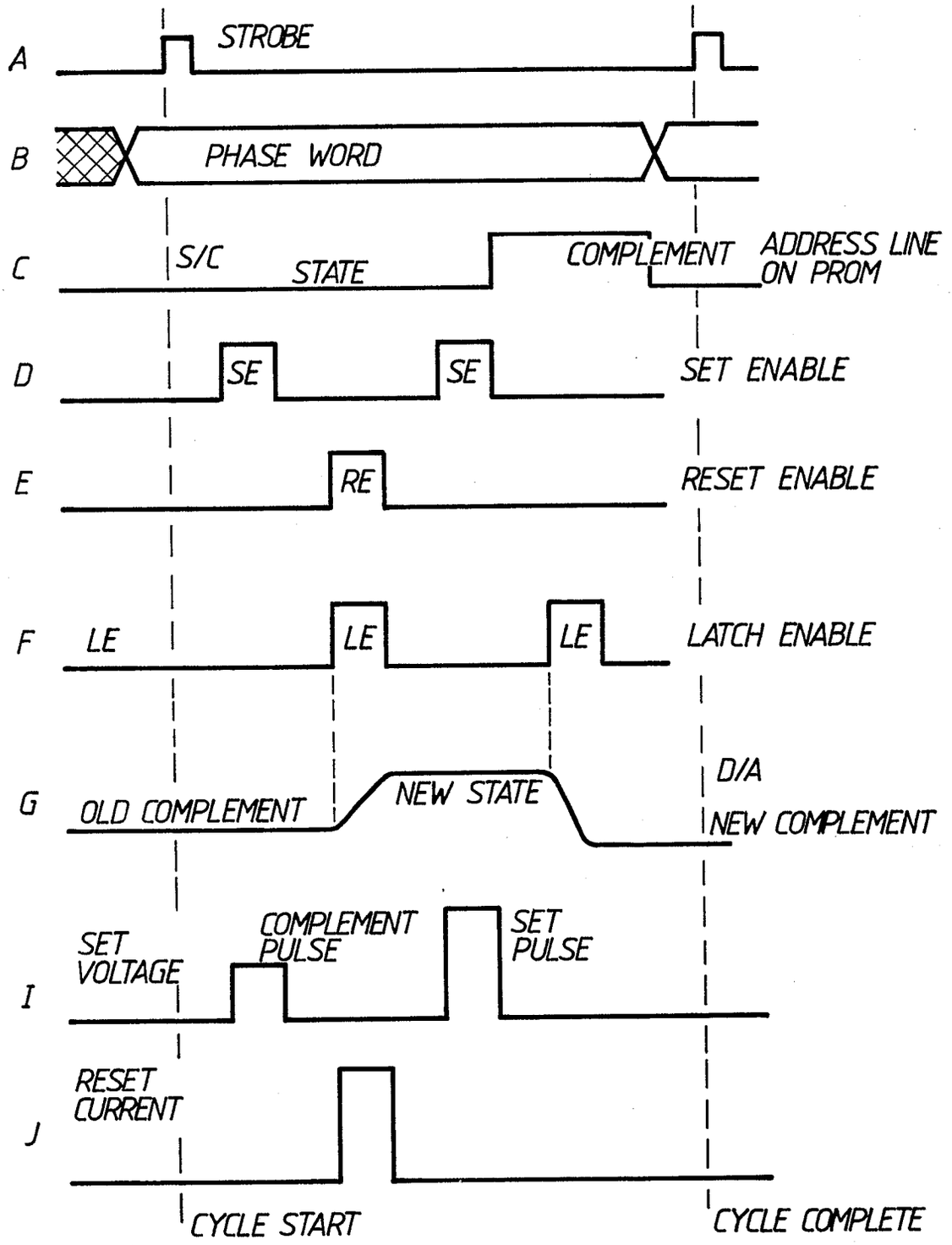


FIG. 2.


A
STROBE
B
PHASE WORD
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S/C STATE
COMPLEMENT ADDRESS LINE ON PROM
D
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SE
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LATCH ENABLE
G
OLD COMPLEMENT
NEW STATE
D/A
NEW COMPLEMENT
I
SET VOLTAGE
COMPLEMENT PULSE
SET PULSE
J
RESET CURRENT
CYCLE START
CYCLE COMPLETE

FIG. 4.

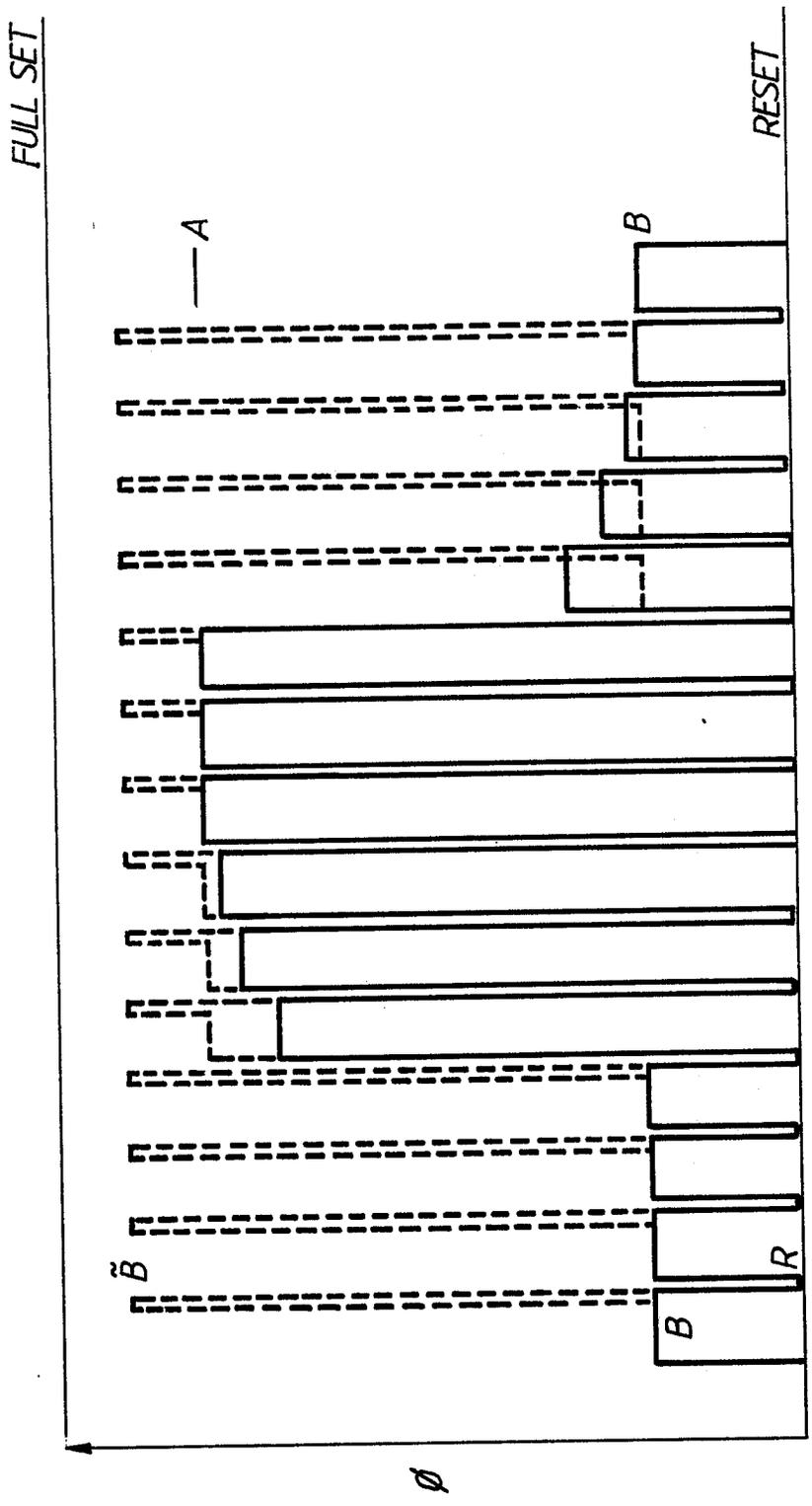

FIG. 5.

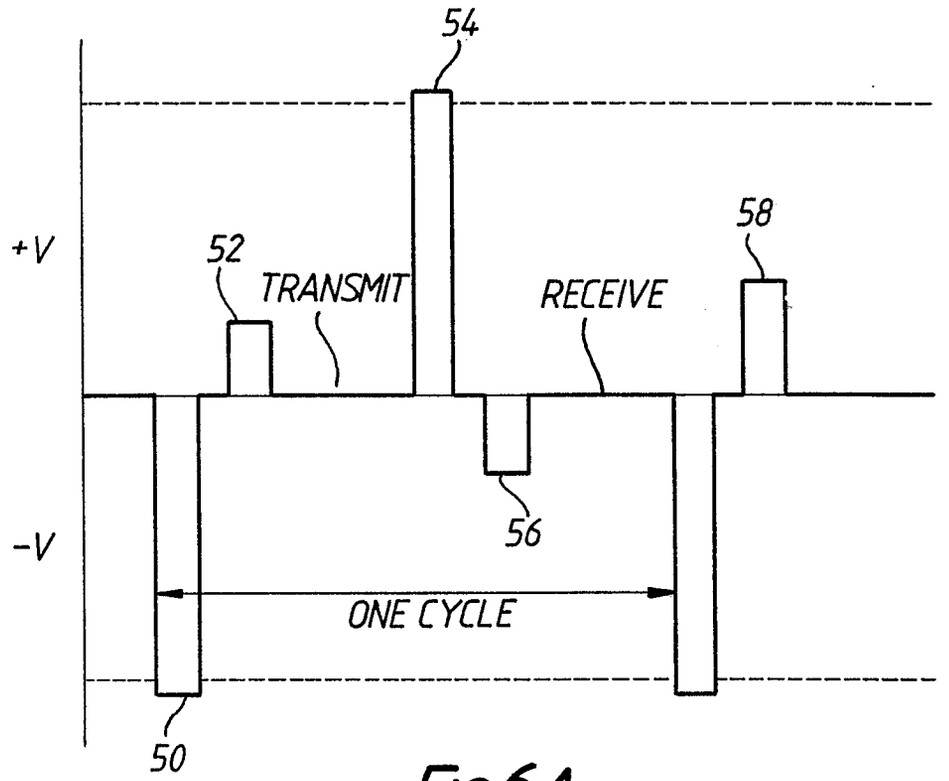
54
+V
52
TRANSMIT
RECEIVE
58
56
-V
ONE CYCLE
50

FIG.6A.

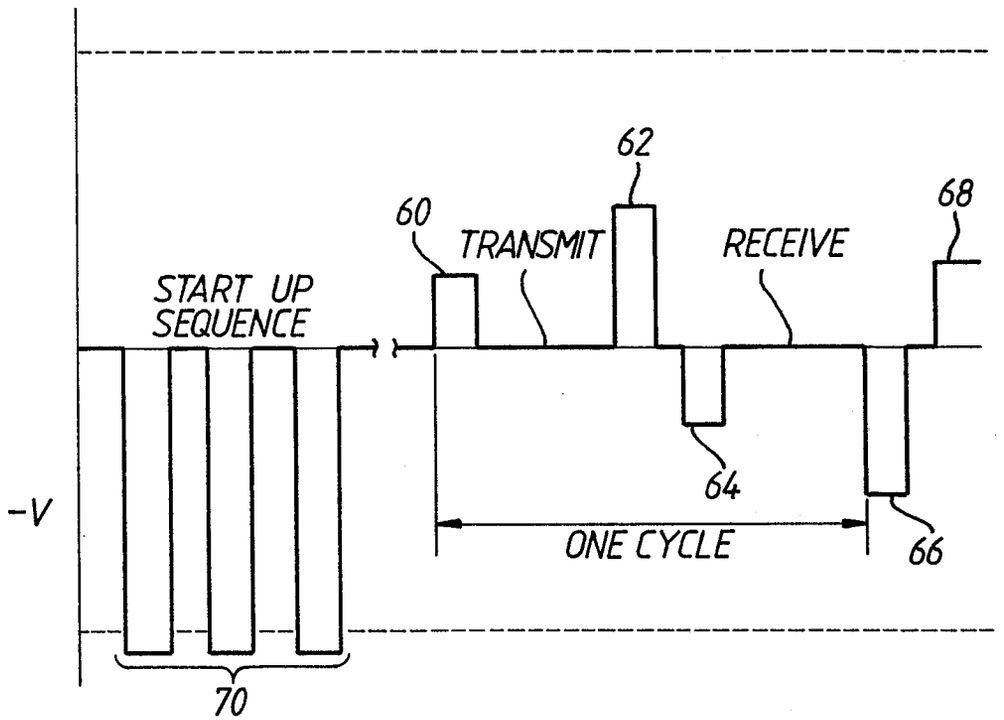
62
60
TRANSMIT
RECEIVE
68
START UP
SEQUENCE
64
-V
ONE CYCLE
66
70

FIG.6B.