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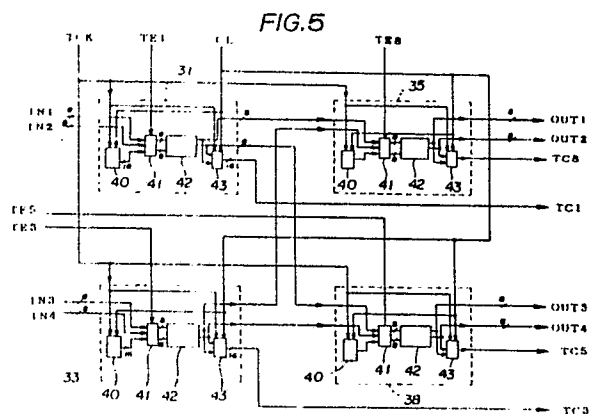
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54 **Semiconductor integrated circuit with a test function.**

57 A semiconductor integrated circuit comprises a plurality of integrated circuit blocks (31 - 39) constituted on a wafer (30), the integrated circuit blocks being arbitrarily electrically connected to each other so as to form a system. Each of the integrated circuit blocks comprises a logical operating circuit (42) for carrying out a logical operation; a pseudo-random pattern generating circuit (40) for generating a pseudo-random pattern signal; switching circuit (41) for selecting either an input signal to be processed by the logical operating circuit or the pseudo-random pattern signal in response to a test enabling signal (TE1 - TE9) which is independently applied to each integrated circuit block so that each integrated circuit block is independently set to either a test mode or a normal mode and for outputting the selected signal to the logical operating circuit; and a data compressing circuit (43) for compressing an output data signal of the logical operating circuit.



EP 0 273 821 A3



DOCUMENTS CONSIDERED TO BE RELEVANT					
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)		
Y	ELECTRONIC DESIGN, vol. 33, no. 16, 11th July 1985, pages 63-64, Schiphol, NL; M. BEEDIE: "Testing, fault tolerance emerge as top issues at wafer-scale conference" * Page 63, column 1, last paragraph - column 2; page 64, column 2, lines 39-46 *	1,3,4	G 01 R 31/28		
A	--- * Page 63, column 3, lines 28-40 *	6			
Y	AUTOTESTCON'80-1980 AUTOTEST CONFERENCE, Washington, 2nd-5th November 1980, pages 135-139, IEEE, New York, US; D.K. BHAVSAR; "Self-testing supercells" * Page 138, paragraph "Polynomial division (POLYDIV) Scheme" *	1,3,4			
A	--- * Page 138, point "FSR" *	7			
P,X	PROCEEDINGS OF THE IEEE 1987 CUSTOM INTEGRATED CIRCUITS CONFERENCE, Portland, 4th-7th May 1987, pages 207-210, IEEE, New York, US; K. YAMASHITA et al.: "A wafer-scale 170,000-gate FFT processor with built-in test circuits" * Whole article *	1-7	TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 06 F 11/26 G 01 R 31/28 G 06 F 11/20		
The present search report has been drawn up for all claims					
Place of search THE HAGUE		Date of completion of the search 12-12-1989	Examiner SARASUA GARCIA L.		
<table><tr><td>CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</td><td>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</td></tr></table>				CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document	T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document
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