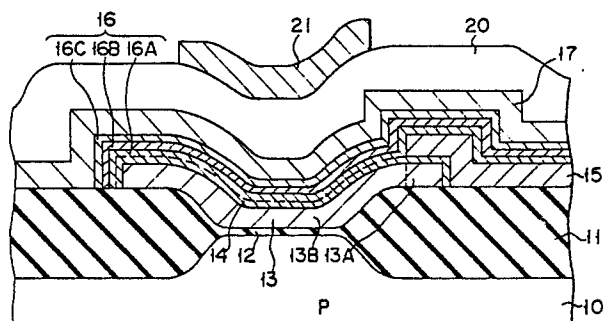# EUROPEAN PATENT APPLICATION

(71) Applicant: **Kabushiki Kaisha Toshiba**
72, Horikawa-cho Saiwai-ku
Kawasaki-shi(JP)

(72) Inventor: **Tanaka, Shinichi c/o Patent Division**
K.K. Toshiba 1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)
Inventor: **Hori, Masayuki c/o Patent Division**
K.K. Toshiba 1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)
Inventor: **Kanebako, Kazunori c/o Patent**
Division
K.K. Toshiba 1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)
Inventor: **Tozawa, Noriyoshi c/o Patent**
Division
K.K. Toshiba 1-1 Shibaura 1-chome
Minato-ku Tokyo 105(JP)

(74) Representative: **Lehn, Werner, Dipl.-Ing. et al**
Hoffmann, Eitle & Partner Patentanwälte
Arabellastrasse 4
D-8000 München 81(DE)

(54) Semiconductor memory device.

(57) Disclosed is a semiconductor memory device containing a number of memory cells each having a floating gate (13), an erase gate (15), and a control gate (17). In a data erasure mode, electrons are discharged from the floating gate (13) into the erase gate (15). In the semiconductor memory device, an impurity concentration in at least a region of the floating gate (13) overlapping with the erase gate (15) is lower than that of the erase gate (15).

FIG. 4

Semiconductor memory device

This invention relates to a semiconductor memory device into which data can be electrically written and in which data can be electrically erased. In particular, this invention relates to a semiconductor memory device wherein the data stored in all memory cells can be erased simultaneously.

A flash type electrical erasable programmable read only memory (FE²PROM) with a function to electrically erase all of the stored bits in a simultaneous manner is known as disclosed in USP Nos. 4,437,172 and 4,466,081. The FE²PROM as disclosed in these patents allows the stored data to be electrically and simultaneously erased on all of the bit lines. With this advantageous feature, the FE²PROM has progressively superseded the UV type EPROM in which the data stored therein is erased by ultraviolet rays.

An example of one of the memory cells constituting the FE²PROM is illustrated in cross sectional form in Fig. 1.

In Fig. 1, showing the structure of the conventional memory cell, reference numeral 30 designates a p-type semiconductor substrate. Field oxide film 31 is layered on substrate 30, and erase gate 32, acting as a first polysilicon layer, is partially layered on field oxidation film 31. Reference numeral 33 indicates a gate oxide film. Floating gate 34 is layered on gate oxide film 33, and consists of a second polysilicon layer. The end portion of floating gate 34 is overlaid on the end portion of erase gate 32, with silicon oxide film 35 interlayered between them. Silicon oxide film 35 serves as an insulating film and is formed by oxidizing erase gate 32. Control gate 37, which serves as a third polysilicon layer, is layered over ffloating gate 34, with silicon oxide film 36 interlayered between them. Silicon oxide film 36 serves as an insulating film and is formed by oxidizing floating gate 34. Although not shown, source and drain regions as N type diffusion layers are provided on substrate 30, and located at sides of floating gate 34, respectively. An interlayer insulating film (not shown) is layered on control gate 37, and has contact holes opened to the source and drain regions, and the surfaces of erase gate 32 and control gate 37. Within each contact hole is formed a lead electrode made of aluminum.

The data write operation of the FE²PROM with the memory cells thus structured is similar to that of the conventional EPROM. Specifically, a high voltage is applied to the drain region (not shown) of the memory cell, and control gate 37. The applied high voltage causes hot electrons in the channel region located under floating gate 34. The generated hot electrons are injected into the floating gate 34 as set at a predetermined potential, because the high voltage has been applied to control gate 37. The injection of electrons into floating gate 34 increases the threshold voltage in the channel region.

In an erasure mode, for erasing the data, a high voltage is applied to erase gate 32, to place the silicon oxide film 35 between erase gate 32 and floating gate 34 in a high electric field. Under this condition, the electrons which have been already injected into floating gate 34, are discharged into erase gate 32. As the result of this discharge, the threshold voltage in the channel region decreases, and the data is erased.

In a read mode for reading out the data, a fixed voltage is applied to the drain region and control gate 37. Under this condition, the memory cells into which the data have been written and whose channel regions have increased threshold voltage, are in an off state. Those memory cells whose data have erased and channel region have decreased threshold voltage, are in an on state. The on-and off-states are read out in the form of logical "1" and "0" of the data, respectively.

In the memory cell as mentioned above, for the data erasure, electrons are discharged through silicon oxide film 35 to erase gate 32, from floating gate 34. Therefore, the erasure characteristic of this cell depends on the quality and thickness of silicon oxide film 35, and the shapes of floating gate 34 and erase gate 32, which are separated by silicon oxide film 35. To quicken the erasure operation, for example, the thickness of silicon oxide film 35 is thin, an insulation of silicon oxide film 35 is reduced by appropriately selecting a way of process for erase gate 32 and a method of forming silicon oxide film 35. However, it is very difficult to appropriately select the process and formation. If the selection is inappropriate, the data write and erasure may be performed erroneously or more adversely silicon oxide film 35 may be electrically broken down. Thus, great care must be used for such selection.

In FE²PROM, the cause for the erroneous data write has been known and will be described. In the write mode, a high voltage is applied to control gate 37 and the drain. The same substrate further contains other memory cells which are not in the write mode, but whose control gates 37 are applied with the same high voltage. In those other memory cells, the potential at floating gate 34 is pulled to a high potential level, so that an electric field is developed between floating gate 34 and erase gate 32. It has been known that an irregularity, called

asperity, is inevitably formed on the upper surface of a polysilicon layer. The leak current flowing from the first polysilicon layer having a surface of small asperity to the second polysilicon layer having a surface of great asperity is larger than the leak current flowing from the second polysilicon layer to the first polysilicon layer. In other words, more electrons move from the second to the first poly-silicon layer than the first to the second polysilicon layer. In the case of the Fig. 1 memory cell, the asperity on the upper surface of erase gate 32 is larger than that on the lower surface of floating gate 34. Therefore, electrons may be injected into floating gate 34, through silicon oxide film 35 exist-ing between erase gate 32 and floating gate 34. In this way, the erroneous data write is caused by injecting electrons into the floating gates of those memory cells which are not in the write mode.

An ideal characteristic required for the insulat-ing films used in the memory cells in FE²PROM is that the leak current easily flows in the erasure direction. but hardly flows in the opposite direction, i.e., the write direction. In this respect, the electrical characteristic of the conventional memory cell shown in Fig. 1 is not always satisfactory.

To cope with this, the memory cell as shown in sectional form in Fig. 2 has been proposed. In this memory cell, the first polysilicon layer constitutes floating gate 34. A second polysilicon layer forms an erase gate 32. Insulating film 38 existing be-tween between erase gate 32 and control gate 37 is formed by oxidizing the polysilicon of erase gate 32.

In the Fig. 2 prior art, one end portion of erase gate 32 is laid on the end portion of floating gate 34. Therefore, a relative large asperity is formed on the upper surface of floating gate 34. At this time, more electrons move from the lower surface of erase gate 32 having a surface of small asperity to the upper surface of floating gate 34 having a surface of great asperity than from the upper sur-face of floating gate 34 to the lower surface of erase gate 32. Therefore, in the memory cell of Fig. 2, the erroneous write operation is restricted and the erasure characteristic is improved.

In the Fig. 2 memory cell as well as the Fig. 1 memory cell, erase gate 32 and control gate 37 are used to conductive layer respectively. For the re-sistance reduction purpose, the polysilicon layers constituting the erase gate and the control gate are doped with impurity, for example, phosphorus atoms or arsenic atoms at $6 \times 10^{20}/cm^3$ or more of concentration, viz., at a concentration of the solu-tion limit. Similarly, the polysilicon layer forming floating gate 34 is doped with phosphorus atoms or arsenic atoms at a concentration of the solution limit. Therefore, a degree of asperity occurring on the upper surface of floating gate 34 is small. A

leak current caused between floating gate 34 and erase gate 32 in the erroneous write direction is nearly equal to that in the erasure direction. In this respect, the erroneous write characteristic and the erasure characteristic are both improved unsatis-factorily.

Accordingly, an object of this invention is to provide a semiconductor memory device with the improved erroneous write characteristic and era-sure characteristic.

According to this invention, there is provided a semiconductor memory device having a semicon-ductor substrate of a first conductivity type, a float-ing gate containing impurity at a predetermined concentration layered on a first insulating film which also is layered on the substrate, an erase gate above the floating gate, with a second insulat-ing film interlaid therebetween, a part of said erase gate overlapping with said floating gate, and said erase gate containing impurity at a predetermined concentration, and a control gate layered above said floating gate with a third insulating film inter-laid therebetween, wherein an impurity concentra-tion in at least the part of floating gate overlapping the erase gate is lower than that of the erase gate.

Other objects and advantages of this invention will become apparent from the following description when take in connection with the drawings in which:

Fig. 1 is a sectional view of a memory cell used in a conventional memory device:

Fig. 2 is a sectional view of another memory cell used in a conventional memory device;

Fig. 3 is a plan view of a group of memory cells used in a semiconductor memory device ac-cording to this invention;

Fig. 4 is a sectional view taken on line I - I' in Fig. 3;

Fig. 5 is a graph showing a variation of the leak current vs. applied voltage of the semiconduc-tor memory device according to this invention;

Fig. 6 is a graph showing a variation of the leak current vs. impurity concentration of the semi-conductor memory device according to this inven-tion;

Fig. 7 is a sectional view showing a structure of a memory cell used for a semiconductor mem-ory device according to this invention, the structure of the memory cell being in one of the steps to manufacture the memory cells; and

Fig. 8 is a sectional view showing another structure of a memory cell used for a semiconduc-tor memory device according to this invention, the structure of the memory cell being in one of the steps to manufacture the memory cells.

A preferred embodiment of a semiconductor memory device according to this invention will be described referring to Figs. 3 and 4. A group of

memory cells used for a semiconductor memory device according to this invention is shown in Fig. 3. A cross section of the memory cell taken on line I - I' is shown in Fig. 4. In the figure, reference numeral 10 designates a silicon semiconductor substrate of p-type. Field oxide film 11 for separating the adjacent memory cells from one another is formed on substrate 10. Gate oxide film 12 is formed on a specific location of substrate 10 which correspond to a channel region in the element region as separated by field oxide film 11. Floating gate 13 as a first polysilicon layer is formed on gate oxide film 12. Both ends of floating gate 13 extend over field oxide film 11.

Erase gate 15 as a second polysilicon layer is laid above one end of floating gate 13 with silicon oxide film 14 interlaid therebetween. Silicon oxide film 14 serves as an insulating film and is formed by oxidizing the polysilicon layer of floating gate 13. Erase gate 15 overlaps with the end portions of floating gate 13 of two adjacent memory cells as viewed horizontally in Fig. 3. Three-layered 16 is layered over floating gate 13 and erase gate 15. Control gate 17 consisting of a third polysilicon layer is continuously layered over the three layered film 16. Three-layered film 16 consists of first silicon oxide (SiO_2) film 16A as a bottom layer, second silicon nitride (Si_3N_4) film 16B as a medium layer, and a third silicon oxide (SiO_2) film 1^{6}C as a top layer. Source region 18 and drain region 19 as n-type diffusion layers are formed on the element region surfaces located at both sides of floating gate 13, respectively. Source region 18 is a single layer and used in common for all of the memory cells. Interlaying insulating film 20 is laid on control gate 17. Conductive layer 21 made of aluminum, for example, is formed on interlaying insulating film 20. Conductive layer 21 is connected to the drain region 19 of each memory cell, through contact hole 22. Erase gate 15 and control gate 17 are incorporated in each memory cell, and these are used as interconnection layers. For this reason, the polysilicon layers of the erase gate 15 and control gate 17 are doped with impurity, for example, phosphorus atoms or arsenic atoms at 6×10^{20}/cm^3 or more, i.e., a concentration equal or approximate to the solution limit. The same type of impurity is also doped into the first layer polysilicon layer of floating gate 13. The same type of impurity is doped into the region 13A of floating gate 13 laid under erase gate 15. In this case, the impurity concentration is much lower than that for erase gate 15 and control gate 17, and less than 6×10^{20}/cm^3 for example, in a range from 1×10^{20}/cm^3 to 4×10^{20}/cm^3. The region 13B of floating gate 13 not overlapping with erase gate 15 is doped with the same type of impurity at the same concentration as that of erase gate 15 and control gate erase

17, i.e., 6×10^{20} cm^3.

Silicon oxide film 14 laid over floating gate 13 is formed by oxidizing the polysilicon layer of floating gate 13. The polysilicon layer satisfactorily doped with impurity at the concentration on the level of the solution limit is then oxidized, so that the asperity appearing on the surface is remarkably lessened. When the impurity concentration is less than 6×10^{20}/cm^3, the asperity rapidly increases on the surface of the polysilicon layer, after it is subjected to the subsequent oxidization process. It is estimated that the rapid increase of asperity is due to the fact that since the impurity concentration of the polysilicon layer is not uniform in the layer, the oxidization rate is not constant over the surface of the polysilicon layer.

For this reason, the asperity on the surface of the region 13A of floating gate 13 overlapping with erase gate 15 increase. Therefore, a concentration of an electric field occurs in the region 13A. In this region 13A, a accelerated electric field make it easy to generate the leak current between floating gate 13 and erase gate 15. The electric field is weaker than that in the flat area of region 13B. Thus, in the memory cell according to this invention, the leak current flows from floating gate 13 to erase gate 15 increases. In other words, when considering the electrons action, the electrons flow is enhanced in the direction from floating gate 13 toward erase gate 15, resulting in improvement of the erasure characteristic of the memory device.

The leak current flowing from floating gate 13 toward erase gate is not increased, while electrons flow in this direction is impeded. Therefore, the erroneous write operation is hard to occur.

A graph of Fig. 5 comparatively shows leak current characteristics between the floating gate and the erase gate of the conventional memory cell and the memory cell of this embodiment. In the graph, the abscissa represents a voltage $V_{FE}(V)$ between the floating gate and the erase gate, and the ordinate a leak current (A).

Curves "a", "b" and "c" indicate variations of the leak current when a voltage V_{FE} is applied to those gates, with its positive polarity at the erase gate. These curves "a", "b" and "c" are for the impurity (phosphorus) concentrations of the region 13A, 6×10^{20}/cm^3, 4×10^{20} cm^3, and 2×10^{20}/cm^3, respectively. Further, curve "a" is the leak current variation of the conventional memory cell. Curves "b" and "c" show the leak current variation of the memory cells according to this embodiment. Curves ①, ②, and ③ indicate variations of the leak current when a voltage V_{FE} is applied to those gates, with its positive polarity at the floating gate. These curves ①, ② and ③ are for the impurity (phosphorus) concentrations of the region 13A, 6×10^{20}/cm^3, 4×10^{20} cm^3, and 2×10^{20}/cm^3, respec-

tively. Further, curve ① is the leak current variation of the conventional memory cell. Curves ② and ③ show the leak current variation of the memory cells according to this embodiment.

As seen from the graph, as the impurity concentration of region 13A, the leak current flowing from the erase gate to the floating gate becomes large. The leak current in this direction contributes to the discharge of electrons from the floating gate to the erase gate. As a result, the erasure characteristic can be improved by reducing the impurity concentration in the region 13A. The leak current flowing from the floating gate to the erase gate increases a little, while electrons move in this direction is impeded. This directional leak current contributes to the erroneous write operation in which electrons are injected into the floating gate. Thus, the increase of the leak current is small, and hence the occurrence of the erroneous write operation is limited. It is confirmed that in actual FE²PROM memory cells, as the impurity concentration of the floating gate decreases, a rate of erroneous write occurrences (operations) decreases. This is because since the erasure characteristic of each cell is improved due to the low impurity concentration of the floating gate, many holes are in the floating gate, neutralize if less electrons than the holes are injected in to floating gate, the gate remains positively charged.

Fig. 6 shows characteristic curves, which describe variations of the leak current between the floating gate and the erase gate. The abscissa of the graph represents a concentration (/cm³) of impurity (phosphorus) in the region 13A of floating gate 13. The ordinate represents a leak current (A). In the graph, characteristic curve I indicates a variation of a leak current flowing from erase gate 15 to floating gate 13, when a voltage of 25 V is applied to between erase gate 15 and floating gate 13. In this case, erase gate 15 is set at the positive polarity of the applied voltage. This curve shows that the leak current increases with reduction of the impurity concentration of the region 13A of floating gate 13. The increased leak current provides an improved erasure characteristic.

Characteristic curve II indicates a variation of a leak current flowing from floating gate 13 to erase gate 15, when a voltage of 25 V is applied to between floating gate 13 and erase gate 15. In this case, floating gate 13 is set at the positive polarity of the applied voltage. This curve II shows that the leak current increases a little when the impurity concentration in the region 13A is decreased.

These curves also show that in the vicinity of 6×10^{20}/cm³ of impurity concentration, a difference between the leak currents flowing from floating gate 13 to erase gate 15 and from erase gate 15 to floating gate 13 is small. It is known that when the current difference is below a value of 2 digits or less, the erasure characteristic and production yield are deteriorated. Therefore, if the impurity concentration is set in the range from 4×10^{20}/cm³ to 2×10^{20} cm³, the current difference is satisfactorily large, and the memory device is free from the problem of the erasure characteristic and production yield.

Description to follow is for a method of manufacturing the memory cells functioning as described above. To begin with, filed oxide film 11 is formed on substrate 10. the first polysilicon layer is deposited thereon. Appropriate impurity such as phosphorus or arsenic are diffused into the polysilicon layer. The first polysilicon layer is patterned by reactive ion etching process (RIE), to form floating gate 13. The structure is thermally oxidized in a condition that it is placed at 1000°C and for 30 minutes in gas containing O_2 and N_2 or O_2 and Ar with the proportion of 2 to 8. As the result of this thermal oxidization, silicon oxide film 14, 350 Angstroms thick, is formed on the surface of floating gate 13. A second polysilicon layer is deposited over the surface of the structure. Phosphorus or arsenic impurity at 6×10^{20} cm³ is diffused into the second polysilicon layer. Then, the second polysilicon layer is patterned by chemical dry etching (CDE) process, to form erase gate 15. The structure is thermally oxidized in a condition that it is placed at 1000°C and for 30 minutes in gas containing O_2 and N_2 or O_2 and Ar with the proportion of 5 to 5. As the result of this thermal oxidization, silicon oxide film 16A, 400 Angstroms thick, is formed over floating gate 13 and erase gate 15. Silicon nitride film 16B of 150 Angstroms in thickness is then formed over silicon oxide film 16A by chemical vapor deposition (CVD) process at 700°C and for 20 minutes. The structure is placed in a wet atmosphere and thermally oxidized at 1000°C and for 50 minutes, to form silicon oxide film 1⁶C of 50 Angstroms in thickness on the surface of silicon nitride film 16B. A third polysilicon layer is deposited and doped with phosphorus or arsenic impurity at 6×10^{20}/cm³ or more, and then is patterned, to form control gate 17.

The process steps to reduce the impurity concentration in the region 13A of floating gate 13 follows. Reference is made to Fig. 7 for this description. Following the steps to form field oxide film 11 and gate oxide film 12, the first polysilicon layer is deposited over the entire surface of the structure. Then, the first polysilicon layer is patterned to form floating gate 13. Subsequently, the portion to be used as region 13A is selectively covered with ion implanting mask 23 made of photo register, for example. Phosphorus or arsenic ions are implanted into floating gate 13 at a predetermined acceleration voltage and a predeter-

mined dosage, by ion implantation process.

After removal of mask 23, phosphorus or arsenic ions are implanted into floating gate 13, again (see Fig. 8). Before this second ion implantation, the acceleration voltage and dosage must be selected so that the impurity concentration of region 13A is in a range from $1 \times 10^{20}/cm^3$ to $4 \times 10^{20}/cm^3$, and that in region 13B is $6 \times 10^{20}/cm^3$ or more. In this way, the concentration in the region 13A of floating gate 13 is set within the range from $1 \times 10^{20}\,cm^3$ to $4 \times 10^{20}\,cm^3$, and that in region 13B is $6 \times 10^{20}\,cm^3$ or more.

A second embodiment of a semiconductor memory device according to this invention will be described. In the second embodiment, the impurity concentration in the region 13A of floating gate 13 of each memory cell is set to be equal to that in region 13B. The exact value of the concentration is $1 \times 10^{20}/cm^3$ to $4 \times 10^{20}/cm^3$, which is lower than $6 \times 10^{20}/cm^3$ of erase gate 15. This embodiment also attains the impurity concentration relationships of the region 13B of floating gate 13 and erase gate 15, which is comparable with that of the first embodiment. Therefore, the satisfactory improvement of the erasure characteristic and production yield can be expected.

In this embodiment, there is a danger that the leak current flowing from control gate 18 toward floating gate 13 increases, to deteriorate the electron holding characteristic of floating gate 13. It is noted, however, that the three-layered film 16 consisting of silicon oxide film 16A, silicon nitride film 16B and silicon oxide film 1⁶C is used for the insulating film interlaid between them. This insulating film prevents the electrons from being discharged from floating gate 13. The reason for this will be descried below.

A first reason for this is that the three-layered film has a lower density of the weak spots contained in the insulating film than the single insulating film. A second reason resides in the current mechanism peculiar to the three-layered film. A number of carriers generated when the leak current is caused are electrons in silicon oxide film 16A or 1⁶C of the three-layered film, and these are holes in silicon nitride film 16B. The leak current is caused in silicon nitride film 16B either when hole current is easy to flow due to the weak spots or when electron current is easy to flow in silicon nitride film. Since there is a rare case that both currents flow simultaneously, the leak current flowing from control gate 17 toward floating gate 13 will never be increased.

As described, it will be understood that this invention successfully improves the erroneous write characteristic and the erasure characteristics.

Claims

1. A semiconductor memory device, characterized by

a semiconductor substrate (10) of a first conductivity type;

a floating gate (12) containing an impurity at a predetermined concentration and layered on a first insulating film (13) which is also layered on said substrate;

an erase gate (15) layered above said floating gate (13), with a second insulating film (14) interlaid therebetween, a part of said erase gate overlapping with said floating gate, and said erase gate containing impurity at a predetermined concentration; and

a control gate (17) layered above said floating gate (13), with a third insulating film (14, 16) interlaid therebetween;

characterized in that an impurity concentration in at least a part (13A) of said floating gate (13) overlapping with the erase gate (15) is lower than that of said erase gate (15).

2. A semiconductor memory device according to claim 1, characterized in that an impurity concentration in the whole of said floating gate (13) is lower than that of said erase gate (15).

3. A semiconductor memory device according to claim 1, characterized in that an impurity concentration in said erase gate (15) is $6 \times 10^{20}/cm^3$ or more, and an impurity concentration in said part (13A) of said floating gate (13) is less than $6 \times 10^{20}/cm^3$.

4. A semiconductor memory device according to claim 2, characterized in that an impurity concentration in said erase gate (15) is $6 \times 10^{20}/cm^3$ or more, and an impurity concentration in the whole of said said floating gate (13) is less than $6 \times 10^{20}/cm^3$.

5. A semiconductor memory device according to claim 1, characterized in that said floating gate (13), said erase gate (15) , and said control gate (17) are made of polysilicon, and the impurity contained in said floating gate (13) , said erase gate (15) and said control gate (17) is phosphorus.

6. A semiconductor memory device according to claim 1, characterized in that said floating gate (13), said erase gate (15), and said control gate (17) are made of polysilicon, and the impurity contained in said floating gate (13) , said erase gate (15) and said control gate (17) is arsenic.

7. A semiconductor memory device according to claim 2, characterized in that said floating gate (13), said erase gate (15), and said control gate (17) are made of polysilicon, and the impurity contained in said floating gate (13) , said erase gate (15), and said control gate (17) is phosphorus.

8. A semiconductor memory device according to claim 2, characterized in that said floating gate (13), said erase gate (15), and said control gate (17) are made of polysilicon. and the impurity contained in said floating gate (13) , said erase gate (15), and said control gate (17) is arsenic.

9. A semiconductor memory device according to claim 1, characterized in that an insulating film having a three-layered structure consisting of an oxide film, a nitride film, and an oxide film is interlaid between said erase gate (15) and said control gate (17) .

10. A semiconductor memory device according to claim 1, characterized in that said erase gate (15) is laid over said control gate (17), with said third insulating film (14, 16) interlaid therebetween.

11. A semiconductor memory device according to claim 1, characterized in that said third insulating film (14, 16) has a three-layered structure consisting of oxide film (14, 16A) , a nitride film (16B), and an oxide film (16C).
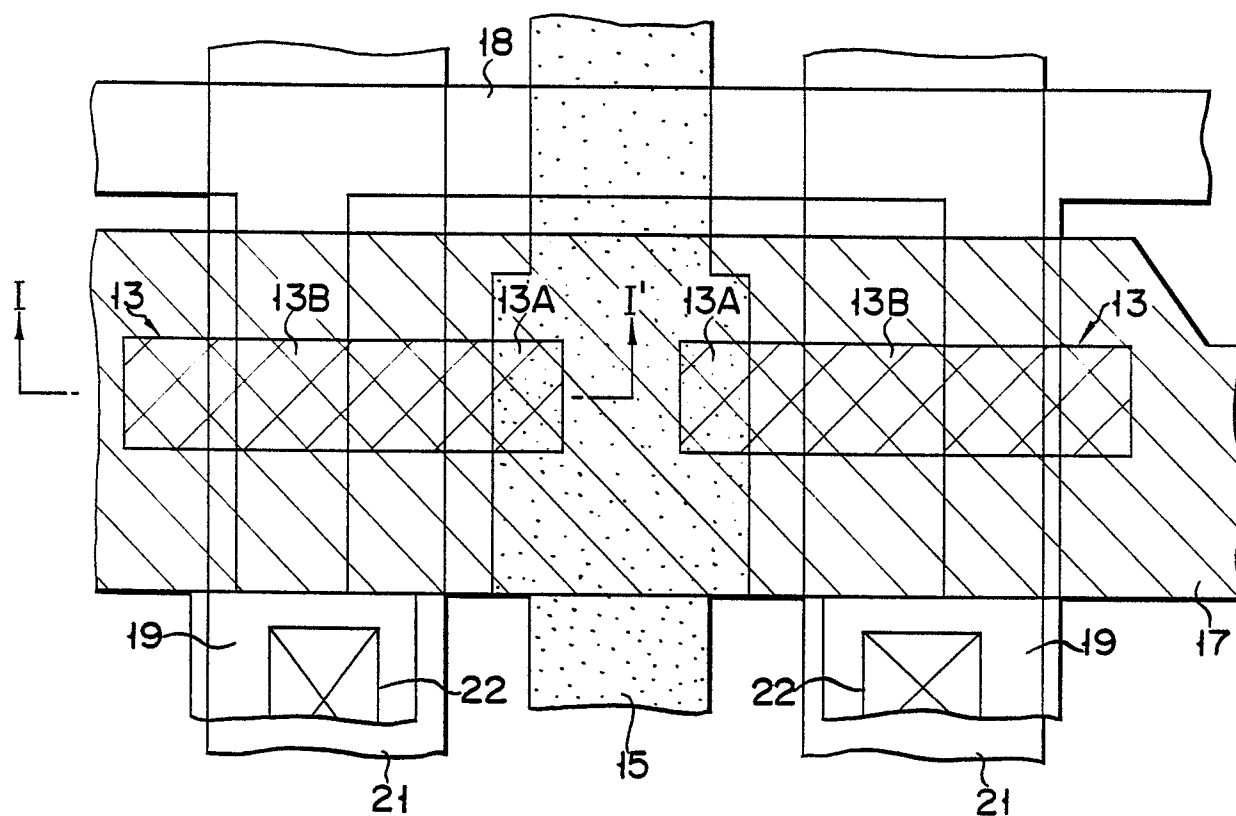
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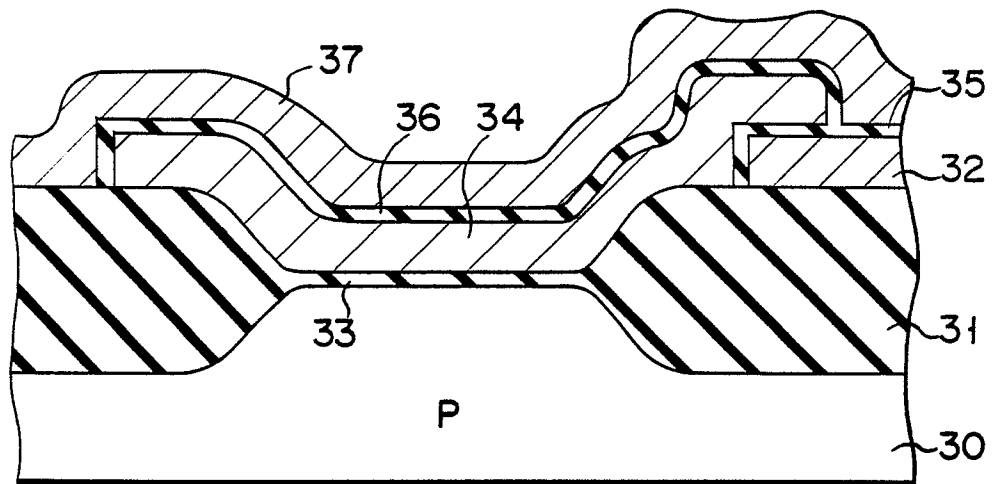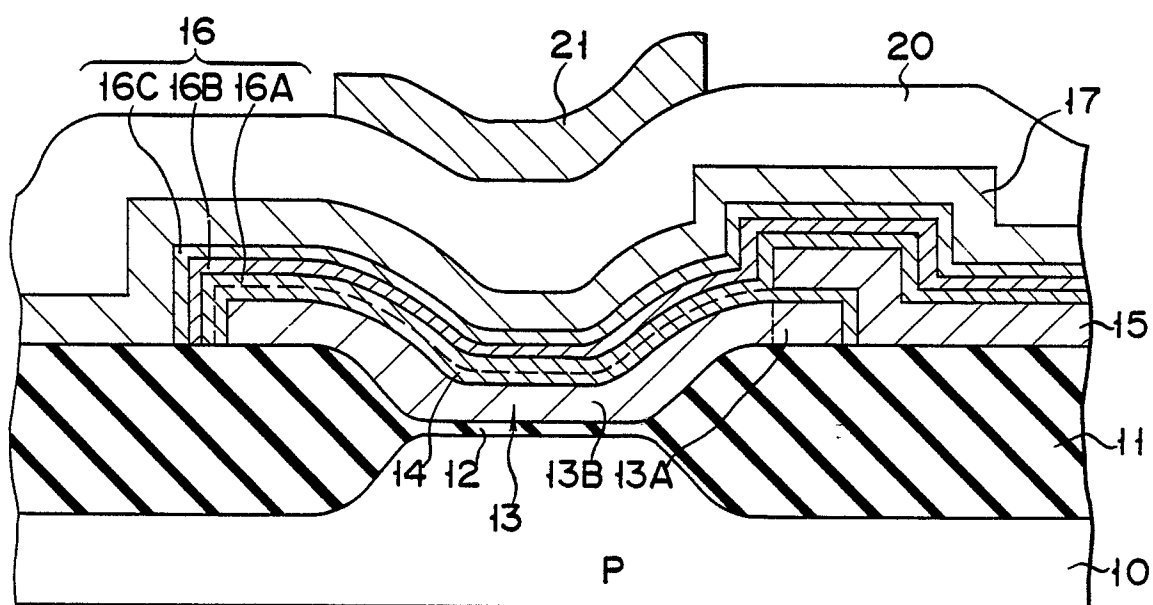
F I G. 1
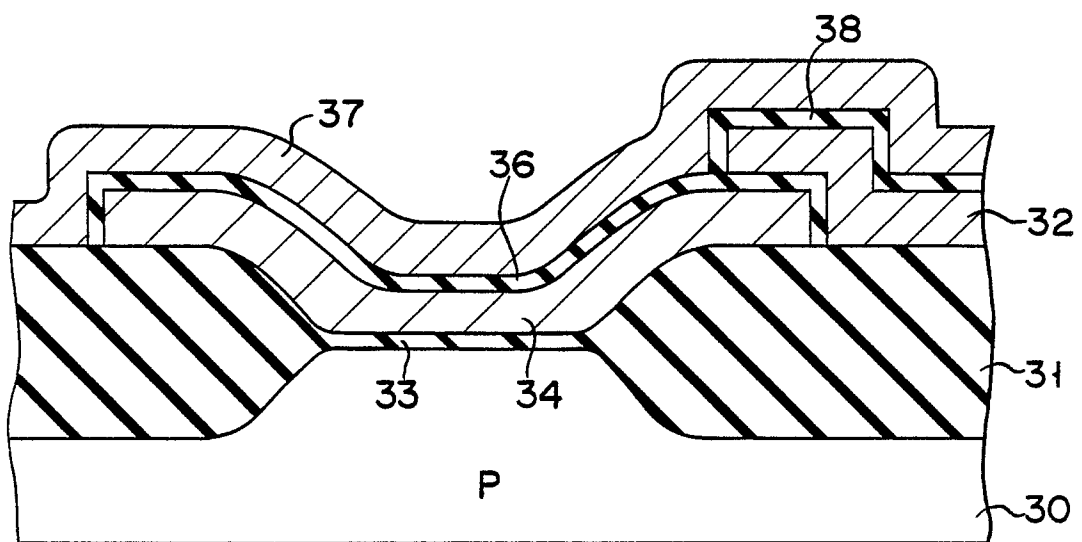
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