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(54) Signal switching processor.

(57) A signal switching processor has a plurality of input and output ports, and a number n of signal switching units (7,9) arranged in series between the input and output ports and coupled together so as to generate at each output port a data output signal corresponding to a data input signal supplied to a respective input port. The switching units are mounted in an array of rows, are coupled together by a perfect shuffle optical system (11), and are responsive to received data signals to modulate respective read signals incident on the switching units. Each of the leading n-1 switching units causes the modulated read signals to be reflected towards a respective reflector (25) for subsequent reflection towards the next row in the array of switching units.

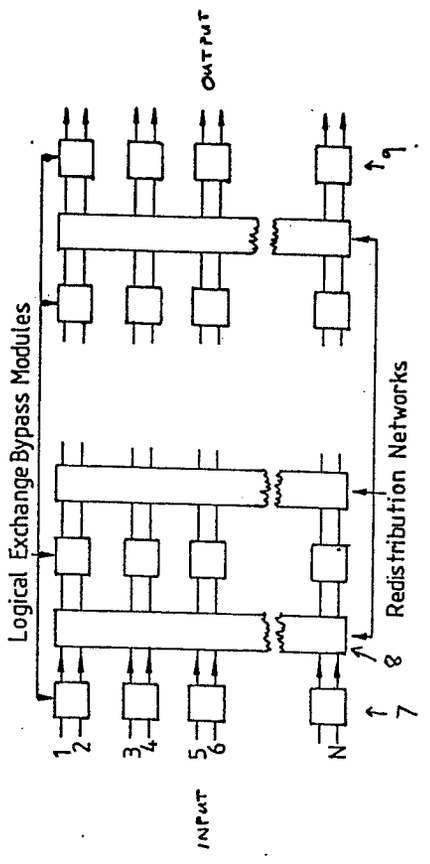

FIG 2

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SIGNAL SWITCHING PROCESSOR

The invention relates to a signal switching processor.

In a paper entitled "Light Electronics, Myth or Reality?" IEE. Proceedings, Vol 132, No. 6, December 1985, pages 371-383, an optical signal switching network is described in which optical data input signals from a number of input ports are passed through a series of switching units and an optical redistribution network so as to convey each optical signal to a respective output port. The network described can be reset very easily since the switching units are each formed from a number of self-setting exchange-bypass modules. Each module has two input ports and two output ports and can exist in one of two states thus linking each input port with a selected one of the output ports. The state of each module is set within the module during a reset operation by supplying as data input signals the addresses of the desired output ports for subsequent data from the corresponding input port. The redistribution optics together with the exchange-bypass modules are arranged so as to perform a perfect-shuffle algorithm on the addresses supplied during a reset operation.

Each exchange-bypass module comprises a pair of detectors for detecting respective input beams, a logic system, and a pair of output beam modulators which are controlled by signals from the logic system in accordance with the logic state of the module. To implement these modules, it is then necessary to supply auxiliary read beams to each of the modulators. The source of these read beams is not shown in the paper mentioned above and indeed in practice it would be very difficult to implement the arrangement shown in the paper.

For example, one solution might be to incorporate within the modules some means for generating the required modulated beams. However, it would then be necessary to mount the arrays on a large heat sink and this would then lead to further complex problems of fabrication.

In accordance with the present invention, a signal switching processor has a plurality of input and output ports, and a number n of signal switching units arranged in series between the input and output ports and coupled together so as to generate at each output port a data output signal corresponding to a data input signal supplied to a respective input port, the switching units being mounted in an array of rows, being coupled together by coupling means, and being responsive to received data signals to modulate respective read signals incident on the switching units, each of the leading n-1 switching units causing the modulated read signals to be reflected towards the coupling means which couples the signals with the next row in the array of switching units.

We have devised an improved signal switching processor which deals with the problems mentioned above by causing the leading n-1 switching units to reflect the incident read signals. This allows the array of switching units to be mounted on an efficient heat sink since no transmission of signals through the array is required. The invention also enables the source of the read signals to be positioned at a location remote from the switching units and in one example, the read signals may be supplied to the switching units from substantially the same position as the data input signals.

Preferably, each switching unit comprises a number of electro-absorption modulators one for each processor input port, the modulators being adapted to reflect an incident read beam and to modulate the read beam in accordance with data signals supplied to the switching unit.

The use of electro-absorbtion modulators is particularly suited to this invention. Typical EAMs have a thickness of about 1μm which in general is not sufficiently thick for there to be a good extinction ratio. However, by operating the modulator in a reflection mode, the incident read signal passes twice through the modulator thus doubling the absorbtion and leading to a much higher extinction ratio.

Although the invention is applicable to the switching of signals of a wide variety of wavelengths, the invention is particularly suited to the switching of optical signals in which the read signals also comprise optical signals. In this case, each switching unit may comprise a number of photodetectors, one for each input port, a number of optical signal modulators, one for each output port, and logic means to which signals from the photodetectors are fed and which passes the signals in accordance with its logical state to respective optical signal modulators which modulate respective read beams in accordance with the signals supplied.

In this case, it is particularly advantageous for the photodetectors to comprise electro-absorbtion modulators.

Where both the photodetectors and modulators comprise EAMs, this leads to a particularly simple fabrication of the switching units.

Typically, each switching unit will comprise at least one exchange-bypass module having first and second input ports and first and second output ports, the module status being selectable such that in a first state the first input and output ports and the second input and output ports are coupled

together, and in a second state the first input port is connected to the second output port and the second input port is connected to the first output port.

Preferably, the coupling means comprises a system which in conjunction with the switching units enables a perfect shuffle algorithm to be performed during a reset operation. For example, in the case where the read signals comprise optical signals, the coupling means may comprise an optical redistribution network through which the modulated read signals are passed prior to impinging on the next succeeding row in the array of switching units.

Conveniently, in the case where the read signals comprise optical signals, the read signals for each switching unit are generated by a respective laser, the processor further comprising splitting means for splitting the beams generated by each laser into a number of subsidiary beams, one for each processor input port.

Typically, each switching unit will further include clock means for controlling operation of the switching unit, the clock means being controlled by clock signals supplied to the array of switching units.

In this case, the clock signals may also be supplied from substantially the same position as the read signals and it is particularly convenient in the case where the clock and read signals comprise optical signals, if the splitting means is adapted to generate from each laser beam one or more additional subsidiary beams to constitute clock signals.

An example of a signal switching processor according to the invention will now be described with reference to the accompanying drawings, in which:-

Figure 1 illustrates an example of an exchange-bypass module (EBM) and its truth table;

Figure 2 illustrates in diagrammatic form a generalised pipeline sort processor;

Figure 3a is a logical diagram for a self-setting EBM, and Figure 3b is the associated Truth Table;

Figure 4 illustrates the three types of EBM required to form a complete switching matrix;

Figure 5 illustrates the logical layout of EBMs for a perfect shuffle sort algorithm;

Figure 6 is a schematic diagram of a reflective, folded perfect shuffle processor;

Figures 7A, 7B, and 7C are a partial section, a perspective view, and a plan respectively of part of the input/output and control subsystem for the processor of Figure 6;

Figure 8 is a block diagram of the overall control system for the processor; and,

Figure 9 is a block diagram of an exchange/bypass module fabricated on a semiconductor chip.

The signal switching assembly or processor to be described includes a pipeline sort matrix formed from a number of groups of exchange/bypass modules (EBMs). An example of the logical construction of an EBM is shown in Figure 1 and comprises four AND gates 1-4 whose outputs are coupled to respective inputs of a pair of OR gates 5, 6. The EBM has two input ports A, B connected to the AND gates 1, 2; 3,4 respectively and two output ports D, E connected to the OR gates 5, 6 respectively. The output ports of the AND gates 1, 3 are connected to the input ports of the OR gate 5 while the output ports of the AND gates 2, 4 are connected to the input ports of the OR gate 6.

The status of the EBM is set by a control signal C fed to the AND gates 1, 4 and its logical complement $\overline{C}$ fed to the AND gates 2,3.

As can be seen from the Truth Table in Figure 1, the EBM is set in its bypass state when the control signal C is logical 1 resulting in a signal on the input port A being passed to the output port D and a signal on the input port B being passed to the output port E. When the control signal C is logical zero, the EBM is in its exchange state in which the signal on input port A is coupled with the output port E and the signal on input port B is coupled with output port D.

Figure 2 illustrates a generalised sort processor having N input ports and N output ports. The input ports are connected in pairs to respective EBMs of a first group 7 whose output ports are connected to a redistribution network 8. The redistribution network has a fixed pattern and couples each input line with a respective output line. As can be seen in Figure 2, this generalised sort processor comprises a number of pairs of EBM groups and redistribution networks together with a final group of EBMs 9 connected to the output ports of the processor.

In this example, we propose that the redistribution networks should be arranged such that the matrix performs a perfect shuffle algorithm. This is particularly suitable for optical signal implementation since each redistribution network has an identical form and so can be fabricated by a common network.

The use of the perfect shuffle for sorting was first described many years ago. For a matrix having N input ports where M = log(N) and log is to base 2, a first cut design requires MxM rows each of N/2 EBMs between the N input and N output ports with perfect shuffle interconnects between each row. These involve three types of logical EBM shown in Figure 4. By the terminology "logical EBM", we imply a module that includes the logic to establish whether it should self set to the exchange

or bypass state according to the address data presented to it through its input ports. The "0" module always bypasses whilst the "+" and "-" modules always route the larger of the two addresses (numbers) to the port marked "h". They are thus logically identical in structure but are mirror images in function.

Figure 5 shows the logical layout for a full 32x32 matrix using the perfect shuffle sort algorithm for its self addressing function. Here N = 32 and M = 5. The layout has been deliberately split into five groups of five rows, with each row containing 16 modules. The data lines emerging from each row of 16 EBMs are perfect shuffled before entering the next row. After the first five rows, (ie. at the output of row five), the input data has been sorted into 8 bitonic sequences, with the adjacent pairs of inputs reversed or not according to the address size and spatial position. After the succeeding groups of five rows, the addresses have been sorted into 4 bitonic sequences, 2, 1 and finally into a linearly ascending sequence at row 25.

The result of this wiring pattern is that after every block of M EBMs, the address data has been bitonically sorted, initially into N/4 sequences and then by factors of two into ever larger sequences. However, it also emerges that the first M-1 rows of "0" EBMs can be completely discarded without altering the overall operation of the matrix. Accordingly, we only need M(M-1)+1 rows of EBMs to implement the matrix. Moreover, of these, 1+2+..-(M-2) = (M-1)(M-2)/2 are entirely composed of "0" EBMs and thus play no active role in the sort. Accordingly, we find the following results:-

Total number of EBM nodes = (N/2).(M(M-1)-+1)

Total number of shuffles = M(M-1)

Number of active EBM nodes = (N/4)M(M-1)

For the case of 128 input ports, M=7, and these evaluate to 2752, 42 and 1344 respectively.

The optical implementation of the perfect shuffle wiring between each row is described below.

It should be noted that a perfect shuffle of the numbers from 1 to N simply involves two operations. In the first, they are split into two equal sequences, 1 to N/2 and N/2+1 to N. Setting N/2 = P for ease of writing, in the second operation these are interleaved to form the sequence:-

1, P+1, 2, P + 2, 3, P+3, ...N/2,N

The fact that this is readily done optically with zero time skew in two dimensions is a major attraction since it allows one to monolithically integrate all the logical EBMs onto a single chip and to use a single optical system to provide all the interconnects in parallel through space normal to the chip.

The setting of each EBM is determined by address data supplied to each input port of the matrix. This address data defines the matrix output port to which subsequent signals are to be switched. The use of logical EBMs is particularly advantageous in this connection since they respond to the relative size of the two addresses arriving at each input port of the respective pair (see Truth Table of Figure 3B). The only action required on the EBM is always to deliver the larger number to the same defined (by position) exit port. Such a logical operation on binary MSB first addresses is trivial, since identical bits always pass directly through. The first pair of bits in the address to differ then define uniquely the larger of the two numbers.

Figure 3a illustrates the overall logical circuit for an EBM where I1, I2, O1, O2 are the input ports and output ports respectively; R indicates a reset signal; and P, Q indicate control inputs and outputs for latching the EBM in one of its two states.

An example of the full Truth Table for the EBM of Figure 3a is shown in Figure 3b.

If the status of the EBM is set or selected then the reset signal R will be logical 1 and the signals P, Q will define whether the state is bypass, exchange, or not yet set. When R=0, the device is in reset mode, as illustrated in Figure 3b. Consider for example line 15 of the Truth Table where Q (n-1) = 1 and P (n-1) = 0. This corresponds to the exchange state and it will be seen that the signal on port I1 has been switched to port O2 and the signal received at port I2 has been switched to port O1.

If the status of the EBM is to be reset, the reset signal is switched to zero causing Q(n) and P(n) to be zeroed thus implying that the EBM is thereafter not set and preparing the EBM to be set once the reset signal returns to logical 1. Upon this return, the EBM will treat the next data received on its input ports I1, I2 as address or setting data. For example, consider line 13 in the Truth Table where Q(n-1) and P(n-1) are both zero implying that the EBM is not set. Since R=1, the data on input ports I1, I2 is treated as setting data which in this case sets the EBM in the exchange mode and also exchanges that address data.

The reset operation will be explained in more detail in due course.

Figures 6 to 9 illustrate a practical implementation of a perfect shuffle sort matrix of the type shown in Figure 2.

Each group of EBMs is fabricated in a manner to be described below into a logic array 10 (Figure 6) comprising a number of rows of EBMs, each row corresponding to one group (such as the group 7 in Figure 2). In the case of the perfect shuffle algorithm, each redistribution network has an identical form and in this example is defined optically by a lens system 11. As in previous implementa-

tions, this shuffle optics relies upon the concept of magnifying an image laterally by a factor of 2, shearing the image into two, and overlaying the two halves to form a shuffled image. It also has some additional advantages not previously achieved since it allows the whole optical system to be folded into a compact sub unit embracing the return data path to the array. It also brings together all the input/output and control channels in a single port 12 located opposite the logic array 10.

The logic array 10 is fabricated on a single chip of for example GaInAs/InP with a band gap in the 1300-1500 nm region. The array comprises a number of MQW electro-absorption modulators (EAM), two for each EBM, each of which can be addressed by an externally generated "read" laser beam.

An example of one EBM within the logic array is shown in Figure 9. This comprises a pair of photodetectors 13,14 formed, for example, from electro-absorbtion modulators. The electronic output signals from these photodectors 13, 14 are fed to respective gain and thresholding circuits 15 whose outputs are fed to an EBM logic circuit 16. A photodetector 17 also formed from an electro-absorbtion modulator is responsive to a clock laser beam to provide clock signals to the EBM logic circuit 16. The electronic output signals from the EBM logic circuit 16 are fed to respective EAM drivers 18, 19 which drive respective electro-absorption modulators 20, 21. An external read beam is supplied to each EAM 20, 21 which modulates the beam to generate the required output signal.

The arrangement of Figure 9 is particularly useful for a number of reasons. Firstly, the optical source of the "read" beam can be located away from the active chip and can thus dissipate its heat elsewhere. This has a secondary, but important advantage, that this enables the beam also to be used for timing and control purposes. Secondly, by externally addressing the modulators, the exit beam direction can be derived from the input. This is highly desirable in order to implement the shuffle wiring scheme. Thirdly, EAMs are known to be inherently fast (sub 100 ps switching speed), are readily fabricated and lend themselves to monolithic integration. They are also (optically) non-resonant so that they are relatively insensitive to temperature and wavelength.

The input/output system positioned at the port 12 in Figure 6 is illustrated in detail in Figure 7. At the input port 12 is positioned a composite, layered I/O structure 22 shown in detail in Figure 7A. This comprises the output end of an input fibre array 23 composed of a number of optical fibres, one for each input port of the matrix, as a top layer followed by alternate layers of microlenses 24 and reflectors 25, there being one pair of layers 24, 25 corresponding to each row of EBMs, and terminating with the input end 26 of an output fibre array 27. In this example, there are 128 input ports and 128 output ports with 64 EBMs in each row.

In order for the EBMs to function, it is necessary to supply three pump laser beams to each EBM. These provide the two "read" beams to the EAMs 20, 21 and the clock beam supplied to the photodetector 17. Each set of three beams is provided in this example by a respective laser the power from which is fanned out into 3 N/2 spots (N is the number of EBMs) on the associated row position on the I/O element 22 to generate three beams to each EBM. These beams are fed via the microlenses 24 associated with the respective EBM row to the logic array 10. Each laser thus provides synchronisation and interrogation for all the EBMs in a single logical row of the pipeline. The laser will be clocked with the appropriate phaseing for that row position. Since all the M(M-1)+1 clock lasers can be colocated in a linear array and will require identical delays between each, it is believed that very accurate clocking should be possible. In addition, the rows enjoy zero clock skew as a result of the optical delivery system.

To examine the operation of the whole matrix, we will follow a signal through from input to output, initially ignoring the control aspects and simply assume that each EBMs exchange or bypass status is already established. Data arrives at the input ports via the input fibre array 23 and passes through the I/O structure 22 at a transparent row space. The lower half of the optical system 11 then images the signals onto the first row of 128 input photodetectors 13, 14 associated with 64 EBMs. The photodetectors 13, 14 generate corresponding electrical signals which are applied to the gain/threshold circuits 15 and then fed to the EBM logic 16 which generates appropriate signals depending on the exchange or bypass state to the drivers 18, 19. These drivers 18, 19 then control the EAMs 20, 21.

In order to read the output signals, interrogation beams from the pump source previously described are injected via the first row of microlenses 24, the interrogation beams impinging onto the logic array at different angles which will be imposed upon them by means of prisms (solid or holographic) located at the I/O element 22. The prisms are indicated by reference numeral 30 (Figure 6). The reason for this is that it is desirable to spatially separate the optical beams emerging from the two halves (1 to P and P+1 to N) of the array in order to operate the shuffle optical system with minimum power loss.

The two read beams are reflected from the respective EAMs 20, 21 after modulation and are guided by the shuffle optics 11 to impinge upon

the first reflector layer 25 of the I/O element 22 to form a shuffled array of outputs at the reflector and are then imaged back to the input photodetector array of the next row of EBMs.

This sequence is then repeated for each row of EBMs with the read beams from the final row of EAMs being guided to the output fibre array 26.

Figure 8 shows a block diagram of the complete processor. At the input to the switching matrix 31, having the Figure 6 structure, a storage register, 33 is positioned which notionally uses electronic logic. In the address register 33, N registers store the desired matrix output port address associated with each matrix input port. Thus if input port 23 is to be connected to output port 56, the number 56 is stored in the 23rd address register. Within the address register 33, the complete set of addresses from 1 to N is stored. If some channels are not active, then one of the unused exit port addresses is stored in its register.

An input buffer 32 is set in the data input line to store data during the reset intervals. This need not be very large, perhaps 20 to 30 bits per input line. The processor is controlled by timing electronics 34.

To establish a global reset of the matrix the clock signal (CK) generated by a clock laser array 36 as previously described is removed (turn off the appropriate clock laser) and the EBM logic is designed so that it falls back to the reset state in the absence of the clock. Any row of the matrix can now be reset at will.

Following the reset operation, the set of N output port addresses is injected via a fibre laser input array 35 and the data path 23 in MSB first format. The EBM examines addresses entering its input ports and as soon as two address bits differ, latches to the appropriate exchange or bypass state and remains there until reset. Immediately following the address bits (7 bits), the data from the buffer 32 follows. If no data is present on a line, then we may consider that channel as remaining idle. In practice it might be necessary to inject some dummy data to limit the signal disparity in the electronic EBM stages.

A further advantage of the linear clock laser array can now be understood. Assume that the EBM logic involves (of order) 10 clock pulses from input to output. Also assume that the round trip optical path through the shuffle optics is of order 50 cms. This will take about 2ns. At a data rate of 10Gbit/s, this corresponds to 20 bits. Accordingly, we have flow delay of about 30 bits per row and about 1200 bits per matrix or about 120ns.

It would be undesirable to close down the whole matrix for a block of this order every time reset was required. Using the discrete clocks, we need only adopt the following sequence. Stop clock, pause for reset, start clock and allow to synchronise, inject 7 bits address. We might postulate this taking 20 bit intervals. The next row can then be shut down and reset using the same sequence but starting 30 bit intervals later. Thus the first rows of the matrix can be reset while the tail of the previous data stream is still passing through the later rows of the matrix. It was for this reason that we suggested the clock laser array be driven in a linear sequence. For the example given above, we would introduce a 30 bit delay between each laser driver for obvious reasons, delaying in particular the control/set/reset signal. It also follows from these considerations that the input data flow in a circuit switched network need only be interrupted for 20-30 bits while reset occurs and this sets in turn the size required for the input buffers.

Clearly these operations need to be under the control of the central clock 34 as shown in Figure 8. Note that although the various modules requiring accurate synchronisation appear widely distributed physically, in reality they will be clustered together very intimately in the region of the I/O structure 22 of Figure 6. Thus, it is likely that they can be packaged in a single sub-assembly, optically connected via fibre highways to the I/O element and with very intimate connection to the single control sub-system.

Claims

1. A signal switching processor having a plurality of input and output ports, and a number n of signal switching units arranged in series between the input and output ports and coupled together so as to generate at each output port a data output signal corresponding to a data input signal supplied to a respective input port, the switching units being mounted in an array of rows, being coupled together by coupling means, and being responsive to received data signals to modulate respective read signals incident on the switching units, each of the leading n-1 switching units causing the modulated read signals to be reflected towards the coupling means which couples the signals with the next row in the array of switching units.

2. A processor according to claim 1, the processor being adapted to perform a perfect shuffle algorithm on output port address signals supplied as data input signals to the input ports during a reset operation to select the input and output ports of the processor which are coupled together.

3. A processor according to claim 1 or claim 2, wherein each switching unit comprises a number of electro-absorption modulators one for each processor input port, the modulators being adapted to

reflect an incident read beam and to modulate the read beam in accordance with data signals supplied to the switching unit.

4. A processor according to any of the preceding claims, wherein the data input and output signals and the read signals comprise optical signals.

5. A processor according to claim 4, wherein each switching unit comprises a number of photodetectors, one for each input port, a number of optical signal modulators, one for each output port, and logic means to which signals from the photodetectors are fed and which passes the signals in accordance with its logical state to respective optical signal modulators which modulate respective read beams in accordance with the signals supplied.

6. A processor according to claim 5, wherein the photodetectors comprise electro-absorbtion modulators.

7. A processor according to any of the preceding claims, wherein each switching unit comprises at least one exchange-bypass module having first and second input ports and first and second output ports, the module status being selectable such that in a first state the first input and output ports and the second input and output ports are coupled together, and in a second state the first input port is connected to the second output port and the second input port is connected to the first output port.

8. A processor according to any of the preceding claims, wherein the switching units are fabricated on a common substrate.

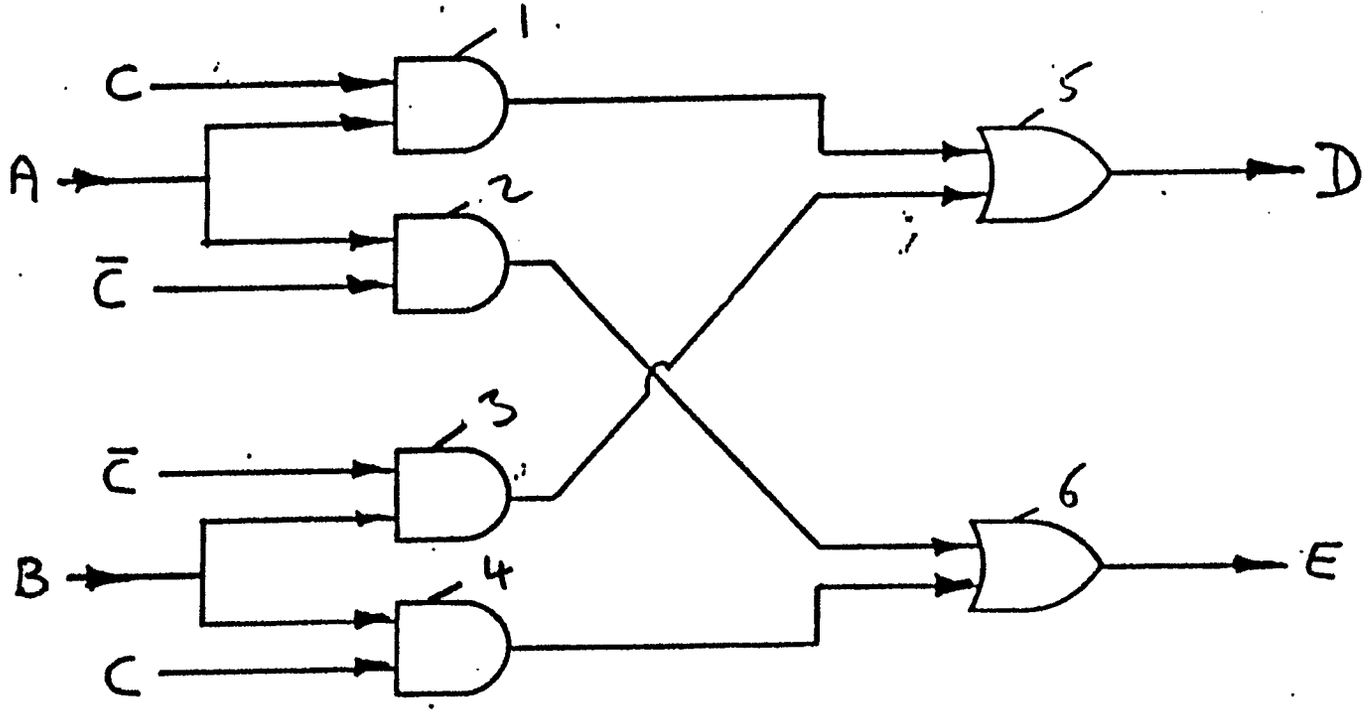
9. A processor according to any of the preceding claims, wherein each switching unit includes clock means for controlling operation of the switching unit, the clock means being controlled by clock signals supplied to the array of switching units.

10. A processor according to claim 9, wherein the clock signals are supplied from substantially the same position as the read signals.

11. A processor according to any of the preceding claims, further comprising an I/O member having a number of layers of microlenses through which the read signals are supplied interposed between reflective layers comprising part of the coupling means for reflecting modulated read signals towards the next succeeding signal switching unit.

12. A signal switching processor substantially as hereinbefore described with reference to the accompanying drawings.

Logical Exchange/By-pass



Optical Pump
& Clock

C	$\bar{C}$	
0	1	exchange
1	0	bypass

- gain
- unidirectional
- clocked (synchronous)

FIG 1

0 282 227

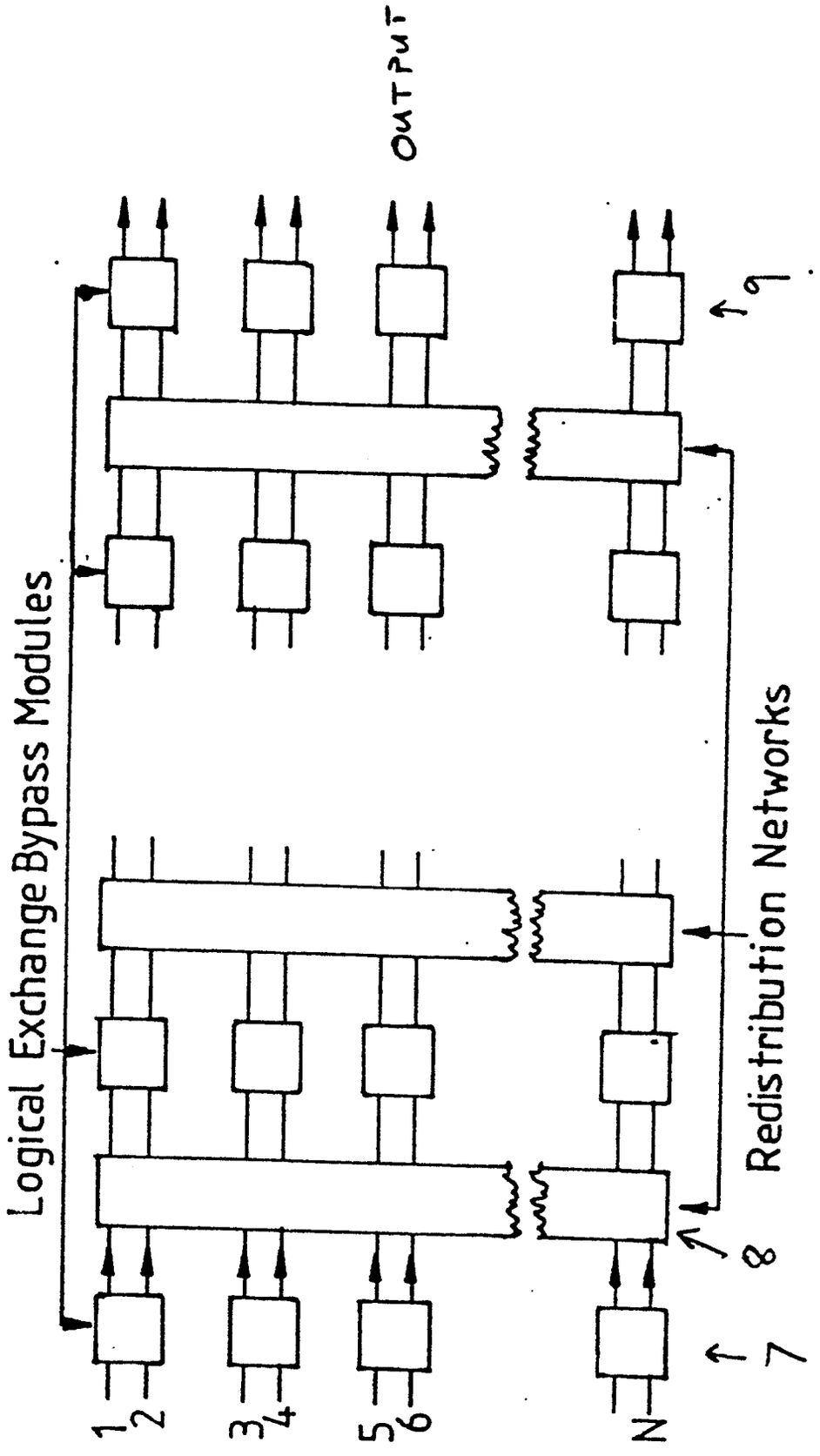
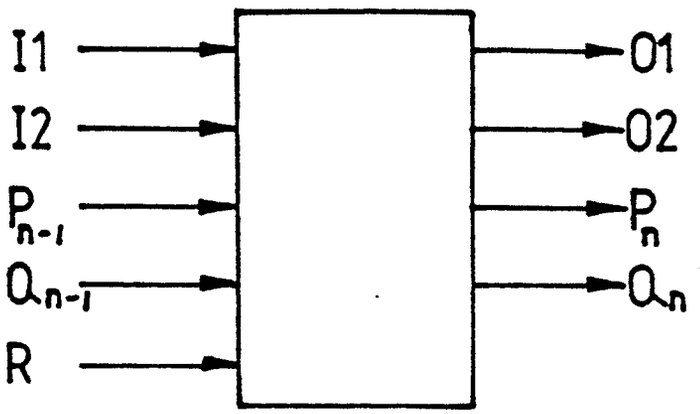

OUTPUT
Logical Exchange Bypass Modules
Redistribution Networks
INPUT
1
2
3
4
5
6
N
7
8
9

FIG 2



Logical Exchange-Bypass Module

FIG 3a

EXCHANGE-BYPASS MODULE
FULL TRUTH TABLE

I1	I2	R	Q(n-1)	P(n-1)	Q(n)	P(n)	O1	O2	Comment
0	0	0	0	0	0	0	x	x	
0	0	0	0	1	0	0	x	x	
0	0	0	1	0	0	0	x	x	
0	0	0	1	1	0	0	x	x	
0	0	1	0	0	0	0	0	0	Defer set, hold BP
0	0	1	0	1	0	1	0	0	Hold BP
0	0	1	1	0	1	0	0	0	Hold EX
0	0	1	1	1	0	0	0	0	Defer set, hold BP
0	1	0	0	0	0	0	x	x	
0	1	0	0	1	0	0	x	x	
0	1	0	1	0	0	0	x	x	
0	1	0	1	1	0	0	x	x	
0	1	1	0	0	1	0	1	0	Set EX
0	1	1	0	1	0	1	0	1	Hold BP
0	1	1	1	0	1	0	1	0	Hold EX
0	1	1	1	1	1	0	1	0	Set EX
1	0	0	0	0	0	0	x	x	
1	0	0	0	1	0	0	x	x	
1	0	0	1	0	0	0	x	x	
1	0	0	1	1	0	0	x	x	
1	0	1	0	0	0	1	1	0	Set BP
1	0	1	0	1	0	1	1	0	Hold BP
1	0	1	1	0	1	0	0	1	Hold EX
1	0	1	1	1	0	1	1	0	Set BP
1	1	0	0	0	0	0	x	x	
1	1	0	0	1	0	0	x	x	
1	1	0	1	0	0	0	x	x	
1	1	0	1	1	0	0	x	x	
1	1	1	0	0	0	0	1	1	Defer set, hold BP
1	1	1	0	1	0	1	1	1	Hold BP
1	1	1	1	0	1	0	1	1	Hold EX
1	1	1	1	1	0	0	1	1	Defer set, hold BP

NOTE - Entry of "x" implies "don't care state"
P=Q implies not set.
P=1, Q=0 implies bypass
P=0, Q=1 implies exchange

FIG 3b

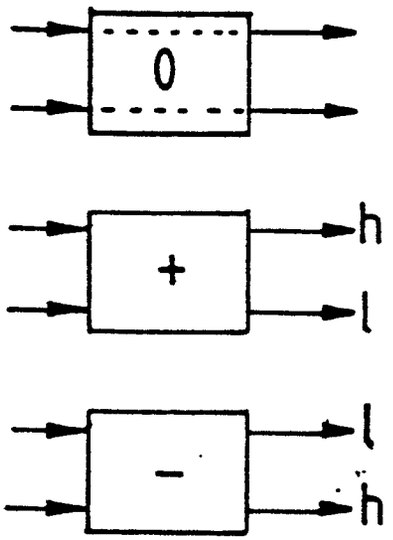


FIG 4

Row	32 input lines															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	+	−	+	−	+	−	+	−	+	−	+	−	+	−	+	−
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	+	−	+	−	+	−	+	−	+	−	+	−	+	−	+	−
10	+	+	−	−	+	+	−	−	+	+	−	−	+	+	−	−
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	+	−	+	−	+	−	+	−	+	−	+	−	+	−	+	−
14	+	+	−	−	+	+	−	−	+	+	−	−	+	+	−	−
15	+	+	+	+	−	−	−	−	+	+	+	+	−	−	−	−
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	+	−	+	−	+	−	+	−	+	−	+	−	+	−	+	−
18	+	+	−	−	+	+	−	−	+	+	−	−	+	+	−	−
19	+	+	+	+	−	−	−	−	+	+	+	+	−	−	−	−
20	+	+	+	+	+	+	+	+	−	−	−	−	−	−	−	−
21	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
22	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
23	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
24	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+
25	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+

32 output lines

N = 32
M = 5

FIG 5

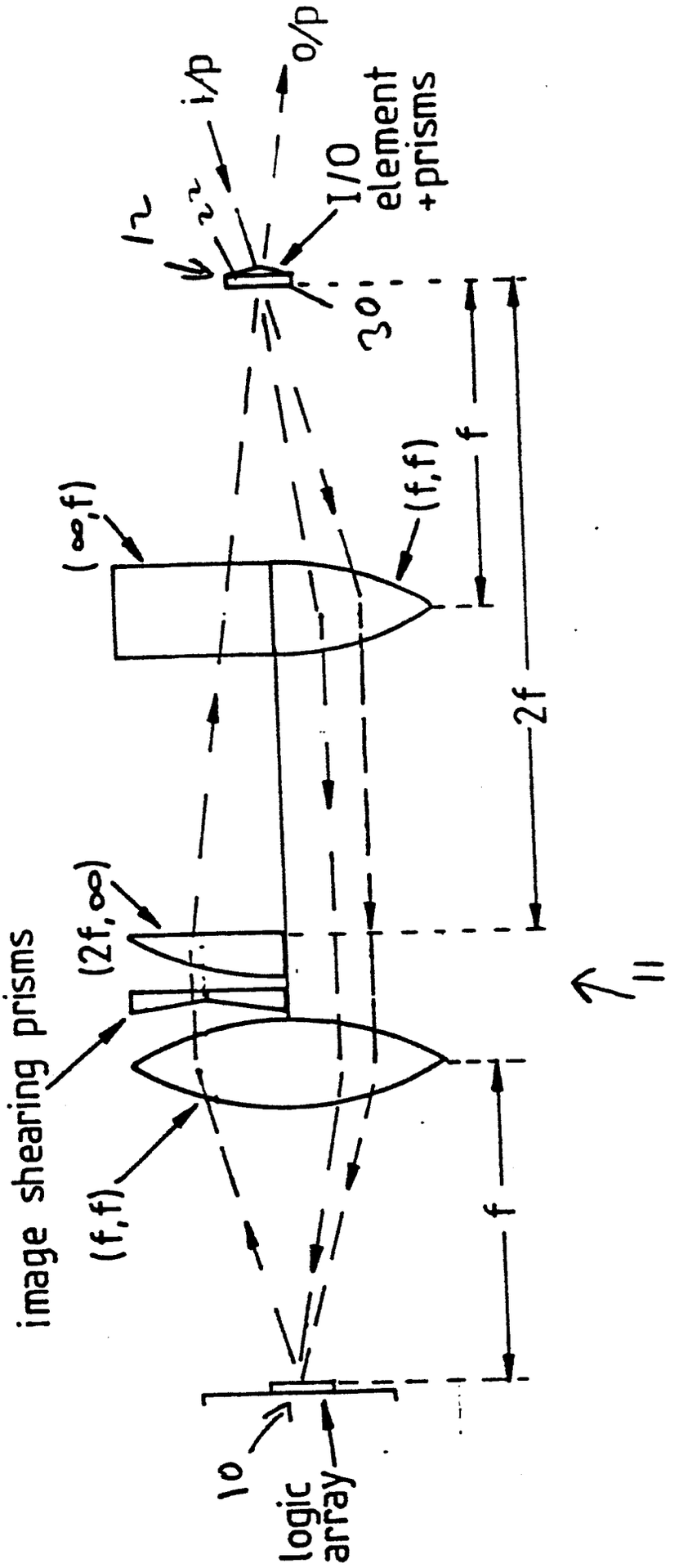

o/p
i/p
I/O element +prisms
12
22
30
(∞,f)
(f,f)
f
2f
(2f,∞)
image shearing prisms
(f,f)
f
10
logic array
11

FIG 6

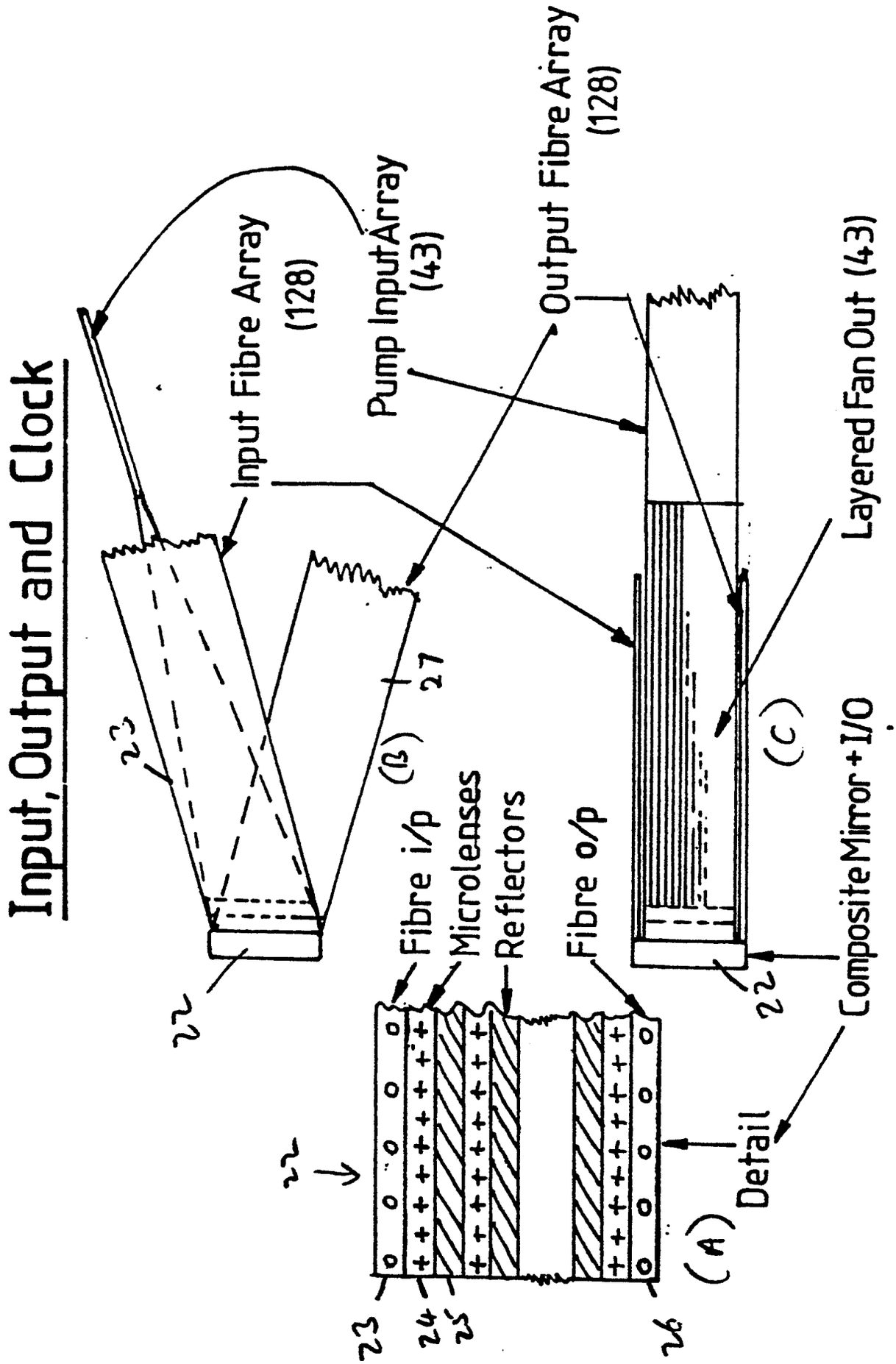

Input, Output and Clock
Input Fibre Array (128)
Pump Input Array (43)
Output Fibre Array (128)
Layered Fan Out (43)
Composite Mirror + I/O
Fibre i/p
Microlenses
Reflectors
Fibre o/p
Detail
(A)
(B)
(C)
22
23
24
25
26
27

FIG 7

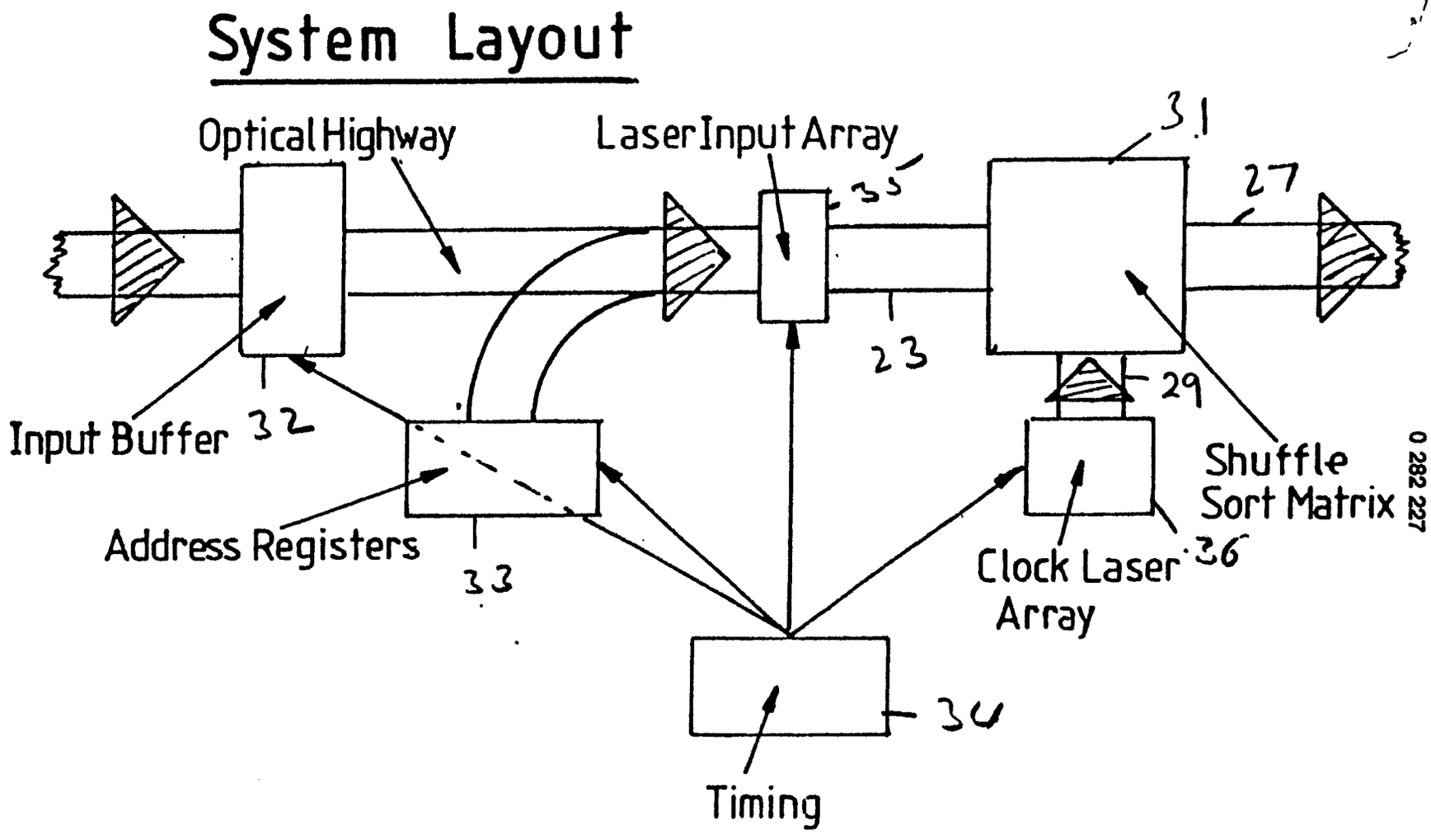

System Layout
Optical Highway
Laser Input Array
35
31
27
23
29
Input Buffer 32
Address Registers
33
Shuffle
Sort Matrix
Clock Laser
Array
36
34
Timing
0 282 227

FIG 8

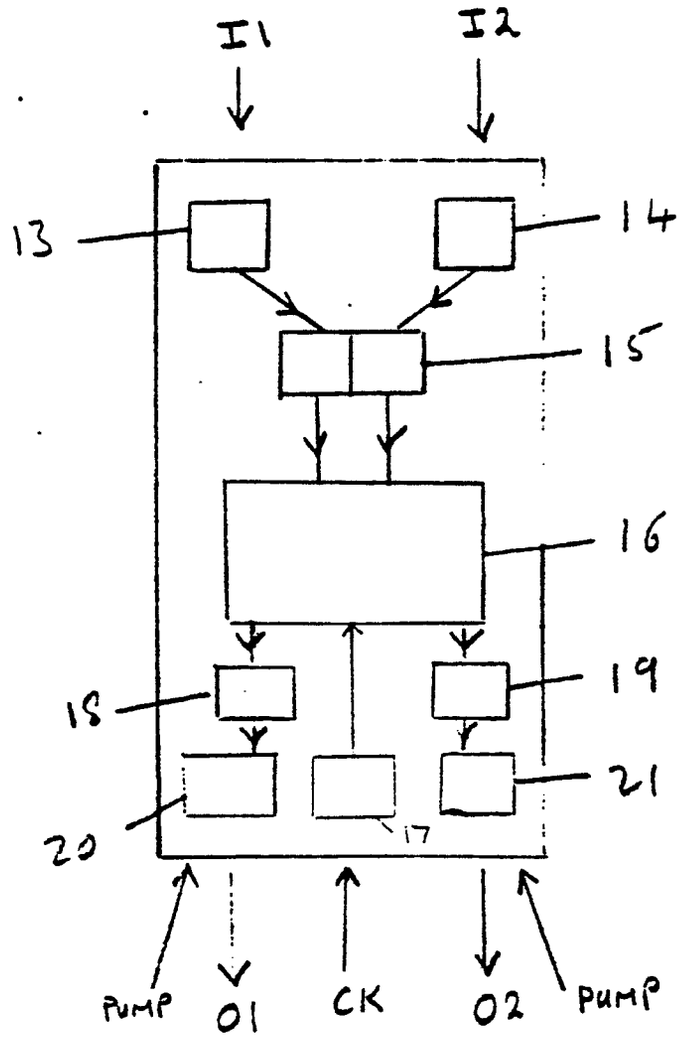


FIG 9

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 30 1841

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
D,A	IEE PROCEEDINGS, vol. 132, part J, no. 6, December 1985, pages 371-383, Hitchin, GB; J.E.MIDWINTER: "'Light' electronics, myth or reality?" * Pages 380,381, paragraphs 6.3,6.4 * ---	1-2,4,7	H 04 Q 3/52 H 04 B 9/00 G 06 F 7/56
A	WO-A-8 700 314 (ATT) * Figures 6-8; page 9, line 23 - page 14, line 25 * ---	1-2,4,7	
A	IEEE TRANSACTIONS ON COMPUTERS, vol. C-20, no. 2, February 1971, pages 153-161, IEEE, New York, US; H.S.STONE: "Parallel processing with the perfect shuffle" * Pages 156-159, paragraph V * ---	1,7	
A	PROCEEDINGS OF THE IEEE, vol. 72, no. 7, July 1984, pages 850-866, IEEE, New York, US; J.W.GOODMAN et al.: "Optical interconnections for VLSI systems" ---		TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	THE 6TH ANNUAL SYMPOSIUM ON COMPUTER ARCHITECTURE, 23rd-25th April 1979, Long Beach, pages 168-177, IEEE, New York, US; J.H.PATEL: "Processor-memory interconnections for multiprocessors" -----		H 04 Q G 06 F H 03 K H 04 B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-05-1988	VANDEVENNE M.J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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