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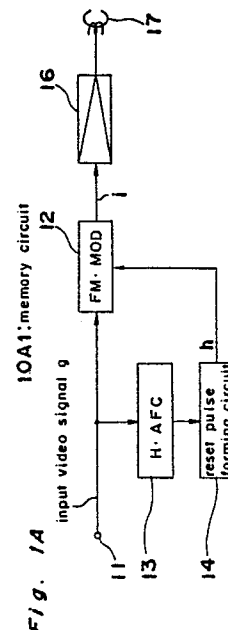
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54 **Jitter-detecting apparatus for a video tape recorder.**

57 An improved jitter detecting method and an apparatus thereof, for detecting a jitter generated in a reproduced video signal of a VTR or video disc wherein a frequency-modulated carrier of a video signal is recorded by synchronizing the leading edge of a sync signal with the phase of the forefront carrier of a constant frequency carrier train corresponding to a sync tip for every horizontal period at the time of a frequency-modulation, and from the reproduced frequency-modulated carrier the phase-reset constant frequency carrier train is abstracted as a reference burst signal, thereby to be capable of removing a time-base error by detecting a specific zero-crossing timing of the abstracted carrier burst through a bandpass filter based on the trailing edge of a frequency-modulated sync signal at the reproduction.



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Jitter Detecting Apparatus for Detecting a VTR Recording/Reproducing Video Signal

The present invention relates to a jitter detecting apparatus for detecting a VTR recording/reproducing video signal to be applied to a recording/reproducing apparatus which records and reproduces a video signal by multiplying a luminance signal and a chrominance signal on time bases.

Description of Related Art

In a video signal reproduced by a recording/reproduction apparatus, a time base fluctuates, i.e., a jitter is generated. A jitter includes a phase jitter and a frequency jitter (velocity error). In principle, the frequency jitter causes the expansion and compression of a horizontal period to occur.

Normally, the fluctuation amount of the frequency jitter is very slight even on a reproduced picture of a home video having a relatively simple mechanism. Therefore, the correction of the phase jitter of a reproduced video signal is enough to ensure the stabilization of a reproduced image.

The correction of the phase jitter generated in a video signal can be applied to the following processings without giving rise to problems: The decrease of a random noise using a frame correlation, the synthesizing of two-channel video signals, specific processings such as a fade-in or a fade-out, and a digital processing operation for performing a double speed scanning in a high dignity television (for example, IDTV).

Fig. 11 shows an example of a jitter detecting circuit 20, for correcting a phase jitter, for use in such a recording/reproducing apparatus (hereinafter referred to as VTR.)

The jitter detecting circuit 20 shown in Fig. 11 is used for a broadcasting VTR in which composite video signals generated by NTSC system, PAL system, or the like are recorded by direct frequency modulation recording system.

A reproduced video signal (a) (shown by (A) in Fig. 12) of, for example, the NTSC system supplied to a terminal 1 is inputted to a synchronizing separating circuit 2 in which a horizontal synchronizing signal (b) (shown by (B) in Fig. 12) is extracted and separated from the video signal (a). A burst gate pulse (not shown) generated from the horizontal synchronizing signal (b) is supplied to a burst gate circuit 3 in which a burst signal (c) (shown by (C) in Fig. 12) is separated from the burst gate pulse.

The burst signal (c) is supplied to a narrow bandpass filter 4 in which a burst signal (d) (shown by (D) in Fig. 12) high in C/N is produced.

The horizontal synchronizing signal (b) is supplied to a delay pulse generating circuit 5 in which a delay pulse (e) (shown by (E) in Fig. 12) is generated. The delay pulse (e) and the burst signal (d) which has passed through the narrow bandpass filter 4 are supplied to a jitter pulse generating circuit 6, thus a jitter detecting pulse (f) (shown by (F) in Fig. 12) being generated. The phase of the leading edge of the jitter detecting pulse (f) lags a predetermined period of time behind the phase of the horizontal synchronizing signal (b).

The phase of the trailing edge of the jitter detecting pulse (f) is obtained by detecting a specific zero crossing point of the burst signal (d). The write timing of a time base correcting circuit (TBC) is determined on the basis of the timing of the fall of the jitter detecting pulse (f).

The fluctuation of the time base in the reproduced video signal (a) causes the time base of the specific zero crossing point of the burst signal (d) to fluctuate. Thus, a video signal can be written in the time base correcting circuit (TBC) in synchronization with a generated jitter.

A burst signal is not produced if a TCI (Time Compressed Integration) system is adopted as a video signal recording system whereas it is generated in the direct frequency modulation recording.

Figure 13 shows the signal format of MTCI (Modified Time Compressed Integration) system, of the TCI system, in which a band-compressed chrominance signal is recorded in line sequential system.

Compressed component chrominance signals, for example, color-difference signals R-Y of red and B-Y of blue are inserted and multiplied in a horizontal blanking period as shown by (A) and (B) in Fig. 13.

Reference symbol (Y) denotes a luminance signal. The color-difference signals R-Y of red and B-Y of blue are inserted into the line sequential system.

Normally, a jitter detecting signal is obtained by detecting the rise or fall of a horizontal synchronizing signal in a video signal reproduced by such a signal format.

As described above, a jitter detecting signal is detected according to the detection of the rise or fall of the horizontal signal in the TCI recording system. This system has a disadvantage in that a jitter detection cannot be performed with a high accuracy.

The generation of a jitter detecting signal based on the fall of the horizontal synchronizing signal is described with reference to Fig. 14.

Normally, noise (N) whose phase and level are random is superposed on a horizontal synchronizing signal. Therefore, if a detecting level is set to (A), the detection timing fluctuates by ΔT caused by the phase of the superposed noise (N). The fluctuation amount ΔT (fluctuation amount of time base, namely, amount of synchronizing jitter) affects the accuracy in detecting a jitter detection.

The fluctuation amount ΔT of a horizontal synchronizing signal is approximated at an intermediate level assuming that its signal band is 4MHz and S/N is 40dB.

As shown in Fig. 15, assuming that the amplitude of a horizontal synchronizing signal is 1 Vp-p, the effective value of the noise (N) superposing on the horizontal synchronizing signal (b) whose amplitude is 0.3 is approximately 10mV. Supposing that the fall portion of the waveform of the horizontal synchronizing signal can be approximated by 1/2 cycle of a sine wave of 4MHz, the inclination (K) of the level at the center of the sine wave is expressed as follows:

$$K = 125\text{ns} / (0.3 (\pi/2)V) \\ = 265\text{ns/V}$$

Assuming that the peak-to-peak value of the superposed noise (N) is six times as great as that of the effective value, the peak-to-peak value of the fluctuation amount ΔT is expressed as follows:

$$\Delta T_{p-p} = 265 \times 0.01 \times 6 = 16\text{ns}$$

That is, caused by the noise (N), the jitter detecting accuracy cannot be below 16nsec.

In addition, as shown in Fig. 14, a detecting level may fluctuate from (A) to (B). The fluctuation of the detecting level causes the jitter detecting accuracy to fluctuate to a great extent. In order to limit the fluctuation amount $\Delta T'$ to below 20nsec, it is necessary that the fluctuation amount of a detecting level does not exceed 50mV, which results in a great increase of the cost of a detecting level generating circuit. In this respect, such a method for generating a jitter detecting signal is not preferable.

The fluctuation of a detecting level occurs also due to the fluctuation of a clamp level and the amplitude fluctuation of a video signal.

The above approximated value of the fluctuation amount is obtained from a VTR having an accurately constructed circuit. However, the fluctuation amount ΔT may be as great as 100nsec in home a VTR.

Thus, the generation of a jitter detecting signal in accordance with the rise or fall of a horizontal synchronizing signal gives rise to the problem that a jitter cannot be detected with a high accuracy.

As a means for solving this problem, the following method is considered: The phase of a frequency modulation carrier is controlled so that it becomes 0° or 180° for every horizontal period.

However, the following problem arises if this method is carried out.

That is, normally, as shown by (B) in Fig. 17, the phase of the frequency modulation carrier is discontinuous before and after a point at which the phase of the frequency modulation carrier is reset.

When a signal recorded with the phase of the frequency modulation carrier discontinuous is reproduced, as shown by (C) in Fig. 17, a level change (defect) occurs in the reproduced video signal in the shape of a sawtooth at the point corresponding to the discontinuous point of the frequency modulation carrier phase.

Thus, such a fluctuation of the frequency-demodulated output causes a large amount of a demodulation error at this point.

The clamp system of a reproduced video signal employed in a home video is a sync chip clamp system. Therefore, the defect of the sync chip may cause a clamp error, which causes a defective detection of a synchronizing signal and the change of the luminance level of the reproduced output signal.

SUMMARY OF THE INVENTION

The present invention has been made with a view to substantially solving the above-described disadvantages and has for its object to provide an improved jitter detecting method for detecting a jitter generated in a reproduced video signal of a VTR.

It is another object of the present invention to provide a jitter detecting apparatus, for detecting a jitter generated in a reproduced video signal of the VTR, capable of removing a demodulation error caused by the reset of a frequency modulation (hereinafter referred to as FM) carrier.

The method for detecting a jitter generated in a video signal recorded and reproduced by multiplying a luminance signal and a chrominance signal on the time bases thereof comprises the steps of recording a video signal by synchronizing the phase of the leading edge of a horizontal synchronizing signal with the phase of a frequency modulation carrier corresponding to a synchronizing peak-to-peak value for every horizontal period at the time of a frequency modulation; and detecting a jitter generated in a reproduced video signal by detecting a specific zero crossing point of a narrow-band FM carrier based on the trailing edge of a frequency-demodulated horizontal synchronizing signal at the time of a reproduction.

A jitter detecting apparatus in accordance with the present invention for detecting a jitter generated in a video signal recorded and reproduced

by performing the time division multiplex or the frequency division multiplex of a luminance signal and a chrominance signal wherein: a frequency modulation recording is performed by synchronizing the phase of the leading edge of a horizontal synchronizing signal or a phase in the vicinity thereof with the phase of a frequency modulation carrier for every horizontal period; and a phase-continuous compensating signal for suppressing the fluctuation of the frequency modulation carrier is inserted into the front porch of the horizontal synchronizing signal when the phase thereof is synchronized with the phase of the horizontal synchronizing signal at the time of a frequency modulation; and the jitter of the reproduced video signal is detected by detecting specific zero crossing point of a narrow-band frequency modulation carrier based on the trailing edge of a frequency-demodulated horizontal signal at the time of a reproduction.

The first feature of the present invention is that the FM carrier is used as a signal which corresponds to a burst signal.

Thus, the FM of a video signal is recorded by synchronizing the phase of the leading edge of a horizontal synchronizing signal or the phase of the horizontal synchronizing signal in the vicinity thereof with the phase of an FM carrier for every horizontal period. That is, the FM carrier is reset at the leading edge of the horizontal synchronizing signal or in the vicinity thereof for every horizontal period.

The second feature of the present invention is that at the time of a reproduction, a delay pulse for detecting a zero crossing point is generated by the trailing edge of the horizontal synchronizing signal.

The trailing edge of a demodulated horizontal synchronizing signal is hardly affected by the fluctuation of the phase of the FM carrier. Thus, the period of a synchronizing jitter is reduced to much less than 1/2 period (150nsec. for 3.4MHz FM carrier). Consequently, the specific zero crossing point of the FM carrier can be accurately detected by a gate circuit in which a delay pulse is generated.

The third feature of the present invention is that a jitter is detected using an FM carrier which has passed a narrow-band filter (BPF).

The C/N of the FM carrier which has passed the narrow-band filter becomes high. Therefore, the fluctuation amount of a time base is reduced to a great extent. Further, no offset errors occur because no direct current components are removed, so that a generated jitter can be detected with a high accuracy.

The fourth feature of the present invention is that a phase continuous compensating signal is inserted into the front porch of a horizontal synchronizing signal.

The phase continuous compensating signal prevents the phase of an FM carrier from being discontinuous when the FM carrier is reset. The value (level) of the phase continuous compensating signal is controlled depending on video signals.

A demodulation error does not occur in a horizontal synchronizing signal because the carrier phase is continuous at the time of a reset.

In addition to the above-described jitter detecting apparatus and the method therefor, the jitter detecting method of the present invention further comprises the steps of recording a video signal by synchronizing the phase of the leading edge of a horizontal synchronizing signal with the phase of an FM carrier corresponding to a synchronizing peak-to-peak value for every period after substituting part or all of the horizontal blanking period including a positive polarity synchronization of the video signal by a negative polarity horizontal synchronizing signal; and at the time of a reproduction, gating the FM carrier corresponding to a sync chip as a reference burst by a frequency-demodulated horizontal synchronizing signal; passing the FM carrier through a noise removing bandpass filter; detecting with a high accuracy the time base error of a reproduced video signal by extracting a specific zero crossing point corresponding to the trailing edge of the horizontal synchronizing signal therefrom.

In order to perform the above-described jitter detecting method, the time base error detecting/correcting method comprises the steps of substituting part or all of the blanking period of a video signal including a horizontal synchronizing signal such as a MUSE signal buried (positive polarity) within the video signal by a projecting (negative polarity) horizontal synchronizing signal such as a standard television signal before the video signal is recorded in a VTR so as to detect and correct a time base error; resetting the FM carrier phase corresponding to the leading edge of the substituted horizontal synchronizing signal, namely, the phase of the peak-to-peak value of the carrier corresponding to a sync chip to a constant value when a frequency modulation is performed to record the video signal in a recording medium; and at the time of a reproduction, gating the FM carrier corresponding to the sync chip of a reproduced FM carrier by the frequency-demodulated horizontal synchronizing signal; and detecting a time error signal using the burst carrier present in the portion corresponding to the sync chip of the reproduced FM carrier as a reference burst at the time of a reproduction.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A and 1B are schematic flow diagrams of examples showing recording circuits for achieving a jitter detecting device and the method therefor for detecting a jitter of a video signal in accordance with the present invention;

Fig. 2 is a schematic flow diagram of an example of a reproducing circuit showing a jitter detecting apparatus for detecting a jitter of a video signal in accordance with the present invention;

Fig. 3 is a schematic flow diagram showing an example of a time base correcting device;

Fig. 4 is a waveform chart related with a phase continuous compensating signal;

Figs. 5 through 8 waveform charts for describing the operation performed when the phase continuous compensating signal is inserted;

Fig. 9 shows waveforms for describing a pre-emphasizing processing;

Fig. 10 is a connection diagram of an emphasizing circuit;

Fig. 11 is a schematic flow diagram of a jitter detecting circuit;

Fig. 12 is an explanatory drawing for describing the operation of the jitter detecting circuit shown in Fig. 11;

Fig. 13 is an explanatory drawing for describing the format of a video signal using MTCI system;

Figs. 14 and 15 are explanatory drawings for explaining synchronizing jitters;

Figs. 16 and 17 are explanatory drawings for describing operations of an FM carrier reset system;

Fig. 18 is a block diagram of a video tape recorder for performing a time base error detection/correction in accordance with the present invention;

Fig. 19 is a timing chart showing the waveforms of the respective portions shown in Fig. 18;

Fig. 20 is a block diagram showing an example of a time base error correcting circuit;

Fig. 21(a) shows an allocation of one horizontal line of a MUSE signal; and

Fig. 21(b) is a view showing an HD waveform within the HD period of the MUSE signal.

DESCRIPTION OF THE PREFERRED EMBODIMENT

First embodiment

The description of a jitter detecting apparatus for detecting a jitter generated in a video signal in accordance with the present invention is made by applying it to a VTR which records and reproduces the video signal in accordance with the TCI (Time Compressed Integration) with reference to Fig. 1 through Fig. 17.

For conveniences' sake, a time base correcting device including a jitter detecting system is described referring to Fig. 3.

A horizontal synchronizing signal of composite synchronizing signals outputted from a reference synchronizing disk 31 is compared with a horizontal synchronizing signal reproduced in a horizontal phase comparing circuit 33. A vertical synchronizing signal outputted from the reference synchronizing disk 31 is compared with a vertical synchronizing signal reproduced in a vertical phase comparing circuit 34.

Error signals obtained in the horizontal phase comparing circuit 33 and the vertical phase comparing circuit 34 are supplied to a capstan servo system 35 and a drum servo 36, provided in a recording/reproducing circuit 10, in which capstan servo and drum servo controls are effected.

The frequency of a reproduced video signal is demodulated in a demodulator 32. The frequency-demodulated output is supplied both to an A/D converter 42 constituting a time base correcting circuit (TBC) 40 and to a jitter detecting circuit 20 in which a jitter generated in the video signal is detected. A jitter detecting signal is utilized as a trigger signal of a write clock generating circuit 41, and the phase of a write clock is reset in synchronization with the fall of the jitter detecting signal.

The write clock is used as a sampling signal in the A/D converter 42 and also as a write address signal in a digital memory 43. Accordingly, the reproduced video signal is written by the digital memory 43 with a jitter generating therein.

A reference clock outputted from the reference synchronizing disk 31 is supplied to a readout clock generating circuit 44 in which a readout address signal is generated and the video signal is read out in synchronization of the clock of the readout address signal. The readout video signal is converted into an analog signal in a D/A converter 45 to which the clock of the readout address signal has been supplied.

Since the readout clock is generated in a constant period, a video signal which does not fluctuate on the time base is reproduced. That is, a jitter-corrected video signal is reproduced.

According to a jitter detecting apparatus of the present invention, a video signal is recorded and

reproduced by multiplying a luminance signal and a chrominance signal on the time bases thereof and by synchronizing the phase of the leading edge of a horizontal synchronizing signal or phases of the horizontal synchronizing signal in the vicinity of the phase of the leading edge thereof with the phase of an FM carrier corresponding to a synchronizing peak-to-peak value for every horizontal period. Thus, the FM carrier is reset at the leading edge of the horizontal synchronizing signal or in the vicinity of the leading edge thereof for every one horizontal line.

The discontinuity of the phase generated before and after a point when an FM carrier is forcibly reset is removed by a phase continuous compensating signal inserted into the front porch of the horizontal synchronizing signal.

At a reproduction time, a jitter of a reproduced video signal is detected by detecting a specific zero crossing point in a narrow-band FM carrier based on the trailing edge of the frequency-demodulated horizontal synchronizing signal.

The phase of the write clock of the digital memory 43 is reset by the jitter detecting signal. Accordingly, the reproduced video signal is sampled and written by the writing clock which fluctuates in synchronization with the reproduced video signal. Thereafter, using the readout clock which is constant on the time base, video signals are sequentially read out in pixels, whereby a jitter-corrected video signal can be obtained.

Fig. 1A and Fig. 1B show examples of such a jitter detecting device for detecting a jitter generated in a video signal. In the signal recording system of this jitter detecting apparatus, a signal processing serving as the criterion for detecting a jitter is performed.

Fig. 1A shows an example of recording circuit 10A1 of the above-described recording/reproducing circuit 10.

A video signal to be inputted to a terminal 11 includes no jitters. The shape of the signal is an MTCI signal formed by compressing a line sequential system-component chrominance signal on the time base which is multiplied by a luminance signal.

The frequency of the inputted video signal shown by (A) in Fig. 16 is modulated by an FM modulator 12. In consideration of the possible degradation of the S/N of the inputted video signal, the horizontal synchronizing frequency is stabilized in an automatic frequency control (AFC) circuit 13 in this recording/reproducing circuit 10, whereby the value of the jitter which has been generated at the leading edge of the horizontal synchronizing signal does not exceed a predetermined value (5nsec in this example).

A horizontal synchronizing signal outputted

from the AFC circuit 13 is supplied to a reset pulse generating circuit 14 in which a reset pulse ((h) shown by (B) in Fig. 16) synchronized with the leading edge of the horizontal synchronizing signal is produced.

The FM carrier is reset by the reset pulse (h). That is, the FM carrier frequency corresponding to the synchronizing peak-to-peak value corresponding to the leading edge of the horizontal synchronizing signal is reset. Thus, the rise portion of the horizontal synchronizing signal is synchronized with the phase of the FM carrier.

Normally, in a magnetic recording, low carrier wave FM system is adopted and a carrier wave generating portion is integrally formed with the FM modulation portion, so that these portions cannot be distinguished from each other. Thus, the information of the phase of the FM carrier modulated by a video signal (g) is lost within the effective scanning period of an image because the frequency of the video signal is modulated. Therefore, it is necessary to add the phase information to every horizontal period. To this end, the FM carrier is reset by the reset pulse (h) for every horizontal period.

The FM carrier frequency corresponding to the synchronizing peak-to-peak value varies with the recording systems of VTRs. For example, in a VTR employing very high frequency (VHS) system, the frequency of the FM carrier frequency corresponding to the synchronizing peak-to-peak value is 3.4 MHz (5.4 MHz in a high resolution system).

As shown by (D) in Fig. 12, when the detection of a zero crossing point is performed in an operation for detecting a jitter phase, the FM carrier may be reset at an angle of 0° or 180° .

As a result, an FM signal (i) shown by (C) in Fig. 16 is obtained from the FM modulator 12. The FM signal (i) is supplied to and recorded by a rotary magnetic head 17 through a recording amplifier 16.

Fig. 1B shows another example of the recording circuit 10A2 of the above-described recording/reproducing circuit 10 which constitutes part of the jitter detecting apparatus.

A video signal which includes no jitters are inputted to an input terminal 50.

The shape of the video signal inputted to the input terminal 50 is an MTCI signal generated by compressing line-sequential chrominance components on the time base which is multiplied by a luminance signal.

Considering that the S/N of the frequency of the inputted video signal degrades, a video signal whose horizontal synchronizing frequency has been stabilized is supplied to the input terminal 50, whereby the value of jitter generated at the leading edge of a horizontal synchronizing signal is kept

below a predetermined value (5nsec. in this example).

The inputted video signal is supplied to a low-pass filter 54 in which a noise component outside the transmission band is removed. Thereafter, the inputted video signal is clamped to have a predetermined level (pedestal level in this example) by a clamp circuit 55.

A phase continuous compensating signal (s) to be described later is inserted into and added to the clamped video signal in a phase continuous compensating circuit 60 which is the principal portion of the jitter detecting apparatus of the present invention. Thereafter, a high-band emphasizing is effected in a pre-emphasizing circuit 56.

The video signal whose frequency characteristic has been corrected is inputted to an FM modulator 57 for modulating its frequency. The frequency-modulated video signal is supplied to a magnetic head 59 through an amplifier 58 in which the frequency-modulated video signal is recorded. As a result, an FM signal (i) shown by (C) in Fig. 16 is obtained from the FM modulator 57.

The FM carrier frequency varies with the recording systems of VTRs. For example, in a VTR employing VHS system, the frequency of the FM carrier corresponding to the synchronizing peak-to-peak value is 3.4 MHz (5.4 MHz in a high resolution system (S-VHS system)).

The video signal inputted to the input terminal 50 is also supplied to a reference signal generating circuit 70 from which three reference signals (h), (p), and (q) are outputted.

The third reference signal (h) of these three reference signals is used as the reset pulse (refer to Fig. 16, (B)) of the FM carrier, whereby the fall portion of the horizontal synchronizing signal is synchronized with the phase of the FM carrier.

The FM carrier frequency corresponding to the synchronizing peak-to-peak value corresponding to the leading edge of the horizontal synchronizing signal is reset by the reset pulse (h).

The reset pulse (h) can be produced in synchronization with the leading edge of the horizontal synchronizing signal. The reset pulse (h) can be also produced with a predetermined period of time later than the leading edge. The description on the reset pulse (h) is made referring to the latter.

The phase continuous compensating circuit 60 is provided with the recording circuit 10 so as to remove the discontinuity of the phase of the FM carrier generated at a phase reset point. To this end, the phase continuous compensating signal (s) is inserted into the video signal inputted to the recording circuit 10. As shown in Fig. 4, the phase continuous compensating signal (s) having a predetermined level is inserted into the front porch of the horizontal synchronizing signal in a predeter-

mined period of time.

The frequency of the FM carrier is deviated by the phase continuous compensating signal (s). Therefore, the phases of the FM carrier at a phase reset point before and after the insertion of the phase continuous compensating signal (s) differs from each other.

The phase (shown by (B) in Fig. 4) at a phase reset point of the FM carrier before the insertion of the phase continuous compensating signal (s) varies depending on the level of a video signal inputted immediately before the insertion of the phase continuous compensating signal (s). When the phase continuous compensating signal (s) is inserted into the front porch of the horizontal synchronizing signal in this state, the phase of the FM carrier at the phase reset point is changed by the phase continuous compensating signal (s) as well (shown by (B) in Fig. 4).

It is possible to assume how the phase of the FM carrier at the phase reset point is changed by the insertion of the phase continuous compensating signal (s).

Thus, the phase of the FM carrier at the phase reset point can be changed to 0°, 180° or in the vicinity thereof by setting the level of the phase continuous compensating signal (s) for every one line depending on the level of a video signal inputted immediately before the insertion of the phase continuous compensating signal (s).

As a result, the phase of the FM carrier at the phase reset point becomes continuous by inserting the phase continuous compensation signal (s). Even if the phase of the FM carrier is discontinuous, the degree of the discontinuity of the phase of the FM carrier is slight.

The phase of the FM carrier is reset for every one line is for the following reason:

Normally, in a magnetic recording, low carrier wave FM system is adopted and a carrier wave generating portion is integrally formed with the FM modulation portion, so that these portions cannot be distinguished from each other. Thus, the phase information of the FM carrier modulated by a video signal (g) is lost within the effective scanning period of an image because the FM of the video signal is modulated. Therefore, it is necessary to add the phase information to every horizontal period. To this end, the FM carrier is reset by the reset pulse (h) for every horizontal period.

Considering the above-described fact, the phase continuous compensating circuit 60 is constructed as follows:

The video signal clamped at the pedestal level is first supplied to a front porch expansion circuit 61 provided as necessary.

This is because there is a case in which the phase continuous compensating circuit 60 does not

allow the front porch provided at the front stage of the horizontal synchronizing signal to have a length (approximately $2.2\mu\text{sec.}$ in NTSC) enough to insert the phase continuous compensating signal (s) into the front porch expansion circuit 61.

The expansion circuit 61 is used in this embodiment.

The front porch is expanded by the following two methods: One of them is to remove a part of the latter portion of a luminance signal present immediately before the front porch (refer to Fig. 5.) The other one is to displace a horizontal synchronizing signal by substituting it by another horizontal synchronizing signal (refer to Fig. 6.)

Referring to Fig. 5, a first reference signal (p) generated by a reference signal generating circuit 70 is supplied to the front porch expansion circuit 61. The reference signal (p) functions as a blanking pulse which blanks the latter portion of inputted video signals as shown by (A) and (B) in Fig. 5.

As a result, a video signal (shown by (C) in Fig. 5) whose front porch is wider than the standard width is outputted from the front porch expansion circuit 61.

Fig. 6 shows the above-described latter case of expanding the front porch, namely, the case in which the horizontal synchronizing signal is displaced by substituting it with another horizontal synchronizing signal. The reference signal (p) also functions as a blanking pulse in this case. However, as shown by (A) and (B) in Fig. 6, the generation timing of the reference signal (p) is near the sync chip (fall timing) of the horizontal synchronizing signal and set to have a predetermined pulse including the fall portion.

Part of the horizontal synchronizing signal is removed by the reference signal (p) and a new horizontal synchronizing signal (shown by (C) in Fig. 6) substitutes the horizontal synchronizing signal which has been partly removed. As a result, similarly to Fig. 5, a video signal whose front porch has become wide is outputted from the front porch expansion circuit 61.

The output of the front porch expansion circuit 61 and the phase continuous compensating signal (s) are added to each other in an adder 62. The phase continuous compensating signal (s) is generated as follows:

First, the phase of the FM carrier at a specific point is detected. The specific point is referred to as a point corresponding to the undershoot portion of a video signal generated when the video signal is pre-emphasized.

As shown by (D) through (F) in Fig. 5 and (E) through (G) in Fig. 6, the second reference signal (q) is supplied to a carrier phase difference detecting circuit 65 in which a phase difference $\Delta\theta$ (phase

the FM carrier) at a point at which the second reference signal (q) has been obtained is detected.

The phase difference detecting output (shown by (G) in Fig. 5 and (H) in Fig. 6) is supplied to a compensation signal generating circuit 64 in which the level of the pulse output (s) in a trapezoidal waveform is modulated depending on a detected phase difference (shown by (H) in Fig. 5 and (I) in Fig. 6).

The frequency deviation amount of the output pulse (s) differs depending on the magnitude of its level, which differentiates the phase at a phase reset point.

An assumption output (DC level) is also supplied from a phase shift assumption circuit 63 to the compensation signal generating circuit 64.

An assumption output in accordance with the undershoot of the video signal at the specific point is generated in the phase shift assumption circuit 63 in this example.

Accordingly, the phase shift assumption circuit 63 comprises an emphasizing circuit (not shown) having the same frequency characteristic as that of the emphasizing circuit 56 and a sampling hold circuit (not shown) which holds the sampling output, at the undershoot portion, to which the emphasizing characteristic has been applied.

Since the output (SH) of the sampling hold circuit is proportional to the undershoot amount, the output (SH) is utilized as the output by which the amount of a phase shift is assumed. The assumption output is added to the phase difference detecting output and the resulting output is superposed on a video signal inputted to the recording circuit 10 as the phase continuous compensating signal (s) (shown by (I) in Fig. 5 and (J) in Fig. 6).

Thus, the frequency of the FM carrier is deviated by a signal obtained by adding the assumption output (DC level) proportional to the undershoot of the video signal to a pulse output having a level corresponding to the phase difference of the FM carrier, namely, by utilizing the phase continuous compensating signal (s). The adjustment of the level of the phase continuous compensating signal (s) according to the content of the video signal allows the phase of the FM carrier at the phase reset point to be set to 0° or 180° and the phase of the FM carrier to be continuous when a phase reset is performed.

Even if the phase of the FM carrier cannot be made to be completely continuous, the phase difference at the phase reset point can be made to be slight.

The output (x) of the pre-emphasizing circuit 56 is shown by (K) in Fig. 6 and the reset pulse (h) is shown by (L) in Fig. 6. The reset pulse (h) is obtained a predetermined period of time after the peak-to-peak value of the leading edge of the hori-

zontal synchronizing signal is obtained. The predetermined period of time is $1\mu\text{sec}$. in this example.

It seems that only a pulse output corresponding to the phase difference of the FM carrier at the specific point is enough to function as the phase continuous compensating signal (s), but the continuity of the phase of the FM carrier at the phase reset point cannot be sufficiently held by the pulse output only.

This is because as shown in Fig. 7, even when the detecting outputs of the phase difference $\Delta\theta_s$ at the specific point (point (A)) are the same, the phase shift amounts at the phase reset point at that time are not constant.

That is, the phase differences of the inputted video signals shown by (B), (D), and (F) in Fig. 7 at the point (A) are constant ((C), (E), and (G) in Fig. 7). However, even when the phase differences at the point (A) is the same, the phase shift amounts fluctuate in a great extent according to the undershoot amount at the point (A).

Thus, unless the undershoot amounts at the specific point are considered, the frequency deviation amounts are all the same in either case: The continuity of the phase at the phase reset point cannot be ensured.

Contrary to the above, frequency deviation amounts can be varied with the undershoot amounts by considering the undershoot amounts at the specific point. Thus, the phase of FM carrier can be controlled so that it is continuous at the phase reset point by setting the levels of the sampling hold output (SH) and the level of the pulse output at desired levels.

Fig. 2 shows an example of a video signal reproducing circuit 10B.

An FM video signal (i) (shown by (A) in Fig. 8) reproduced by a rotary magnetic head 17 is supplied to an FM modulator 32 through a pre-amplifier 18 and a carrier gate circuit 22 constituting a jitter detecting circuit 20.

A video signal (j) (refer to (B) in Fig. 8) demodulated by an FM demodulator 32 is supplied to a time base correcting circuit 40 as an input video signal having a jitter component and also supplied to a synchronizing separating circuit 21 by which a horizontal synchronizing signal is extracted and separated from the video signal (j). Thereafter, the video signal (j) is supplied to a delay circuit 26.

The delay circuit 26 functions to obtain the phase reset point (shown by (L) in Fig. 6) of the FM carrier. A horizontal synchronizing signal (k) delayed a predetermined period of time ($1\mu\text{sec}$) is shown by (C) in Fig. 6.

The horizontal synchronizing signal (k) delayed the predetermined period of time is supplied to a carrier gate 22 as a gate signal by which the FM

carrier (carrier corresponding to the horizontal synchronizing peak-to-peak value) present between horizontal synchronizing signals is gated (shown by (D) in Fig. 6). The gated FM carrier (l) is used as a burst signal similarly to a conventional method.

The FM carrier (l) is supplied to narrow-band pass filter 23 in which the C/N thereof is improved. When 3.4MHz is selected as the frequency of the FM carrier of the horizontal synchronizing peak-to-peak value, a filter of $3.4\text{MHz} \pm 0.1\text{MHz}$ is used as a passband.

Using such a narrow-band filter, the level (effective value) of noise which has mixed with the FM carrier is reduced below $1/4$. As a result, the value of a synchronizing jitter (fluctuation of time base) which has mixed with the FM carrier is reduced below $1/4$.

For example, when the value of the synchronizing jitter is approximately 16nsec . before it is processed with the filter, the value of the synchronizing jitter is reduced to approximately 4nsec . by the use of such a narrow-band pass filter. The FM carrier (m) obtained after it is processed by the filter is shown by (E) in Fig. 6.

The horizontal synchronizing signal (k) is supplied to the delay pulse generating circuit 24 in which a delay pulse (n) (shown by (F) in Fig. 6) with a predetermined period of time lagging behind the trailing edge of the horizontal synchronizing signal (k) is generated.

The delay pulse (n) and the FM carrier (m) processed with the filter are supplied to a jitter detecting signal generating circuit 25 which is composed of an RS flip-flop, and set by the delay pulse (n), and reset by the zero crossing point of the FM carrier (m) inputted after it is set.

Accordingly, as shown by (G) in Fig. 6, a jitter detecting signal (o) is outputted from the jitter detecting generating circuit 25 as a signal synchronized with a specific zero crossing point of the cycle of the FM carrier (m).

The specific zero crossing point is referred to as the zero crossing point of a cycle at which the amplitude of the FM carrier (m) becomes maximum. In the waveforms shown in Fig. 8, since the amplitude becomes maximum in a cycle which lags approximately $1\mu\text{s}$ behind the trailing edge of the horizontal synchronizing signal (k), the delay period of the delay pulse (n) is set to approximately $1\mu\text{s}$.

This is because the influence of noise superposed on the video signal is reduced by detecting a zero crossing point in a cycle whose C/N is high, so that a jitter can be detected with a high accuracy.

The reason the delay pulse (n) is generated based on the trailing edge of the horizontal synchronizing signal is that the influence of a carrier

leak at the time of a frequency demodulation on the horizontal synchronizing signal is much less at the trailing edge thereof than at the leading edge thereof. That is, even if there is a carrier leak, the fluctuation of the phase of the leak component is reduced and stabilized from the leading edge (reset point of phase) of the horizontal synchronizing signal toward the trailing edge thereof. Therefore, the accuracy of the delay pulse (n) is improved.

When the frequency of the FM carrier (m) is 3.4MHz, zero crossing points exist approximately every 1.47nsec. Therefore, when the value of the synchronizing jitter of the horizontal synchronizing signal (k) at the trailing edge thereof is 100nsec. at its maximum, it is possible to detect a specific zero crossing point at the accuracy below 5nsec. if the S/N ratio is approximately 40dB.

That is, the value of the residual jitter of a reproduced video signal can be suppressed below 5nsec.

The cycle of the jitter generated at the trailing edge of the carrier reset demodulated horizontal synchronizing signal cannot be more than 1/2 cycle of the FM carrier. Therefore, a malfunction that the delay pulse (n) detects zero crossing points other than a predetermined specific zero crossing point does not occur.

The object of the present invention can be achieved by synchronizing the phase of the FM carrier with that of the horizontal synchronizing signal and superposing the phase continuous compensating signal (s) on a video signal. The above-described phase control necessary for holding the continuity of the phase of the FM carrier at the phase reset point thereof is qualitatively described.

Normally, an frequency modulation wave $f(t)$ is expressed as follows:

$$f(t) = A \cos(\int (\omega_c + \omega_a v(t)) dt + \phi) \\ = A \cos(\omega_c t + \phi + \omega_a \int v(t) dt)$$

where A is amplitude; ω_c , frequency deviation; ω_a , carrier angular frequency; ϕ , initial phase; $v(t)$, modulation signal.

The above equation is a modulation system in which the fluctuation amount of a momentary angular frequency is proportional to the momentary value of a modulation signal.

The phase angle is expressed by the momentary phase angle $\phi(t)$ as follows:

$$\phi(t) = \omega_c t + \phi + \omega_a \int v(t) dt$$

where is constant.

The above equation indicates that the phase angle can be controlled by using an integration value on the time base of a modulation signal.

The carrier phase can be controlled so that the phase is continuous before and after a reset point by adding a signal (rectangular or trapezoidal wave) having an appropriate area (integration val-

ue) to the front porch of a modulation signal (input video signal).

In this case, it is necessary to consider the influence of the pre-emphasizing circuit 56. This is because when a certain waveform is inserted into a pre-emphasized input video signal without considering a de-emphasis, a horizontal synchronizing signal is distorted by the influence of the de-emphasis of the inserted waveform at the time of a reproduction.

The phase continuous compensating signal (s) is shown by (A) in Fig. 9 and the pre-emphasized waveform is shown by (B) in Fig. 9.

When the high-pass filter having the construction shown in Fig. 10 is used as the pre-emphasizing circuit 56, the transmission function $G(s)$ and the modulation signal $v(t)$ determined by the $G(s)$ are expressed as follows:

$$G(s) = \{(R_b + sCR_aR_b)/(R_a + R_b + sCR_aR_b)\} \\ (s + 1/T)/(s + (1 + X)/T) \\ v(t) = \mathcal{L}^{-1}(G(s)/s) = [u(t) + X \exp\{-(1 + X)t/T\}]/(1 + X)$$

When the edge of the waveform of the phase continuous compensating signal (s) to be inserted is regarded as a step steeper than the time constant of the pre-emphasis, the integrated value $S(t)$ (output of the emphasizing circuit provided in the assumption circuit 63) between the point $t_1 \sim t_2$, when a rectangular wave whose voltage is V is inputted between the point $t_0 \sim t_1$ shown in Fig. 9, is as follows:

$$S(t) = S_1(t) + S_2(t)$$

where $S_1(t)$ indicates the integrated value obtained by inputting a step waveform (step waveform from 0 to 1) which rises when $t = 0$.

Similarly, $S_2(t)$ indicates the integrated value obtained by inputting a step waveform (step waveform from 0 to 1) which falls when $t = 1$.

The above equation can be changed as follows:

$$S(t_2) = \{S_1(t_2) + S_2(t_2)\}V \\ = V\{t_1/(1 + X)\} - TX/(1 + X)^2\{-(1 + X)t_2/T\} - \exp\{-(1 + X)(t_2 - t_1)/T\}$$

From the above equation, t_1 and t_2 by which the value of the second term can be ignored are set. In this example, the relationship between t_1 and t_2 is expressed as follows when $X=4$, $T=1.3\mu\text{sec.}$ (home video of VHS system), and $V=1$.

$$S = t_1/5 - (T/5)(4/5)\{\exp(-5T_2/T) - \exp(-5(t_2 - t_1)/T)\}$$

The value of the second term of the above equation can be less than 1% (value which can be ignored in consideration of the accuracy in clamping) of the value of the first term by selecting the following condition: when $X = 4$, $t_1 < 1$, $t_2 = 2T$ ($> 2.3\mu\text{sec.}$). The detailed description is omitted herein.

Thus, a relatively accurate control (error is be-

low 1%) can be obtained in a short period of $t = 2T$ even if the phase continuous compensating signal (s) is inserted into the front stage of the pre-emphasizing circuit 56.

The time width T of the phase continuity compensating signal (s) controlling the phase of the FM carrier is determined by an integrated value (area) whose top side is 100% white level and which is necessary when a maximum phase difference is obtained. In this example, $T = 1.0\mu\text{sec}$.

When a VTR whose transmission band is wide such as a S-VHS is used, it is possible to determine a phase shift amount at the front porch by performing an operation after an A/D conversion of a video signal into a digital data before a recording is performed and also possible to adopt a means for inserting the phase continuous compensating signal (s) in a trapezoidal waveform based on a digital data. According to these methods, the expansion circuit 61 can be omitted from the phase continuous compensating circuit 60.

The above description is directed to the application of the jitter detecting apparatus and the method therefor of the present invention to a VTR which records and reproduces a video signal by the MTCI system. However, a jitter detecting method in accordance with the present invention may be applied to a narrow-band input video signal obtained by narrowing a carrier wave recording band and converting a chrominance signal at a low frequency and recording the frequency modulation of an input video signal.

In addition to the above, the jitter detecting apparatus and the method therefor in accordance with the present invention can be applied to a video signal for use in a high dignity television (HDTV) and a MUSE signal for use in a satellite broadcasting. In this case, before a recording is performed, a positive polarity synchronization of the MUSE signal is substituted by a negative polarity synchronization and a synchronizing peak-to-peak value is reset as a reference burst, whereby several cycles' reference burst recordings of MUSE signals are possible by the FM carrier even if the horizontal fly-back time thereof is very short. Thus, a jitter can be detected with a high accuracy.

As described above, in the first embodiment of the present invention, a video signal is recorded by synchronizing the phase of the leading edge of a horizontal synchronizing signal with the phase of an FM carrier corresponding to a phase synchronizing peak-to-peak value for every horizontal period and the jitter of a reproduced video signal is detected by detecting a specific zero crossing point of a narrow-band FM carrier based on the trailing edge of a frequency-demodulated horizontal synchronizing signal at the time of a reproduction.

Accordingly, the specific zero crossing point of

the FM carrier can be detected with a high accuracy. According to this method, the value of the residual jitter of the reproduced video signal can be reduced to $1/n$ of that conventionally detected.

This is because an FM carrier having a high C/N obtained by passing it through a narrow-band filter is used as used in the conventional manner.

Since a jitter of a signal reproduced by a VTR can be accurately detected, a phase error can be detected with a high accuracy. Therefore, a speed error accuracy which is the difference value of the phase error is improved and a speed error correction can be easily made.

In addition, according to the present invention, a demodulation error which is a disadvantage of a carrier reset system can be reliably removed.

Therefore, according to the jitter detecting method in accordance with the present invention can be very preferably applied to a recording/reproducing system of a video signal employing the TCI system.

Second Embodiment

A second embodiment of the present invention is described with reference to Figs. 18 through 22.

Fig. 18 is a block diagram showing an example of recording and reproducing a MUSE signal in accordance with the present invention. Referring to Fig. 18, a MUSE signal (a) having a short blanking period (MUSE HD period) of approximately 700nsec. is inputted to a synchronizing substituting circuit 101 in which the horizontal blanking period is substituted by a negative polarity synchronizing signal (shown by (b) in Fig. 19). This signal is frequency-modulated by an FM modulation circuit 103 (an example of an FM allocation at this time is shown on the upper right in Fig. 19.)

The FM modulation circuit 103 is of an external reset type in which the initial phase of a carrier (frequency is 8MHz in this case, but a carrier may have a frequency higher than that of the video signal as shown by a dotted line (b) in Fig. 19, for example, 13MHz) corresponding to a sync chip is reset by a reset pulse (c) to have a constant value for every horizontal period. That is, the synchronously substituted horizontal synchronizing signal is supplied to a reset pulse generating circuit 102 in which the reset pulse (c) synchronized with the leading edge of the horizontal synchronizing signal is generated.

An FM carrier phase corresponding to a synchronizing peak-to-peak value which corresponds to the leading edge of the horizontal synchronizing signal is reset by the reset pulse (c), whereby the phase of the rise portion of the horizontal synchro-

nizing signal is synchronized with the phase of the FM carrier.

The number of the cycles of the FM carrier corresponding to the horizontal synchronizing signal portion depends on an FM frequency. An FM carrier (d) of approximately nine cycles can be obtained in a horizontal blanking period of the MUSE signal as short as approximately 700nsec. and a detecting accuracy of within 5nsec. is obtained when the C/N thereof is more than 30dB at the time of a reproduction by setting the level of a synchronizing signal to be substituted to have the frequency modulation of 13MHz.

The FM signal (d) thus obtained is recorded in a VTR by a magnetic head 4.

At the time of a reproduction, an FM signal (e) reproduced by the magnetic head 4 is inputted to a frequency demodulation circuit 105 and a carrier gate circuit 107 constituting a jitter detecting circuit. A frequency-demodulated video signal (f) is supplied to a time base error correcting circuit 111 as an input video signal having a jitter component and also supplied to a synchronizing separating circuit 106 in which a horizontal synchronizing signal (g) is extracted and separated from the video signal.

The horizontal synchronizing signal (g) functions as the gate signal in the carrier gate circuit 107 and is capable of separating the FM carrier (FM carrier (h) corresponding to the horizontal synchronizing peak-to-peak value). present between horizontal synchronizing signals of the reproduced FM signal (e). The S/N of the separated FM carrier (h), namely, a reference burst can be improved by the narrow-band pass filter 110.

The frequency-demodulated video signal (f) is also supplied to a delay pulse generating circuit 108 in which a delay pulse (j) which lags a pre-determined time period behind the trailing edge of the horizontal synchronizing signal is generated. The delay pulse (j) and the FM carrier (i) which is the output from the narrow-band pass filter 110 are inputted to a jitter detecting signal generating circuit 109 constituted by an RS flip-flop from which a jitter detecting signal (k) is outputted by a specific zero crossing point of the cycle of the delay pulse (j) and the FM wave (i). The specific zero crossing points are referred to as the point at which the amplitude of the FM carrier becomes maximum.

The reason the delay pulse (j) is generated based on the trailing edge of the horizontal signal is that the influence on the horizontal synchronizing signal by the carrier leak at the time of a frequency demodulation is much less at the leading edge thereof than at the trailing edge thereof. That is, even if there is a carrier leak, the amount of the fluctuation of the phase of the leak component becomes less and the phase of the leak compo-

nent becomes stabilized from the leading edge which is the reset point of the phase toward the trailing edge. Thus, the accuracy in detecting the timing of the delay pulse can be improved.

The jitter detecting signal (k) obtained by the above-described method and the frequency-demodulated video signal (f) are supplied to the time base error correcting circuit 111 from which a jitter component-corrected video signal is outputted.

Fig. 20 shows a time base error correcting circuit.

Referring to Fig. 20, the jitter detecting signal (k) is obtained by the jitter detecting circuit 109 for every one horizontal scanning period (1H) of the reproduced video signal (f). The phase of the jitter detecting signal (k) is compared with that of a phase reference signal (Wck/n) obtained by dividing a write clock (Wck) which has been phase-locked by the reference phase into 1/n for every one horizontal scanning period (1H) in a phase lock loop 135. The reproduced video signal (f) is sampled by the write clock (Wck) through an A/D conversion circuit 131 and converted into a digital signal, and then, written in a memory 132.

The signal written in the memory 132 is read out by a stable clock (Rck), and a negative polarity synchronizing signal in the horizontal blanking period is substituted by a MUSE HD signal shown in Fig. 21(b) in a synchronizing substituting circuit 133.

As a result, an analog video signal outputted from a low-pass filter 137 through a D/A conversion circuit 134 becomes an original MUSE signal.

As described above, according to the second embodiment of the present invention, even when a video signal such as a MUSE signal which is very narrow in its horizontal blanking period and has a positive polarity synchronization is recorded and reproduced, a time base error can be detected with a high accuracy by using a video FM signal as a burst. Further, since the video FM signal becomes a high-pass frequency, the period of one cycle thereof becomes short. Thus, a reproduced video signal has few residual jitters because the time base error can be detected with a high accuracy.

Although the present invention has been fully described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications are apparent to those skilled in the art. Such changes and modifications are to be understood as included within the scope of the present invention as defined by the appended claims unless they depart therefrom.

Claims

1. A jitter detecting method, for detecting a jitter generated in a video signal recorded and reproduced by multiplying a luminance signal and a chrominance signal in the time bases thereof, comprising the steps of:

recording a frequency-modulated carrier of video signal by synchronizing the phase of the leading edge of a sync signal with the phase of the initial carrier of the constant frequency carrier corresponding to a sync tip of the video signal for every horizontal period prior to the recording;

detecting the jitter of said reproduced video signal by detecting a specific zero-cross timing of a train of the constant frequency carrier corresponding to the sync tip portion through a band pass filter (23), based on the tailing edge of a frequency-demodulated sync signal at the time of a reproduction.

2. A jitter detecting apparatus for detecting a jitter generated in a video signal recorded and reproduced by performing the time division multiplex or the frequency division multiplex of a luminance signal and a chrominance signal wherein:

a frequency modulation recording is performed by synchronizing the phase of the leading edge of a sync signal or a phase in the vicinity thereof with the phase of the initial carrier of the corresponding constant frequency carrier for every horizontal period;

a phase-continuous compensating signal for preventing the frequency-modulated carrier's phase from abruptness is inserted into the front porch of said sync signal when the phase thereof is synchronized and

a jitter of a reproduced video signal is detected by detecting a specific zero cross timing of a train of the constant frequency carrier corresponding to said sync tip portion through a narrow band pass filter, based on the tailing edge of a frequency-demodulated sync signal at the time of a reproduction.

3. A time base error detecting/correcting method comprising the steps of:

replacing part or all of the blanking period of a video signal including a sync signal with a noiseless sync signal generated in a sync generator gen-locking the input video signal before the video signal is recorded in a video tape recorder so as to detect and correct a time base error;

resetting the phase of the forefront carrier in a train of the constant frequency carrier train to a constant value at the leading edge of the replaced sync signal, when a frequency modulation is performed to record the video signal in a recording medium;

abstracting the constant frequency carrier

portion corresponding to the sync tip from a reproduced frequency modulation carrier by means of the frequency-demodulated sync signal, and

detecting a time error signal by abstracting the phase-reset carrier of a constant frequency present in the portion corresponding to the sync tip from the reproduced frequency modulation carrier as a reference burst at the time of a reproduction.

Fig. 1A

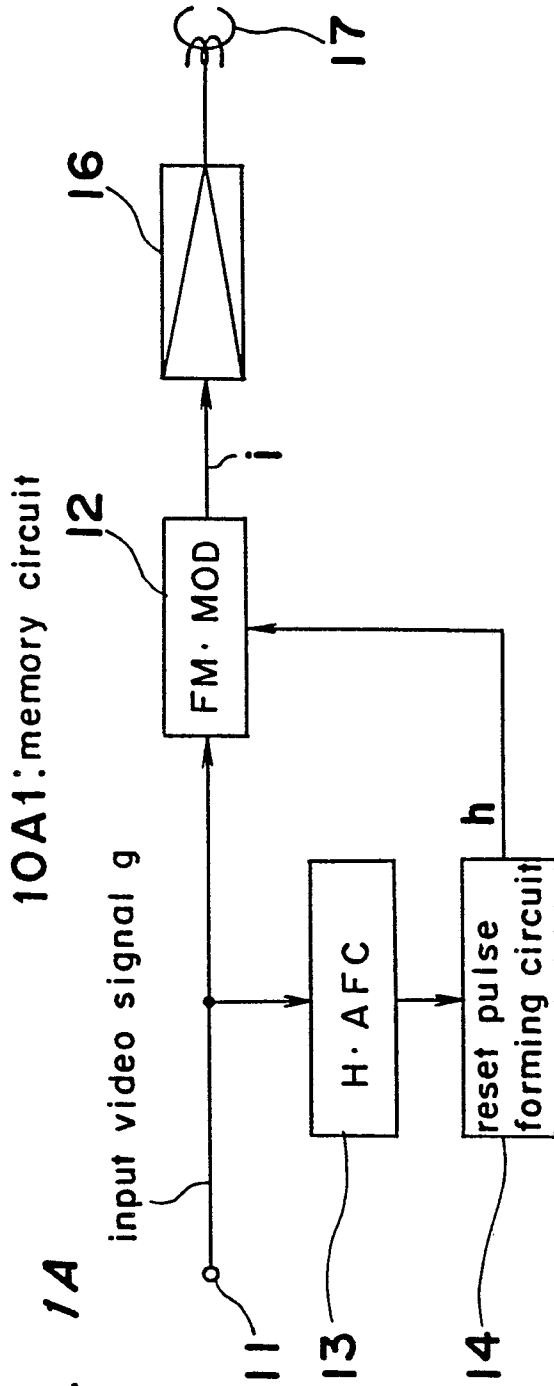


Fig. 1B

10A2:memory circuit

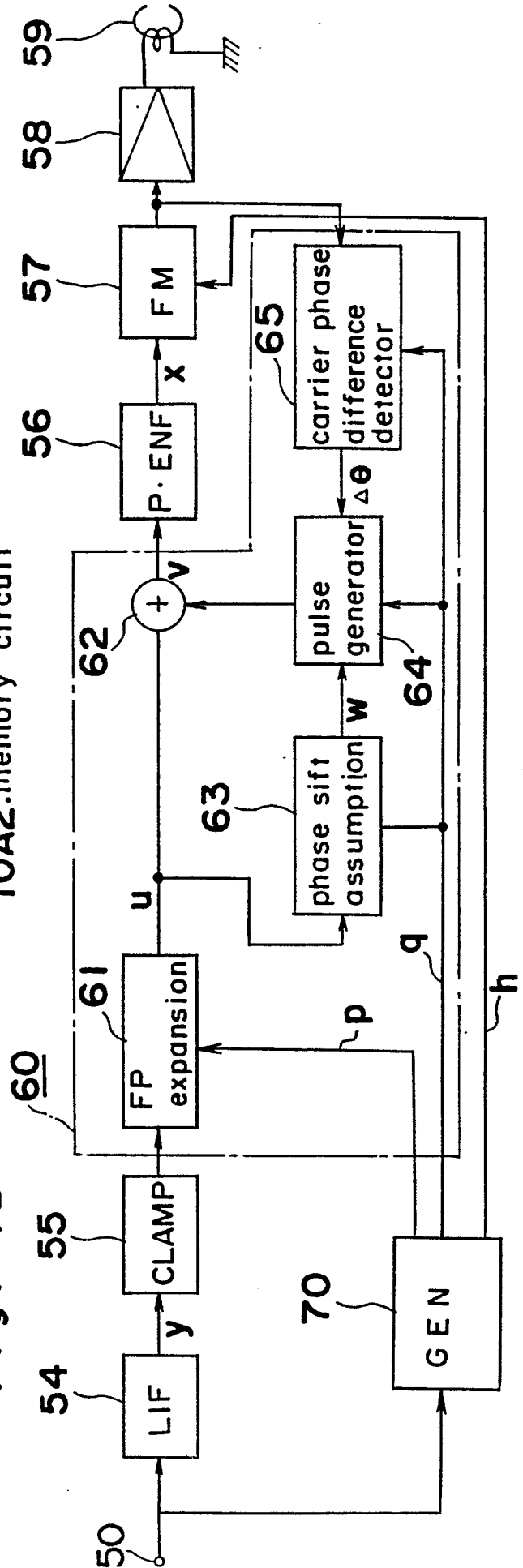
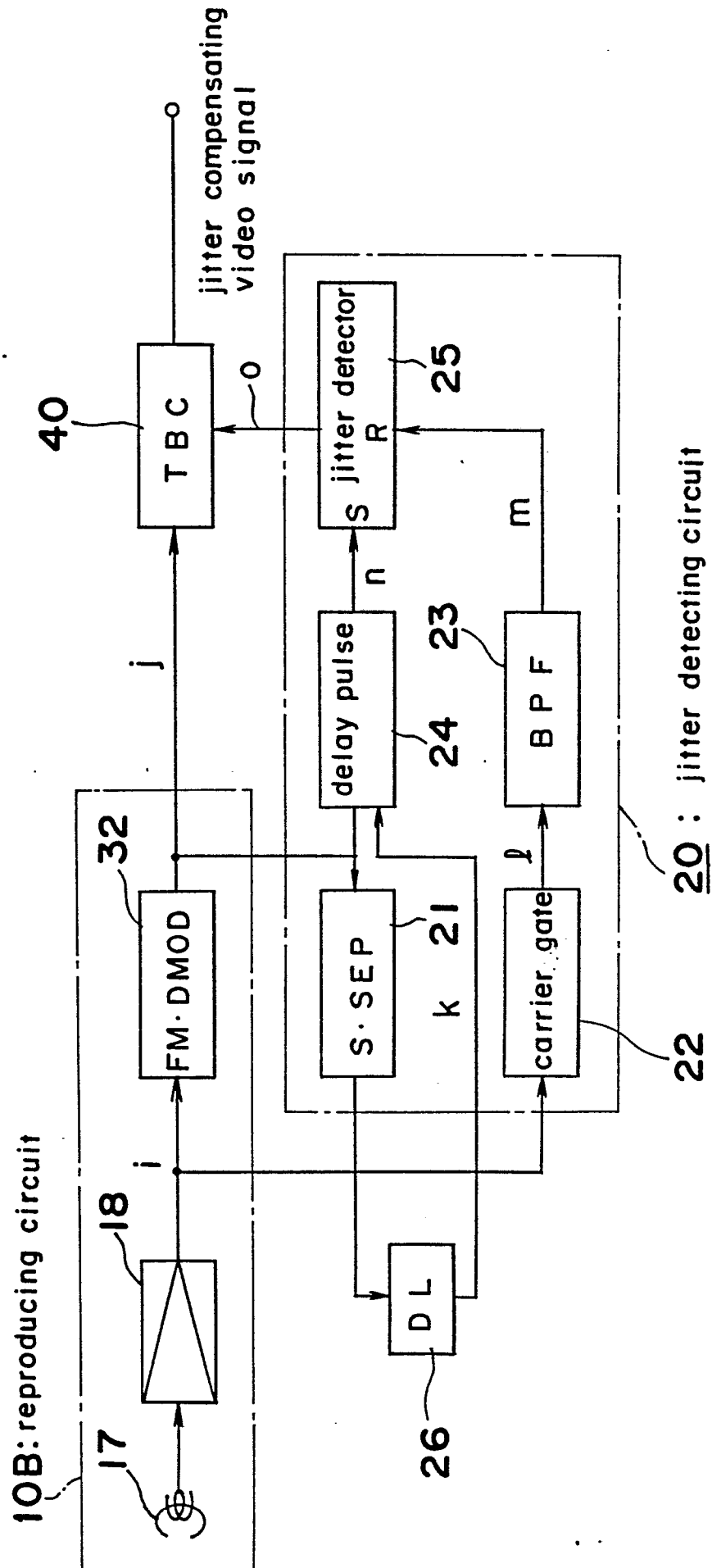


Fig. 2



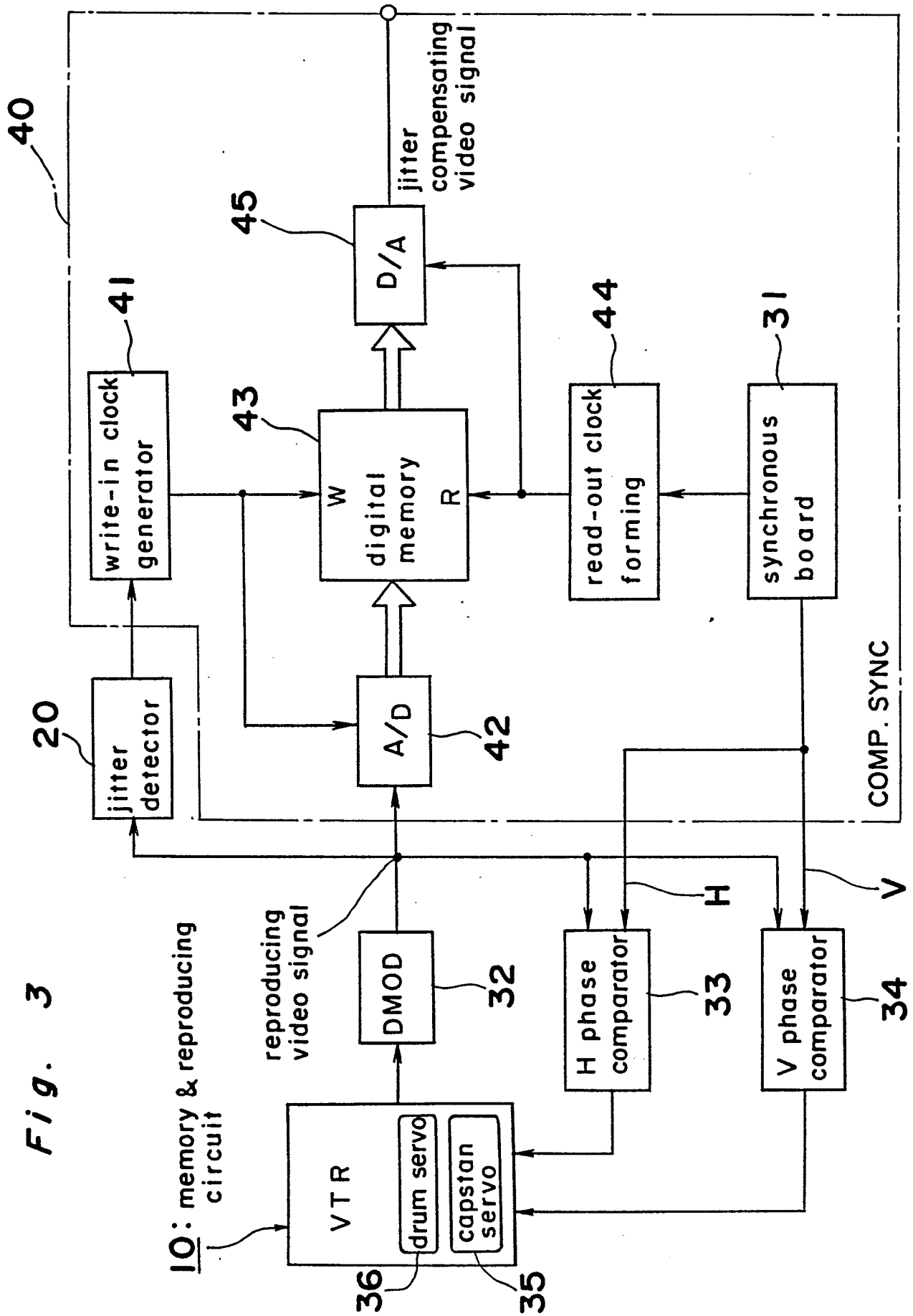


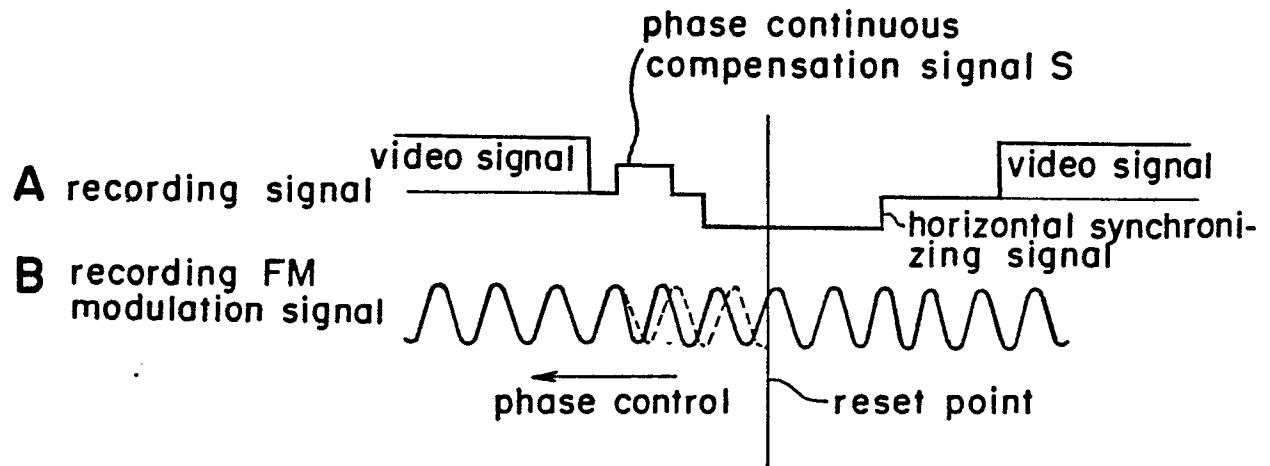
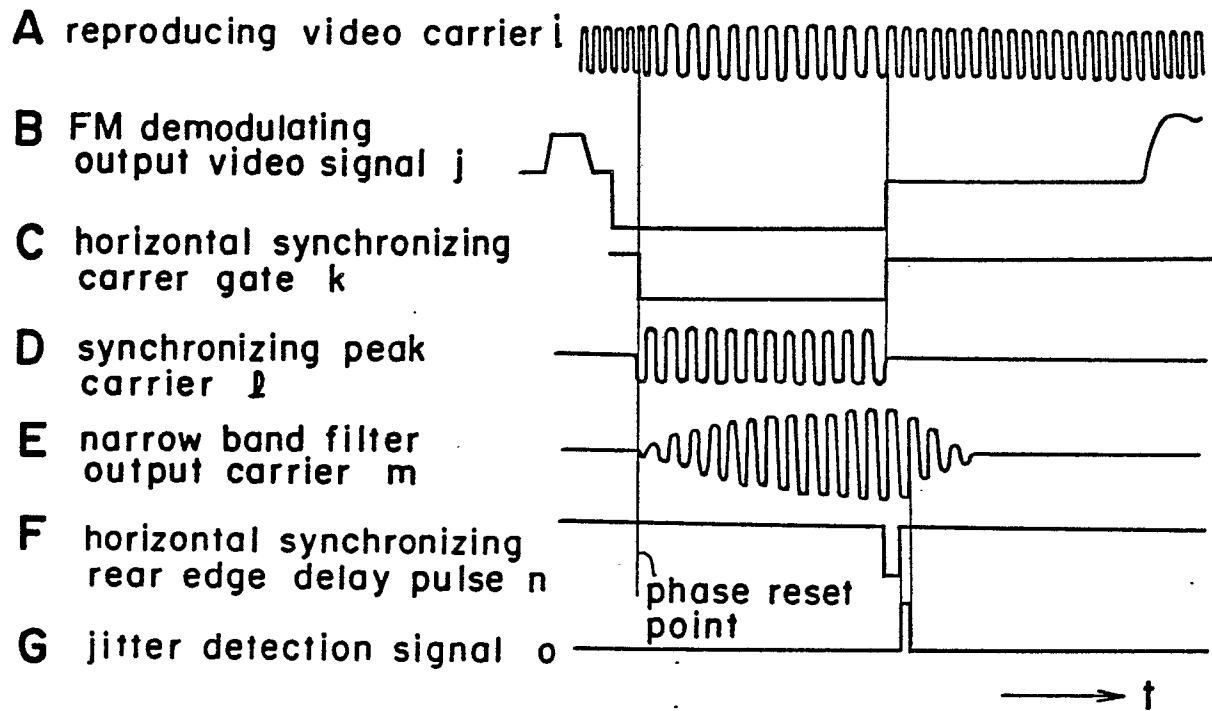
Fig. 4**Fig. 8**

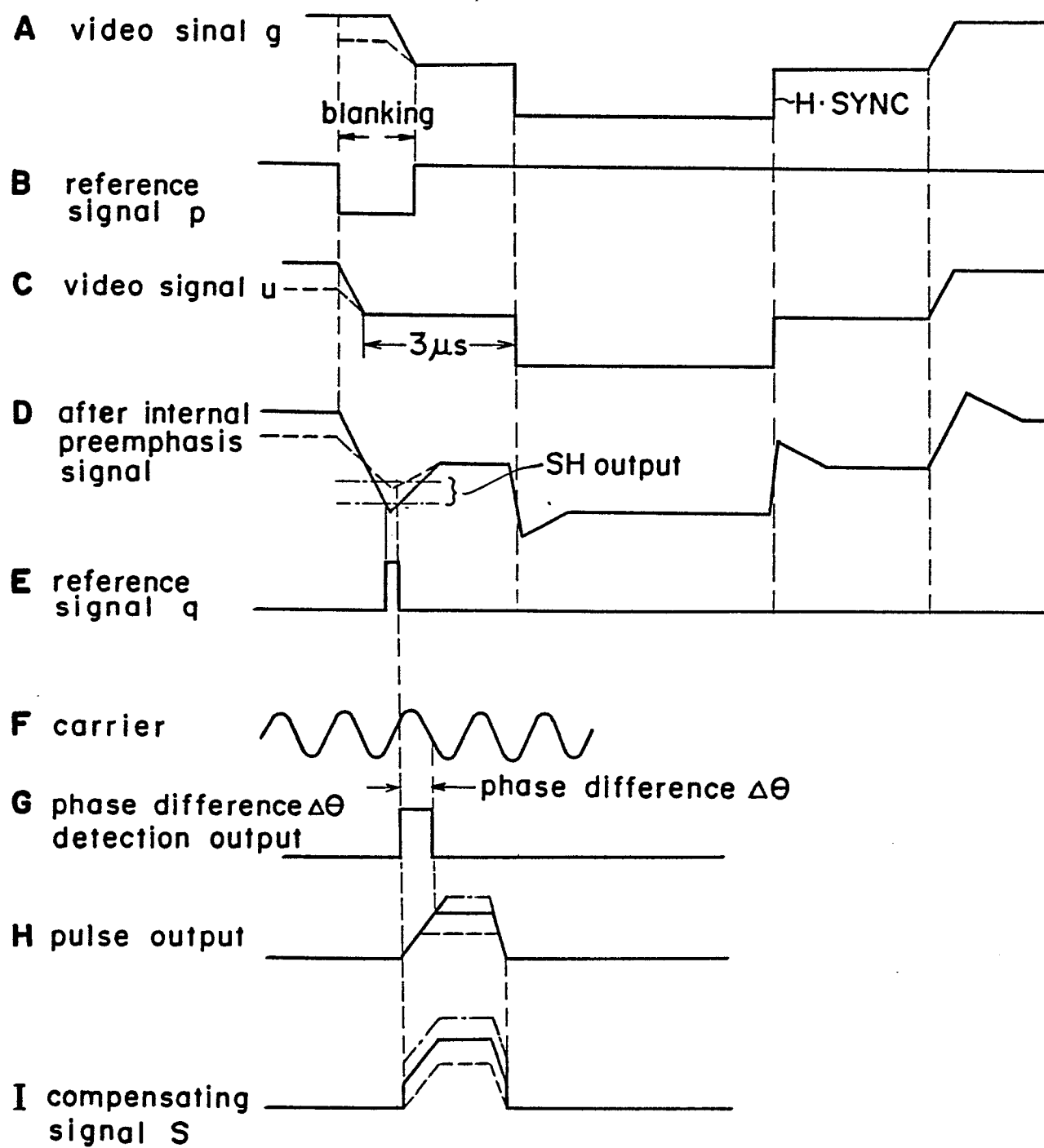
Fig. 5

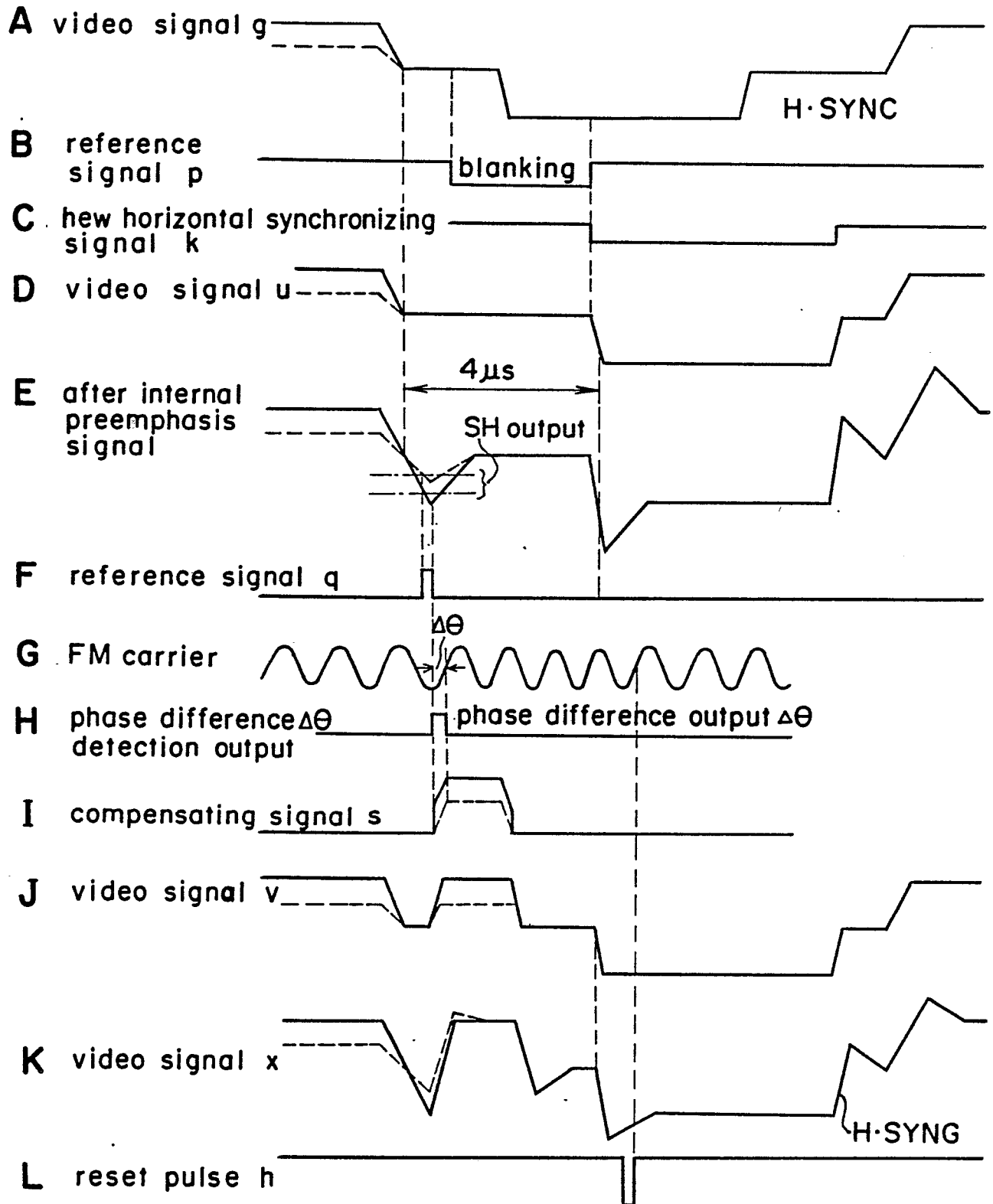
Fig. 6

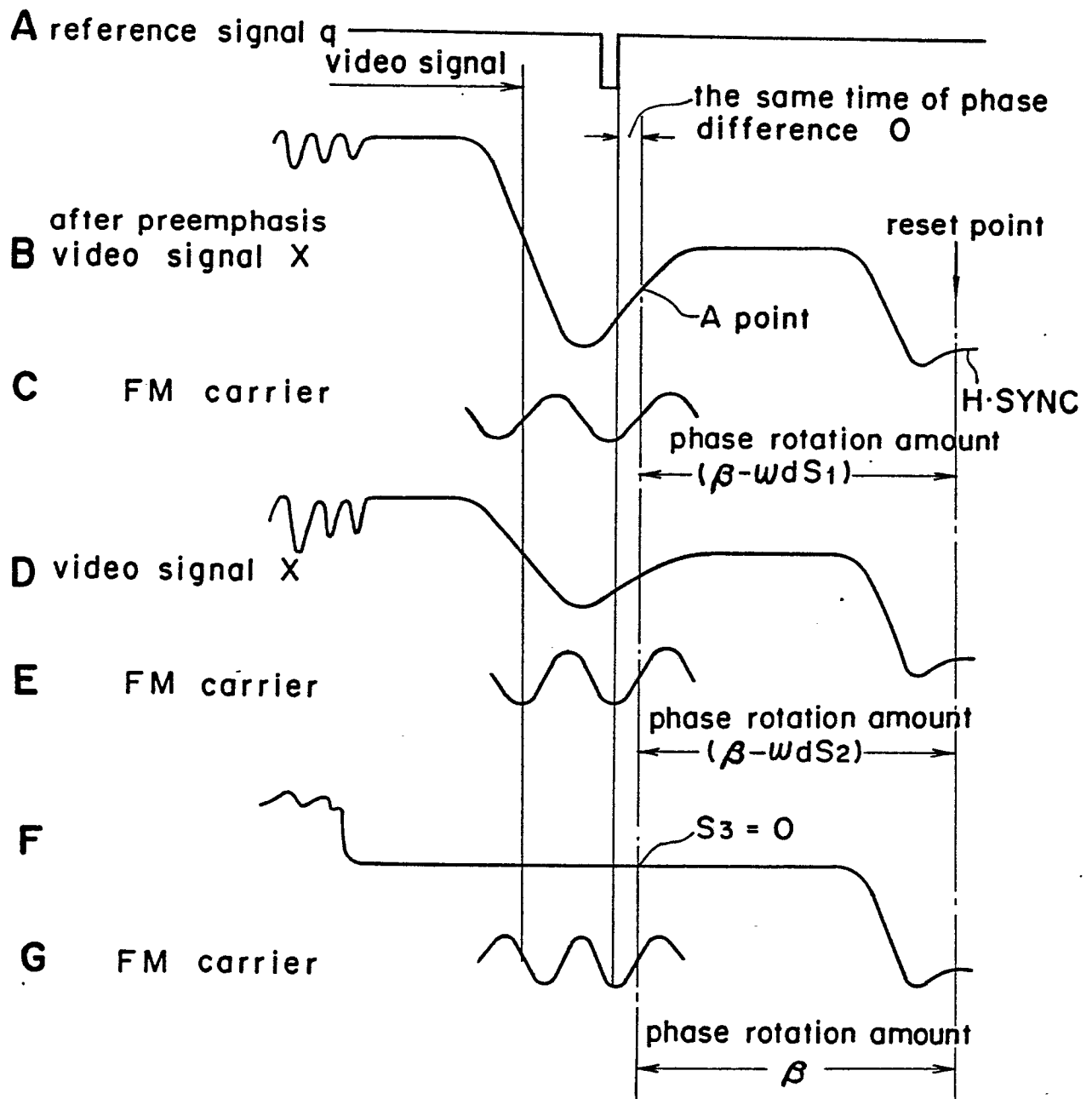
Fig. 7

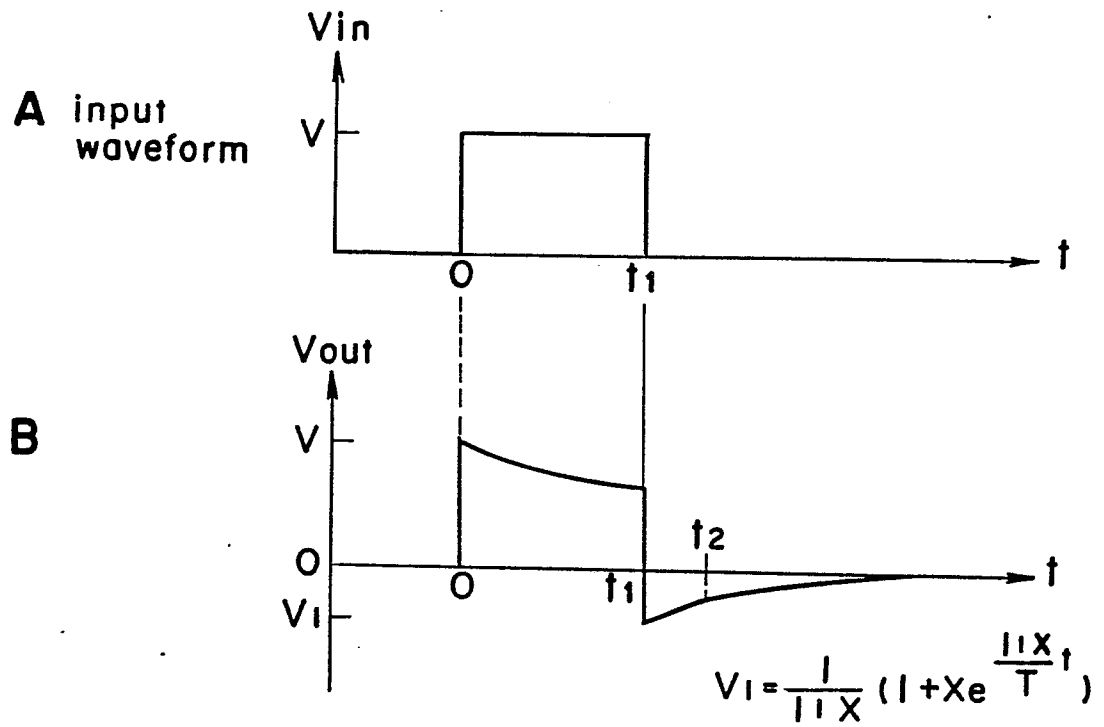
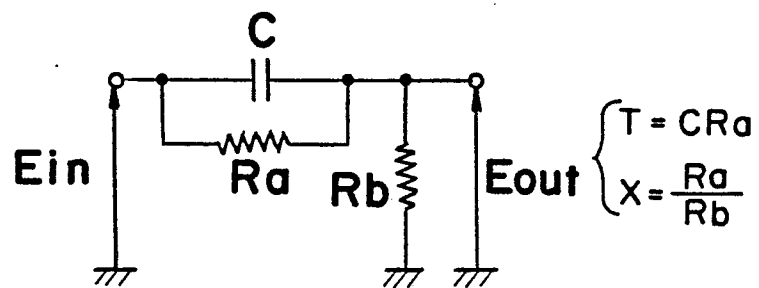
Fig. 9**Fig. 10**

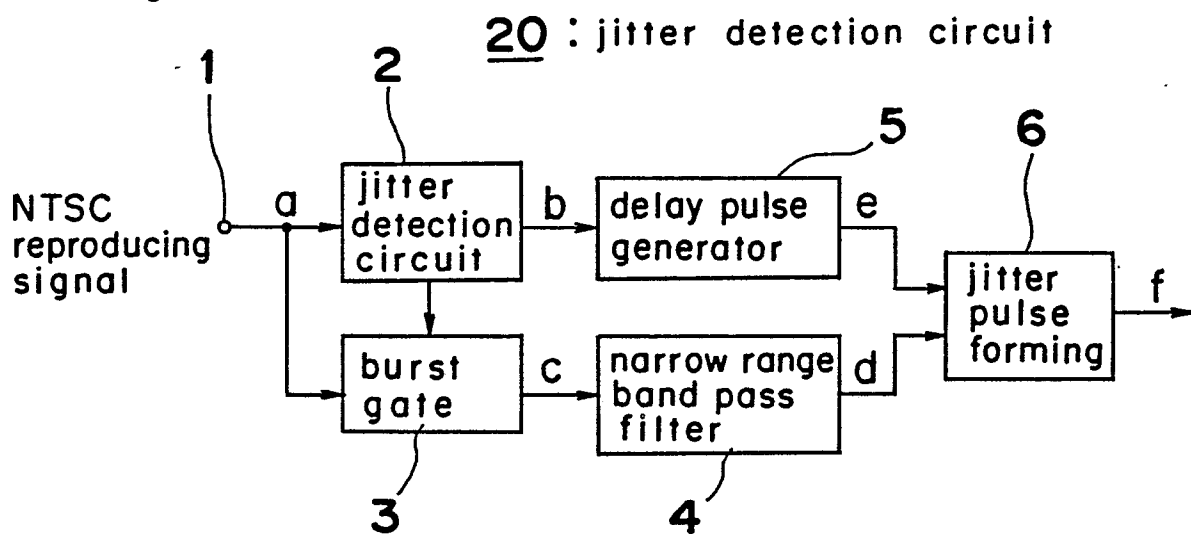
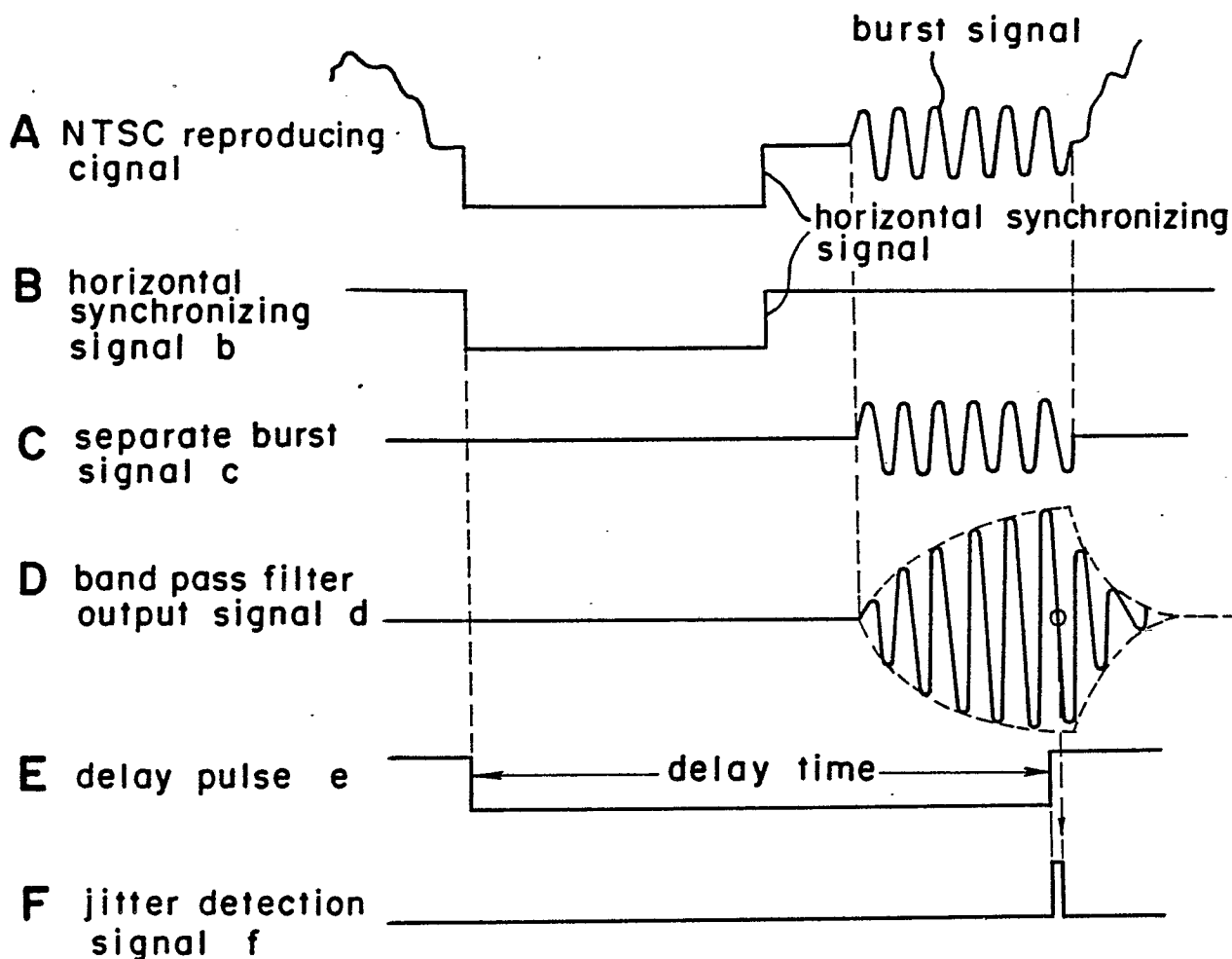
Fig. 11*Fig. 12*

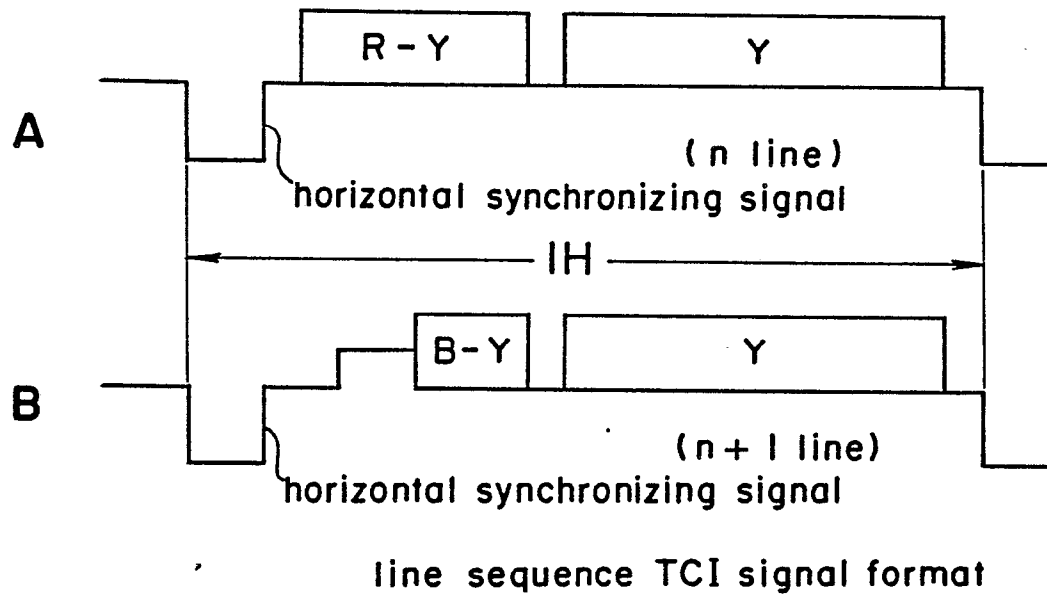
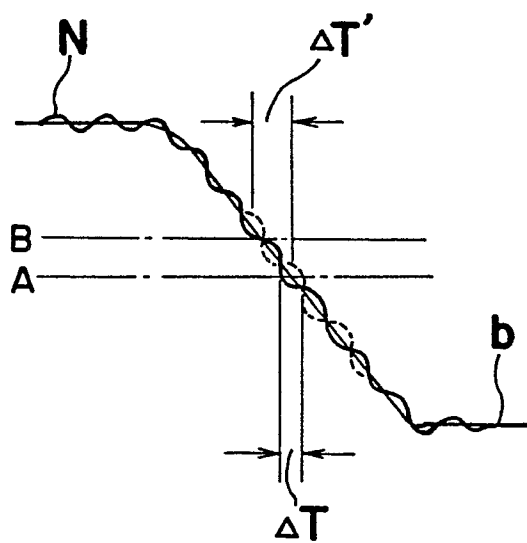
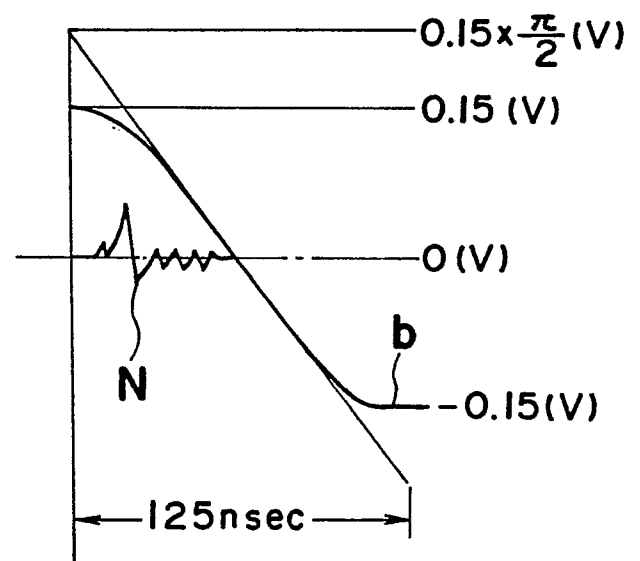
Fig. 13*Fig. 14**Fig. 15*

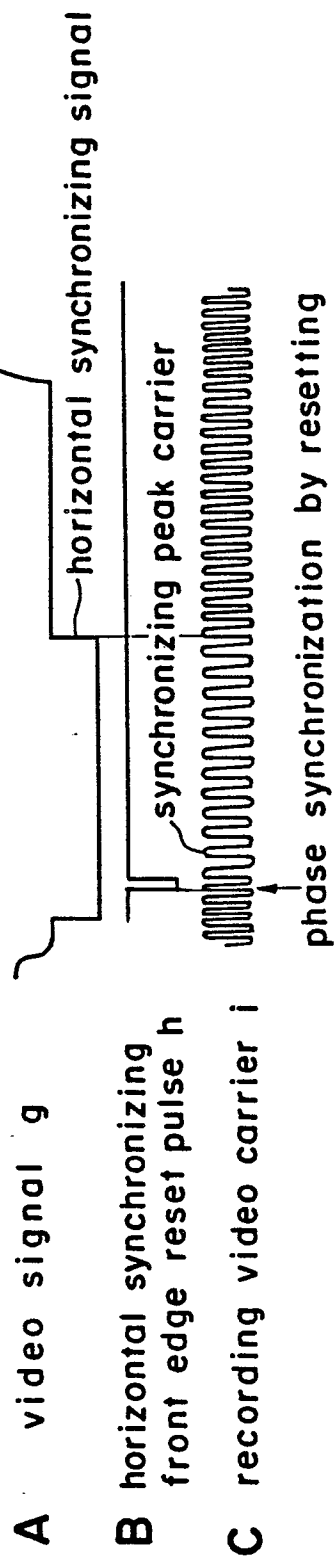
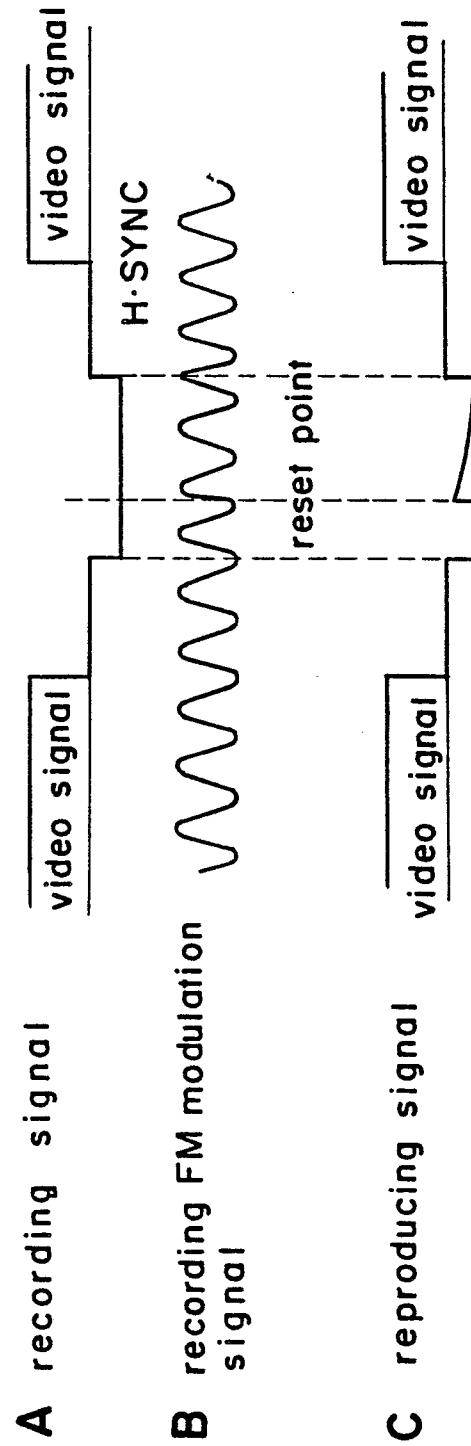
Fig. 16*Fig. 17*

Fig. 18

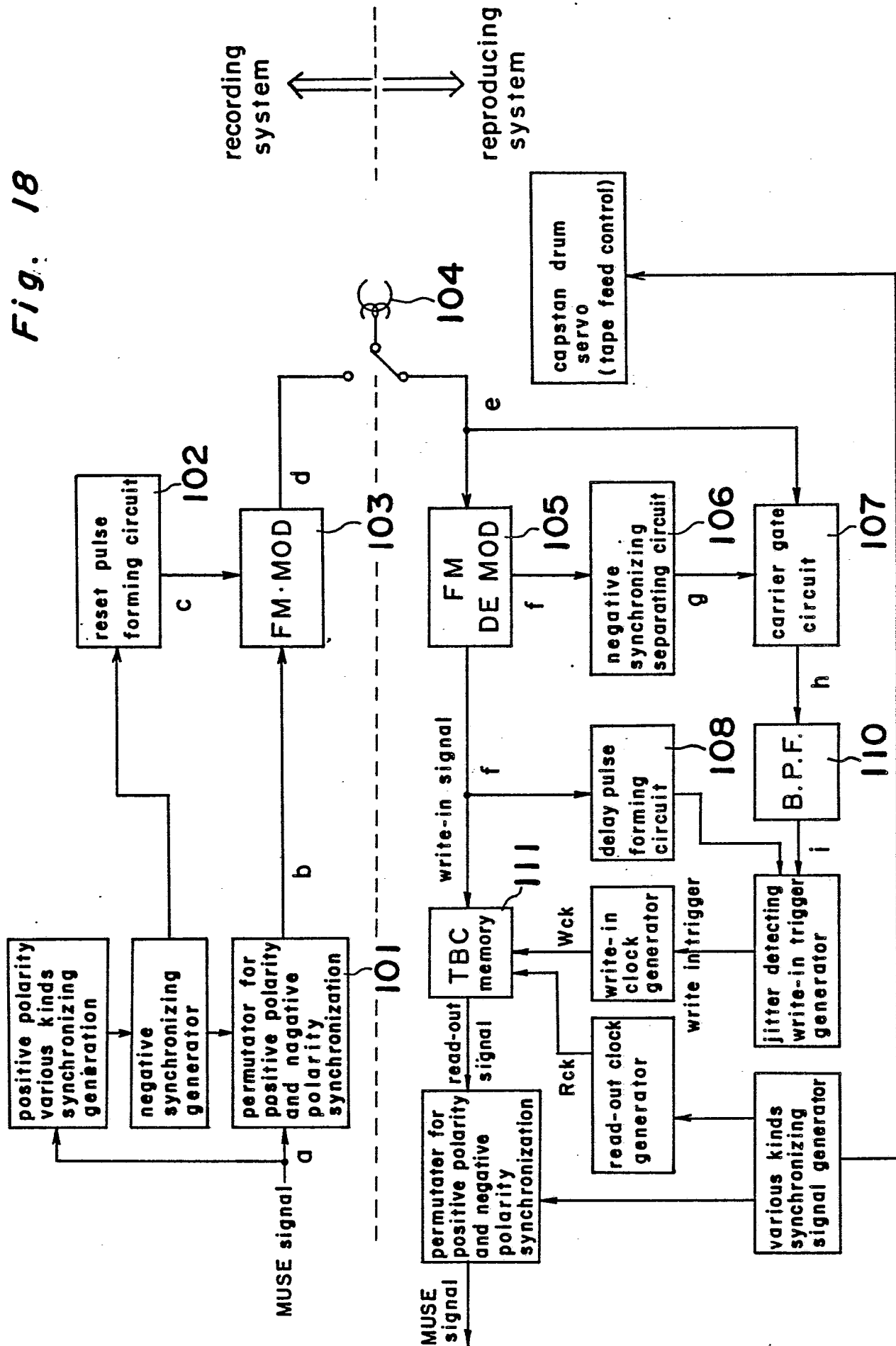


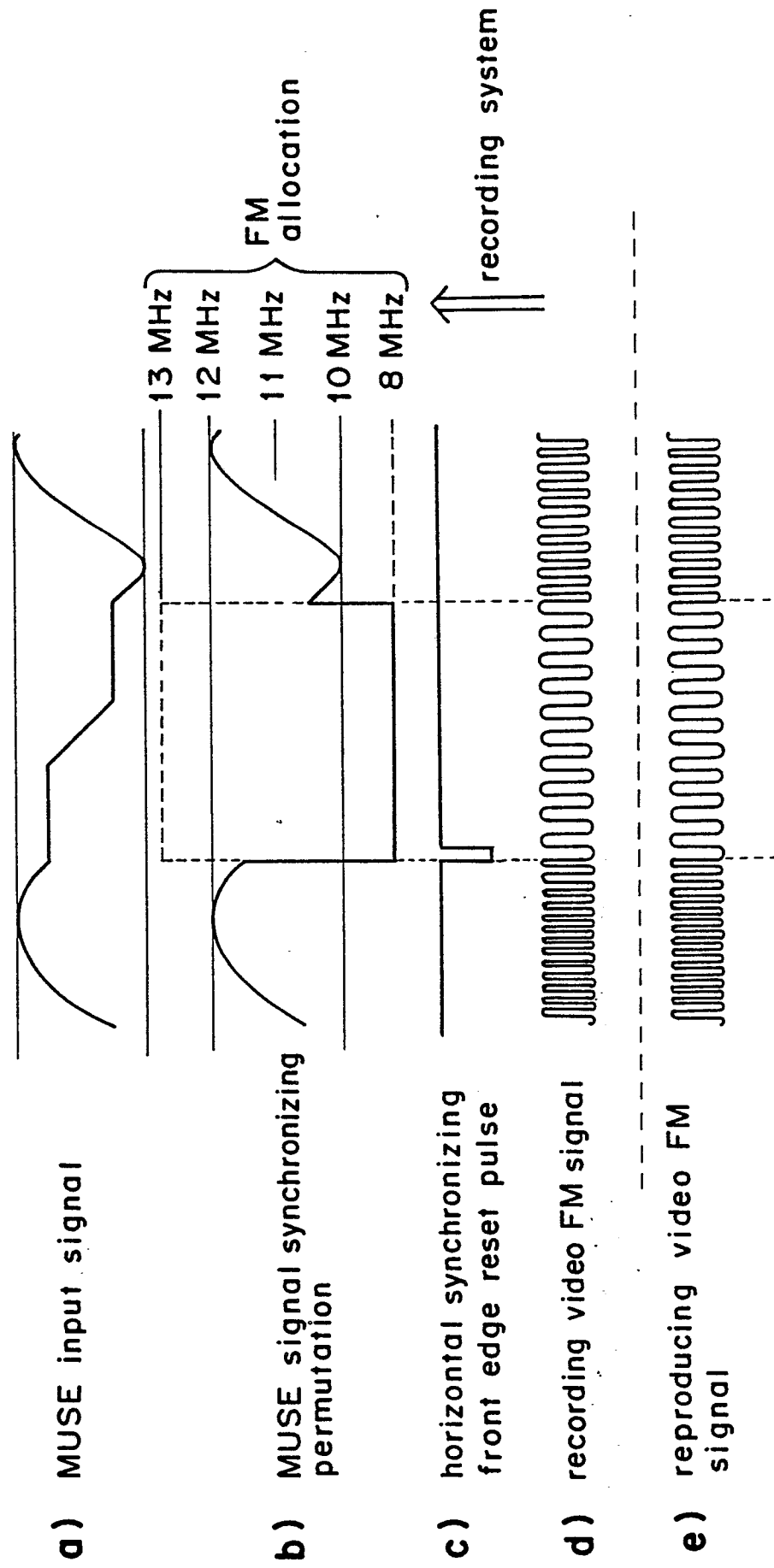
Fig. 19(a)

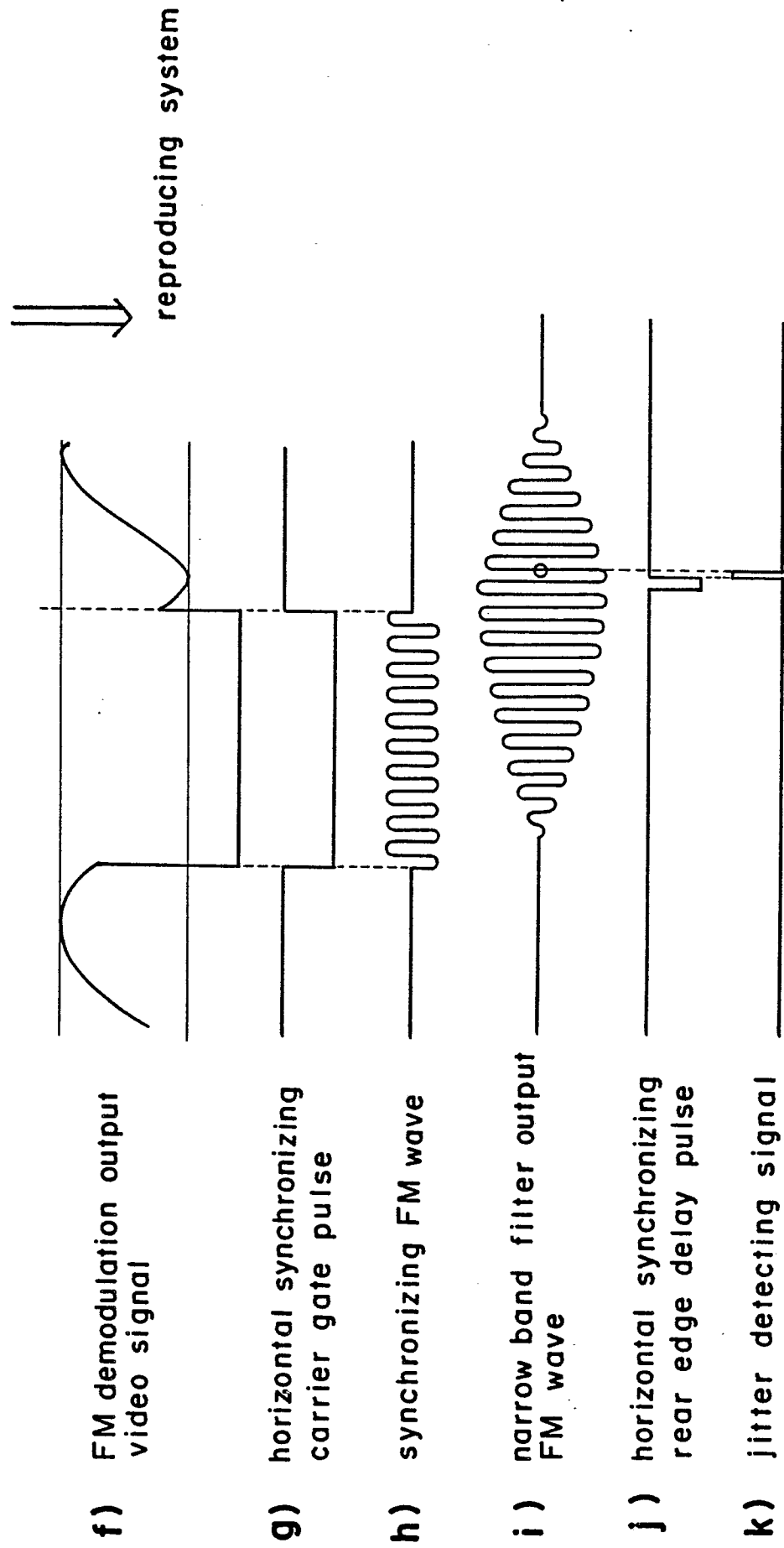
Fig. 19(b)

Fig. 20

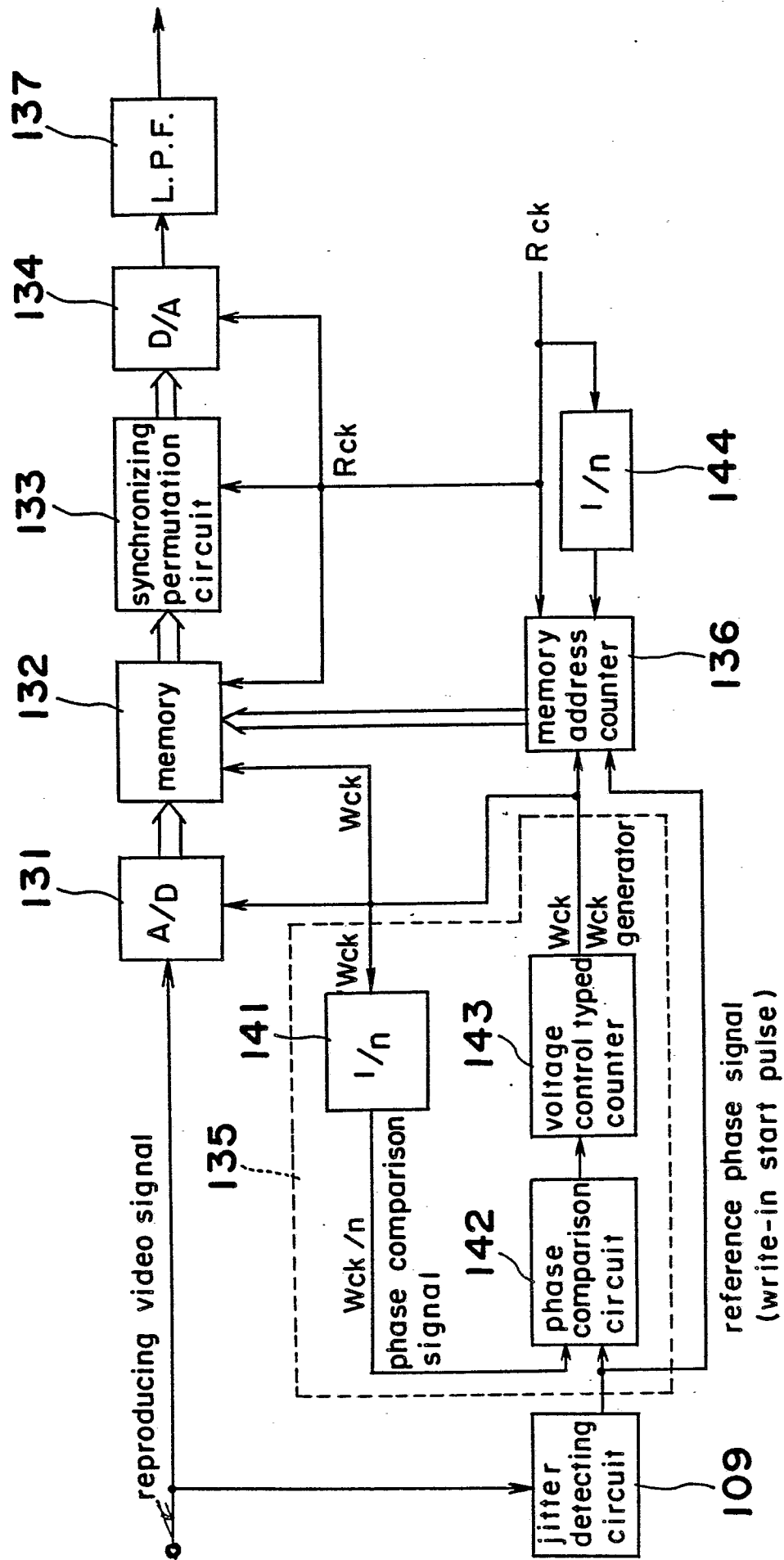
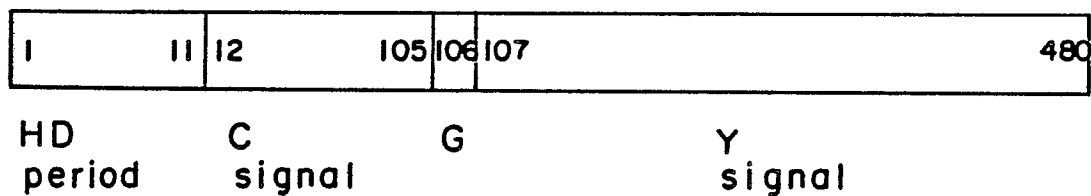
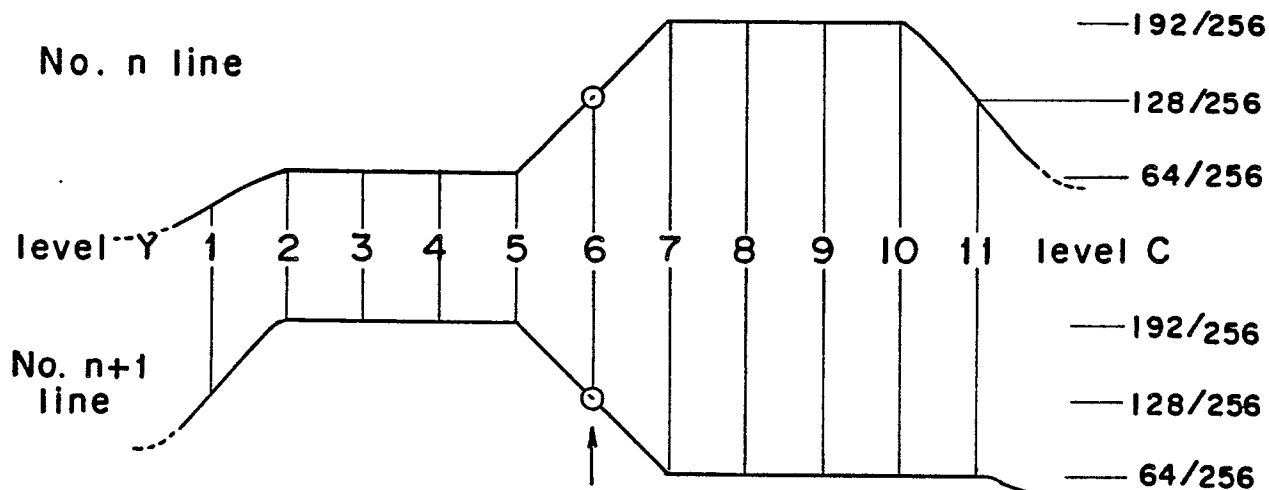


Fig. 21(a)**(a)** MUSE signal horizontal line assignment*Fig. 21(b)***(b)** horizontal synchronizing wave
(timing phase having been passed signal
middle level)