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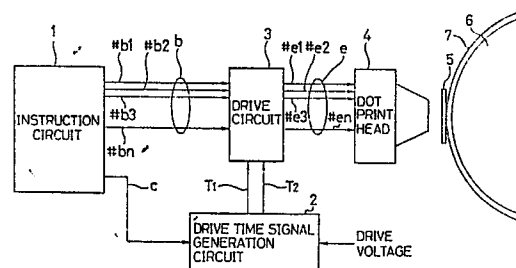
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㉙ **Dot matrix print head drive method.**

㉚ In a dot matrix print head drive method for controlling head drive signals for driving dot pins in accordance with print pattern signals, a correction factor is set specifically to each dot pin; and the length of time for which the print pattern signals are to remain in effects is varied according to the correction factor, to correct the drive time for each dot pin.

FIG.1



Description

DOT MATRIX PRINT HEAD DRIVE METHOD

BACKGROUND OF THE INVENTION

This invention concerns a method for driving dot matrix print heads in serial dot matrix printers for printing characters and graphics responsive to data transmitted from data processing equipment.

In a serial dot matrix printer, dot printing is made while the dot matrix print head is moved by a space motor, and linefeed is made by a linefeed motor. Characters and graphics are printed by repeating these operations. Of these operations, the drive of the dot print head affects the resulting print quality and print speed.

Figure 1 is a block diagram of a dot print head control circuit in which the conventional dot print head drive method is applied. Figure 2 is a timing chart illustrating the operation of the components in Figure 1. In these figures, 1 denotes an instruction circuit, 2 denotes a drive time signal generation circuit, 3 a drive circuit, and 4 a dot print head.

Instruction circuit 1 is comprised of a microcomputer. For each timing signal a, instruction circuit 1 sets print pattern signal b (#b1, #b2,..., #bn, where n is a dot pin number) to high level "1", corresponding to the dot pins in dot print head 4 to be actuated for printing, and transmits the signals to drive circuit 3; at the same time, instruction circuit 1 transmits drive signals c, which have different effective time values depending on the number of dot pins energized, to drive time signal generator circuit 2.

upon input of drive signal c from instruction circuit 1, drive time signal generator circuit 2 generates drive time signal T1 for releasing the dot pins P1 to Pn, which are pulled in when not in use for printing, and drive time signal T2 for maintaining the self-holding current and preventing the dot pins from being pulled in during printing, and sends these drive time signals T1 and T2 to drive circuit 3.

Figure 3 is a circuit diagram of drive time signal generator circuit 2. Its operation will now be described. When drive signal c is input to inverter 2a capacitor C1 which has been charged is discharged at a rising edge of the drive signal c. Then capacitor C1 is charged by current from drive voltage V_{cc} via resistor R1 at a falling edge of the drive signal c. The output d of the inverter 2a, which is called a charge/discharge signal, is input into one input terminal (+) of the comparator 2b and one input terminal (+) of another comparator 2c. The +5V voltage is divided by resistors R2 and R3, and resistors R4 and R5. The voltage across resistor R5 is input as slice level SL1 to the other input terminal (-) of comparator 2b. Likewise, the voltage across resistor R3 is input as slice level SL2 to the other input (-) of comparator 2c. Slice level SL2 is set higher than slice level SL1. Thus, as illustrated in Figure 2, as long as the level of charge/discharge signal d is less than slice level SL1, the output of comparator 2b, i.e., drive time signal T1 is kept at high level "1" and as long as the level of charge/dis-

charge signal d is less than slice level SL2, the output of comparator 2c, i.e., drive time signal T2 is kept at high level "1".

Upon receipt of the input of print pattern signal b (#b1, #b2,..., #bn), and the input of drive time signals T1 and T2 at high level "1", drive circuit 3 (Figure 1) generates head drive signal e (#e1, #e2,..., #en) corresponding to the dot pins to drive dot print head 4.

Figure 4 is a circuit diagram of drive circuit 3. As illustrated in Figure 4, inverter 3a receives drive time signal T1, which is transmitted from drive time signal generator circuit 2. The output of inverter 3a is applied to the base of transistor TRn+1. AND circuits 3b-1, 3b-2,..., 3b-n are provided or respective dot pins. Each of the AND circuits 3b-1 to 3b-n receives drive time signal T2 from drive time signal generator circuit 2. AND circuits 3b-1 to 3b-n also receive print pattern signals #b1 to #bn respectively of the print pattern signal b from instruction circuit 1. AND circuits 3b-1 to 3b-n perform logical product operation, and the outputs from these AND circuits are input, respectively, to the bases of transistors TR1 to TRn, provided for respective dot pins. The emitter of transistor TRn+1 is connected to power supply VMM, and its collector is connected to one end of each of head coils L1 to Ln. The other ends of head coils L1 to Ln are connected, respectively, to the collectors of transistors TR1 to TRn. Emitters of transistors TR1 to TRn are connected to ground G. Diode Dn+1 is connected across head coils L1 to Ln and transistors TR1 to TRn with its anode grounded. Diodes D1 to Dn are connected between respective collectors of transistors TR1 to TRn and the emitter of transistor TRn+1 with their anodes connected to the collectors of transistors TR1 to TRn.

The following explains the operation of the system as configured above, and in particular the operation of dot pin No.1 in dot print head 4.

In response to timing signal a, instruction circuit 1 raises print pattern signal #b1 to high level "1" and sends it to drive circuit 3, simultaneously sending drive signal c to drive time signal generator circuit 2 via inverter 2a. When drive signal c rises capacitor C that has been charged is discharged. The level of charge/discharge signal d gradually decreases and when it becomes equal to slice level SL2, comparator 2c sets drive time signal T2 to high level "1", and sends it to drive circuit 3; likewise, when the level of charged/discharge signal d becomes equal to slice level SL1, comparator 2b sets drive time signal T1 to high level "1", and sends it to drive circuit 3. When drive time signal T1 is high transistor TRn+1 of drive circuit 3 is turned on. Further, AND circuit 3b-1 performs logical product operation of drive time signal T2 at high level "1" and character pattern signal #b1 at high level "1". As a result, transistor TR1 is turned on. As a result, head drive signal #e1, or head drive current flows as shown by X1 in Figure 2 from power supply VMM, through transistor

TRn + 1, head coil L1, transistor TR1, and to ground G, in that order. This, in turn, generates from coil L1 a magnetic field cancelling the magnetic field, from a permanent magnet not shown, for pulling dot pins. Because of the cancellation of the magnetic field, dot pin No. 1 (P1), being biased by a leaf spring, not shown, is moved forward (toward printing paper 7 on the platen 6) to perform one dot of printing. When drive signal c sent from instruction circuit 1 falls, capacitor C1 in drive time signal generator circuit 2 is charged up. As the level of charge/discharge signal d gradually rises and when it exceeds slice level SL1, drive time signal T1 becomes low level "0". Transistor TRn + 1 in drive circuit 3 is thereby turned off. As a result, head drive signal #e1 flows through head coil L1, transistor TR1, diode Dn + 1, and head coil L1, in that order. Head drive signal #e1 therefore gradually falls, as shown by X2 in Figure 2. Further, when the level of charge/discharge signal d in drive time signal generator circuit 2 rises higher than slice level SL2, drive time signal T2 becomes low level "0". As a result, drive signal #e1 flows from ground G, through diode Dn + 1, head coil L1, diode D1, and power supply VMM, in that order. Head drive signal #e1 therefore falls quickly as shown by X3 in Figure 2.

The same operation is performed concurrently and in a similar manner on multiple dot pins that are used for printing.

According to the above scheme, however, the dot pins P1 to Pn that are driven for printing are driven for the same length of time, since print pattern signals b have the same effective period. The drive time is set to the maximum value in order to accommodate the dot pin requiring the greatest length of print time and stroke. Consequently, dot pins that print quickly or those g smaller strokes remain in operation by the drive current even after expiration of time required for printing. This results in delayed return. Also, since the drive time is set to the maximum drive time of the dot pins, the power consumption tends to be higher. If the drive period is shortened the problem of missing dots occurs or ribbon 5 can be caught by the pin return of which is delayed.

SUMMARY OF THE INVENTION

An object of this invention is to provide a drive time correction for individual dot pins.

Another object of this invention is to provide a dot print head drive method which would allow increase in speed and efficiency.

To accomplish the above object, this invention is characterized by varying the period for each print pattern signal according to a correction factor specific to each dot pin, thereby correcting drive time for each dot pin.

According to this invention, since the duration of time over which print pattern signals can be in effect is varied according to the correction factor specific to each dot pin, and since the head drive signals for driving dot pins can be controlled for individual dot pins, an optimum time can be set for each dot pin.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing the dot print head control circuit to which the conventional dot print head drive method is applied.

Figure 2 is a timing chart illustrating the operation of components in the conventional dot print head control circuit.

Figure 3 is a circuit diagram of a drive time signal generator circuit.

Figure 4 is a circuit diagram of a drive circuit.

Figure 5 is a block diagram showing the dot print head control circuit to which the dot print head drive method according to this invention is applied.

Figure 6 is a timing chart illustrating the operation of components in the dot print head control circuit according to the present invention.

Figure 7 is a circuit diagram of the delay circuit according to this invention.

Figure 8 is a flowchart illustrating the operation of a system according to the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Figure 5 is a block diagram of the dot print head control circuit to which the dot print head drive method according to this invention is applied. Figure 6 is a timing chart illustrating the operation of the components in Figure 5. The components that are identical to conventional configuration are indicated by identical reference marks. In the figures, 2 indicates the drive time signal generator circuit, 3 the drive circuit, 4 the dot print head, a the timing signal, b (#b1, #b2,..., #bn) the print pattern signals, and T1 and T2 drive time signals, and e (#e1, #e2,..., #en) the head drive signals.

10 represents the instruction circuit which, responsive to timing signal a, sets to high level "1" print pattern signals b (#b1, #b2,..., #bn), corresponding to the dot pins P1 to Pn in print head 4 to be driven for printing.

Instruction circuit 10 sends the print pattern signals b to delay circuit 11.

Further, platen correction data PL for compensating for differences in the distances between dot pins P1 to Pn and the surface of platen 6 due to the curvature of platen 6, or strokes, and print time correction data HD to compensate for the differences in print time between dots due to characteristics of individual dot pins and drive mechanisms therefor are stored in a ROM 10a.

More specifically, platen correction data PL(i) is a factor for compensating for the difference in the distance between the dot pin and the round surface of the platen 6, the distance varying from one dot pin to another due to the curvature of the platen. PL(i) can be theoretically determined when the radius of the platen roll and the distance between the center dot pin (dot pin in the center of the array of dot pin and hence situated nearest to the platen) and the platen are given.

Print time correction data HD(i) is a factor for compensating for the difference in characteristics of the dot pins and their drive mechanisms, e.g., the

strength of magnetization of the permanent magnets pulling the armatures to which the dot pins are attached to hold the dot pins at the retracted position, or the characteristics of the leaf springs for driving the dot pins upon release from the magnets. HD(i) can be determined through experiments, or measurement of the characteristics of the individual dot pins.

Moreover, drive data DR common to all dot pins are stored in a RAM 10b and can be set and varied by operation of an input section 9 such as an operational panel or dip-switch switch.

More specifically, drive data DR is a factor common to all the dot pins. It is varied to add the same amount of correction for all the dot pins. For instance it is varied to correct for deviation in characteristics of the particular print head. It can also be varied to change the density of printing. DR can be stored in a RAM 10b and can be varied or adjusted during use of the printer by manipulation of the input section 9.

When the power is turned on or when a correction data rewriting request is made and new data DR is set, the system, using this predefined information, calculates correction factor Md according to formula (1) below for each dot pin, and transmits correction factor Md, timing signal a, and load signal f (f1 to fn) to delay circuit 11.

$$Md(i) = \alpha PL(i) + \beta HD(i) + \gamma DR \quad (1)$$

(where $1 \leq i \leq n$, and α , β , and γ are parameters for determining the correction factor Md(i)).

The coefficient α , β and γ determine relative weights of the respective factors PL(i), HD(i) and DR, and can be predetermined on the basis of experiments and experiences.

Delay circuit 11 receives input of print pattern signal b transmitted from instruction circuit 10, and stores correction factor data Md sent from instruction circuit 10. It transmits to drive circuit 3 delayed print pattern signals b' (#b1', #b2', ..., #bn') for delaying the commencement of the time period when print pattern signal b is to be sent to drive circuit 3, according to correction factor Md.

Figure 7 shows the circuit configuration of delay circuit 11. In this figure, 11a denotes a correction factor register, 11b a timer counter, 11c a comparator, 11d a JK flip-flop (FF), and 11e an AND circuit.

Correction factor registers 11a (11a-1, 11a-2, ..., 11a-n) are provided for respective dot pins. Each of correction factor registers 11a stores correction factor Md(i) upon receipt of the corresponding one of the load signals f (#f1 to #fn). The correction factors Md(i) and the load signals f are sent from instruction circuit 10. The output from the register 11a is input to input terminal (+) of comparator 11c.

When the power is turned on, timer counter 11b is reset by reset signal RST. When timing signal a, sent from instruction circuit 10 and synchronized to clock signal CLK, is input, the timer counter starts counting, and inputs the current count to the other input terminal (-) of comparator 11c. When another timing signal a is input, the counter resets the count, and re-starts counting from "0".

Comparators 11c (11c-1, 11c-2, ..., 11c-n) are provided for respective dot pins. Each of the

comparators compares correction factor Md(i), from the corresponding correction factor register 11a, with the count from timer counter 11b. When the count becomes equal to the correction factor, the comparator sends high level "1" to FF 11d.

FFs 11d (11d-1, 11d-2, ..., 11d-n) are provided for respective dot pins. Timing signal a is input on one input terminal (J) of each FF 11d. On the other input terminal (K), output from comparator 11c is input. After the power is turned on, and when reset signal RST is input output Q is set to high level "1". When timing signal a, synchronized with clock signal CLK at high level "1" is input to input terminal (J), output Q falls to low level "0". When the output at high level "1" from comparator 11c is input to input terminal (K) high level "1" from output Q is sent to AND circuit 11e.

For respective dot pins, AND circuits 11e (11e-1, 11e-2, ..., 11e-n) are provided. AND circuits perform logical product operation of the output from FFs 11d (11d-1 to 11d-n) and print pattern signals b (#b1, #b2, ..., #bn) transmitted from instruction circuit 10, and transmit the results (logical products) to drive circuit 3 as delayed signal patterns b' (#b1', #b2', ..., #bn').

Drive circuit 3 has the same configuration and operates in the same way as drive circuit 3 shown in Figure 4. But delayed print pattern signals b', instead of print pattern signals b, are supplied to AND circuits 3b-1 to 3b-n. As a result, head drive signals e (#e1 to #en) begin to rise at different times after drive time signals T1 and T2 rise to high level "1". In Figure 6, print pattern signals #b1, #b3 and #bn associated with dot pins Nos. 1, 3 and n (P1, P3 and Pn) respectively are shown to be high during the first dot printing cycle, and accordingly corresponding delayed print pattern signals #b1', #b3' and #bn' are shown to be high. However, the times at which the signals #b1', #b3' and #bn' rise are different from each other, and accordingly the times at which head drive signals #e1, #e3 and #en begin to rise differ from each other.

On the other hand, all the head drive signals begin to fall gradually (at end of T1) and begin to fall rapidly (at end of T2) at simultaneously with each other.

The flowchart in Figure 8 illustrates the operation of the system as configured above. First, when the power is turned on or when there is a request for rewriting correction data (S1) and the new data for DR is set, 1 is substituted for variable i (S2). Then, correction factor Md(1) is calculated for the first dot pin according to Formula (1) above (S3); and correction factor Md(1) is stored in correction factor register 11a-1 of delay circuit 11 by means of load signal f1 (S4). Then, a comparison is made to see whether or not variable i is equal to the number of dot pins, n, (S5); if they are not equal, 1 is added to variable i (S6). By repeating steps S3-S6, the system stores correction factors Md(i) for dot pins Nos. 1 through n (P1 through Pn) in correction factor registers 11a-1 through 11a-n of delay circuit 11. This completes the storage of correction factors Md(n).

When a print instruction is received from the host computer 8 (S7), instruction circuit 10 produces

timing signal a, and sets print pattern signals b (#b1, #b2..., #bn), corresponding to the dot pins to be actuated for printing, to high level "1". The rise of print pattern signal b are synchronized with the rise of the timing signal a. Delay circuit 11 receives timing signal a at high level "1" and print pattern signals (S8). Timing signal a is also sent to drive time signal generator circuit 2 (S9). The input of timing signal a to delay circuit 11 starts the counting process, starting with "0", in timer counter 11b. When the count becomes equal to the correction factor stored in correction factor registers 11a (11a-1, 11a-2,..., 11a-n), comparators 11c (11c-1, 11c-2,..., 11c-n) output high level "1". Further, taking these outputs via FFs 11d (11d-1, 11d-2,..., 11d-n), AND circuits 11e (11e-1, 11e-2,..., 11e-n), performing logical product operation with print pattern signals b, produce the delayed print pattern signals b', which are then supplied to drive circuit 3 (S10). In drive time signal generator circuit 2, when timing signal a is input charge/discharge signal d is compared with slice levels SL1 and SL2, and drive time signals T1 and T2 are transmitted to drive circuit 3 (S11). When delayed print pattern signals b' and drive time signals T1 and T2 are input to drive circuit 3 head drive signals e (#e1, #e2,... #en) flow into respective head coils for the respective dot pins. Dot printing is thereby performed (S12).

According to this embodiment the rising edge of print pattern signal b for each dot pin is delayed by delay circuit 11, to produce delayed print pattern signal b', by means of which the length of time for which head drive signal e for each dot pin flows is controlled. This makes it possible to apply a correction to each dot pin. Therefore, the problem of deficiency in print quality due to difference in dot print head characteristics and due to the difference in stroke between the pins at the center and edges of the print head when a round platen is used can be eliminated.

Although in the above embodiment platen correction data PL, print time correction data HD, and drive information data DR were used for calculating the correction data for each dot pin, other correction data can be used in place of or in addition to the above-mentioned correction data. Also, it may be so arranged that when the power is turned on or when there is a need to revise correction data, correction data can be revised by striking each dot pin against the platen and detecting the time of printing.

As described above, this invention allows changing the effective time of print pattern signals for respective dot pins according to correction factors that are specific to individual dot pins so that the head drive signal, i.e., the drive current for driving dot pins, can be adjusted for individual dot pins. Consequently, since dot drive time can be corrected separately for individual dot pins, rather than commonly for all dot pins, even if print time is decreased a degradation in print quality due to differences in dot print head characteristics or differences in strokes due to differences in the distance between the dot pin and the platen, can be eliminated. This allows further increases in the speed of serial dot printers. Further, since the length of

time in which drive current is allowed to flow can be modified for each dot pin, the power consumption on the printer can be reduced.

Claims

1. A dot matrix print head drive method for controlling head drive signals (e) for driving dot pins (P₁, ... P_n) in accordance with print pattern signals (b), said method comprising :

setting a correction factor (M_d) specific to each dot pin ; and

varying, according to the correction factor (M_d), the length of time for which the print pattern signals (b) are to remain in effects, to correct the drive time (T₁, T₂) for each dot pin.

2. A method according to claim 1, wherein said step of varying the length of time comprises delaying the commencement of said time.

3. A method according to claim 1, wherein said correction factor (M_d) is determined on the basis of the distance from each dot pin (P₁, ... P₂) at rest and the surface of a platen (6) on which print medium is passed, said distance varying from one dot pin to another because of the curvature of the platen.

4. A method according to claim 3, wherein said correction factor (M_d) is determined also on the basis of characteristics of individual dot pins.

5. A method according to claim 4, wherein said correction factors for all the dot pins can be varied by operation through an input means.

FIG. 1

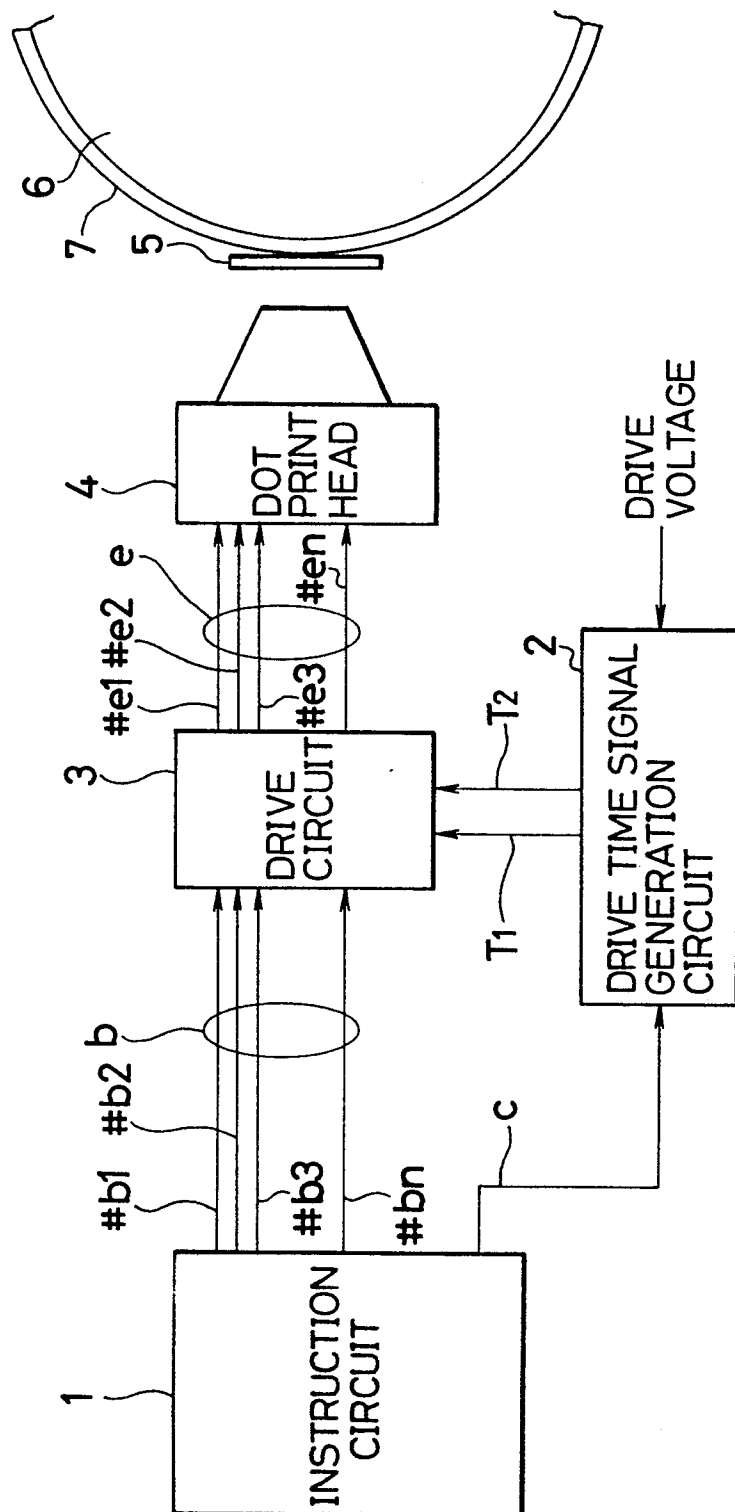


FIG. 2

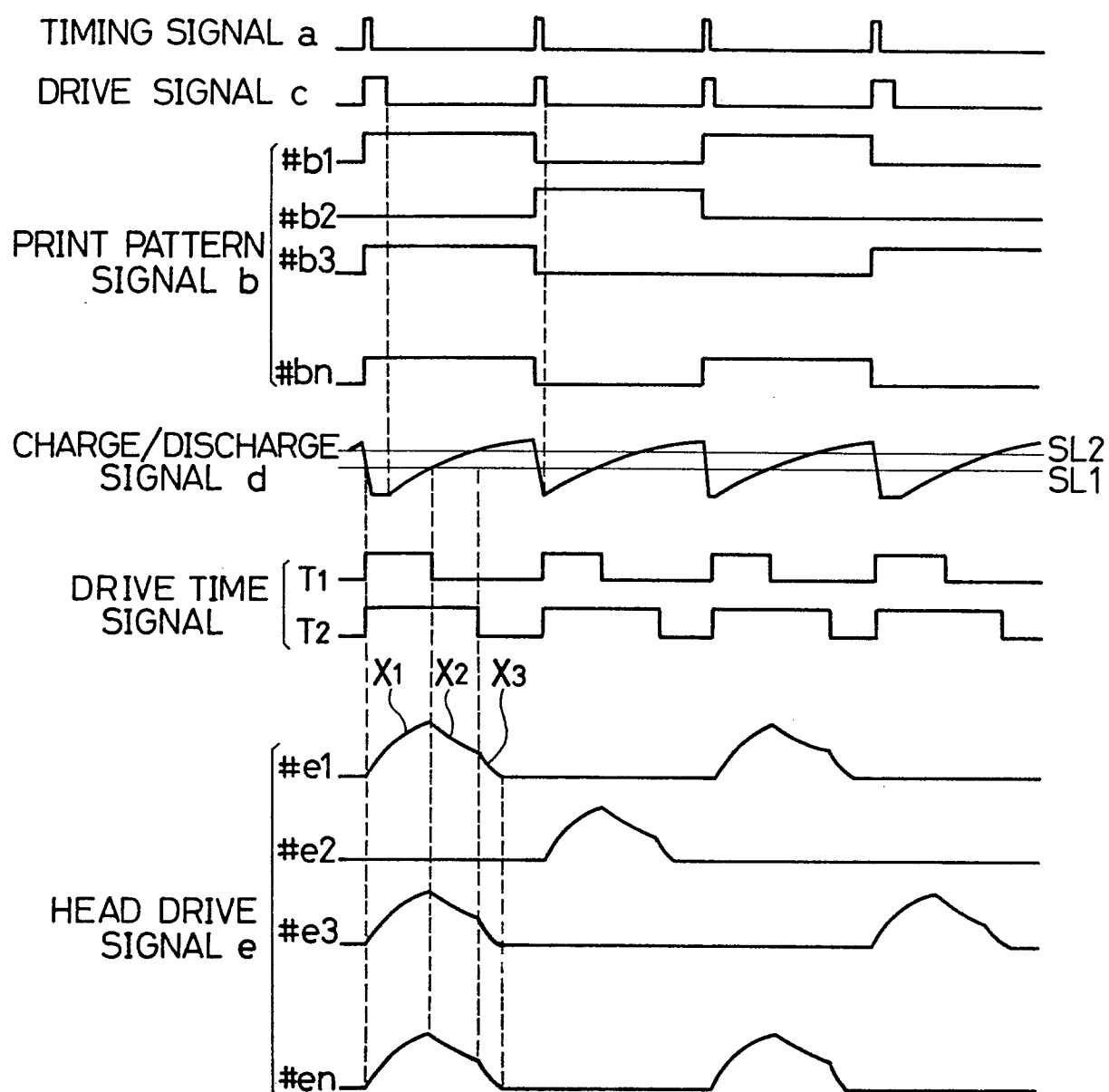


FIG. 4

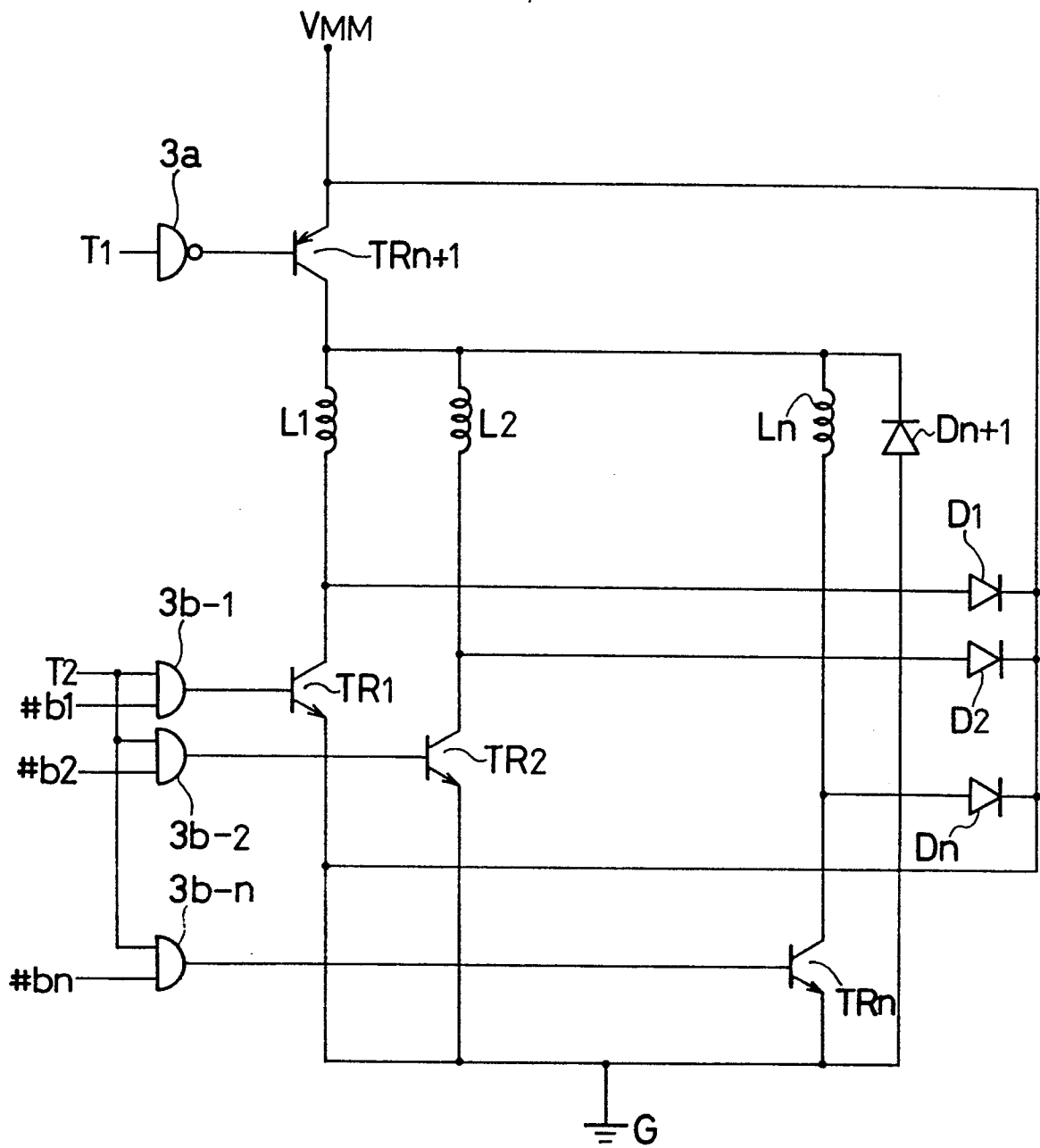


FIG. 5

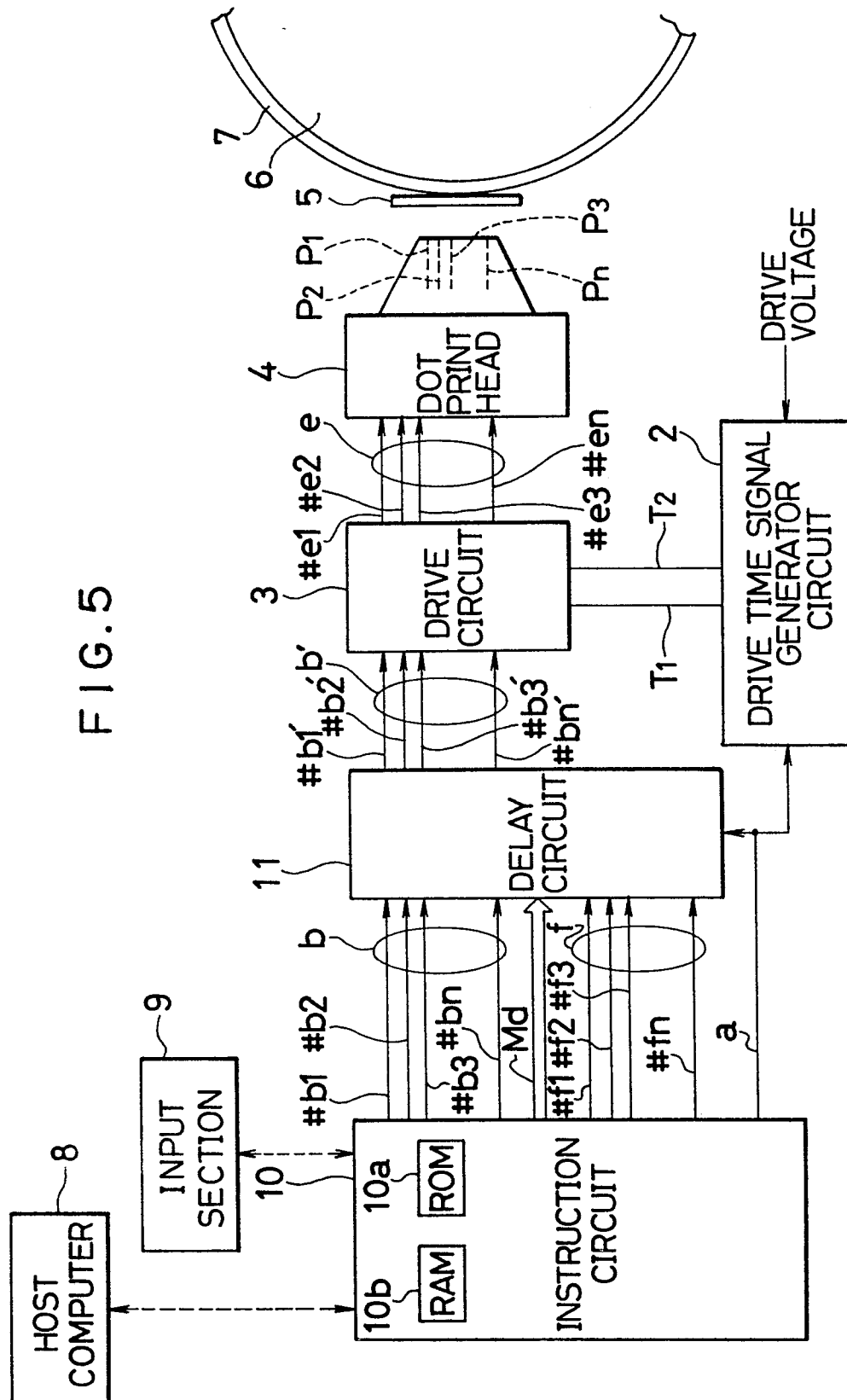


FIG. 6

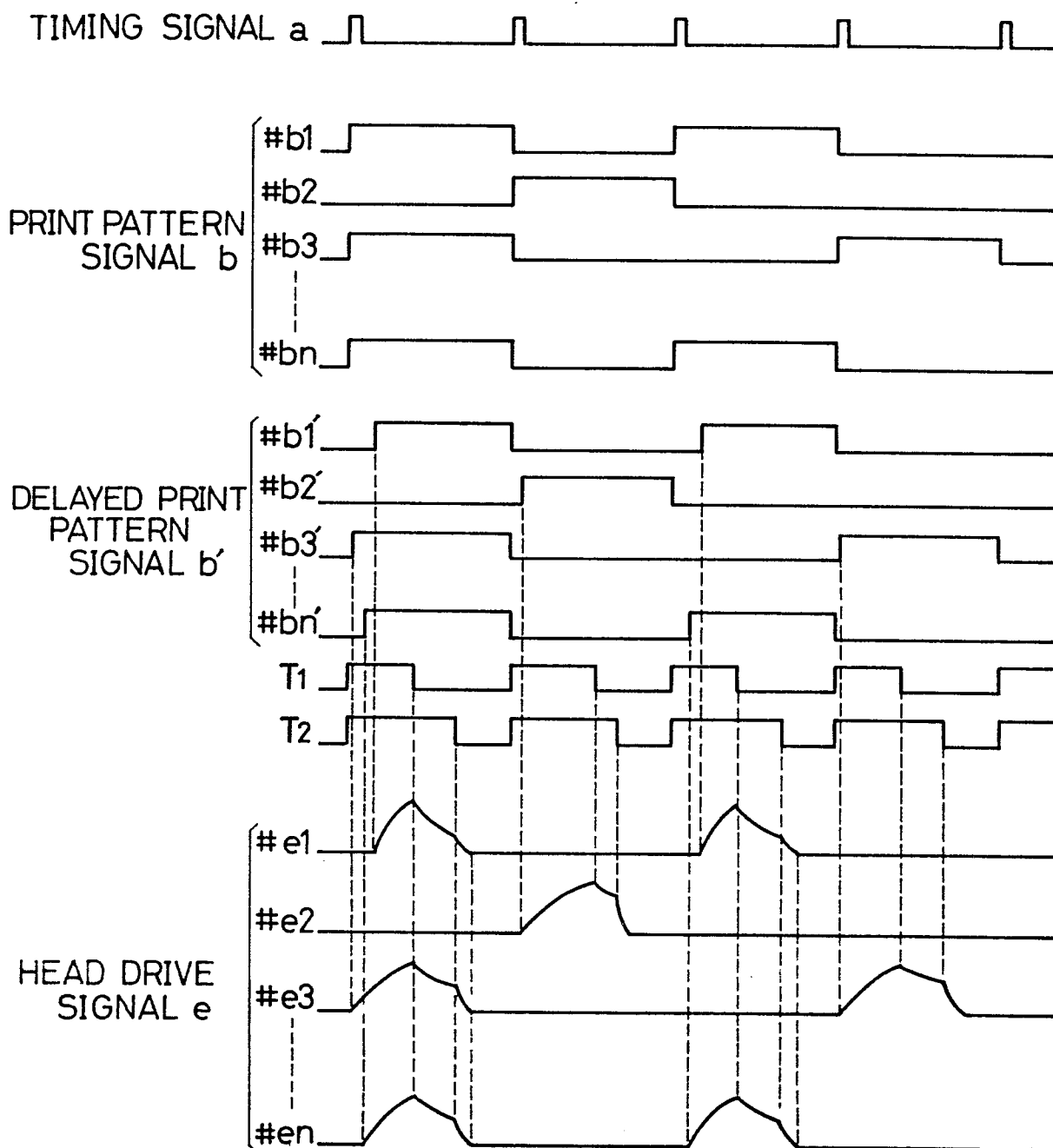


FIG. 7

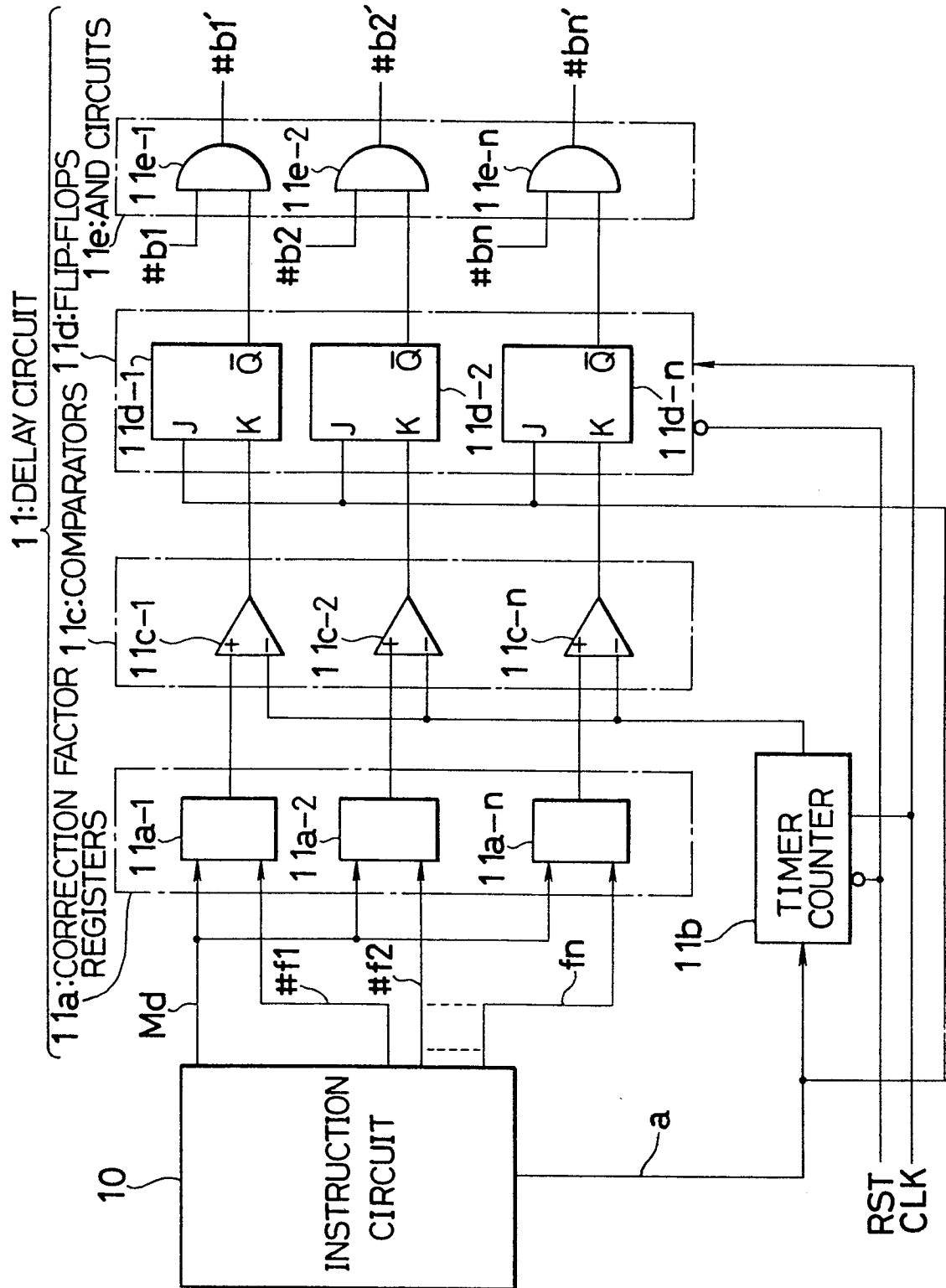


FIG. 8

