(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 301 260 A1**

# (12) EUROPEAN PATENT APPLICATION

(21) Application number: **88110412.9**

(22) Date of filing: **29.06.88**

(51) Int. Cl.[4]: **H01L 29/80 , H01L 29/205 , H01L 29/36 , H01L 29/10**

(30) Priority: **06.07.87 US 69685**

(43) Date of publication of application:
**01.02.89 Bulletin 89/05**

(84) Designated Contracting States:
**DE FR GB NL**

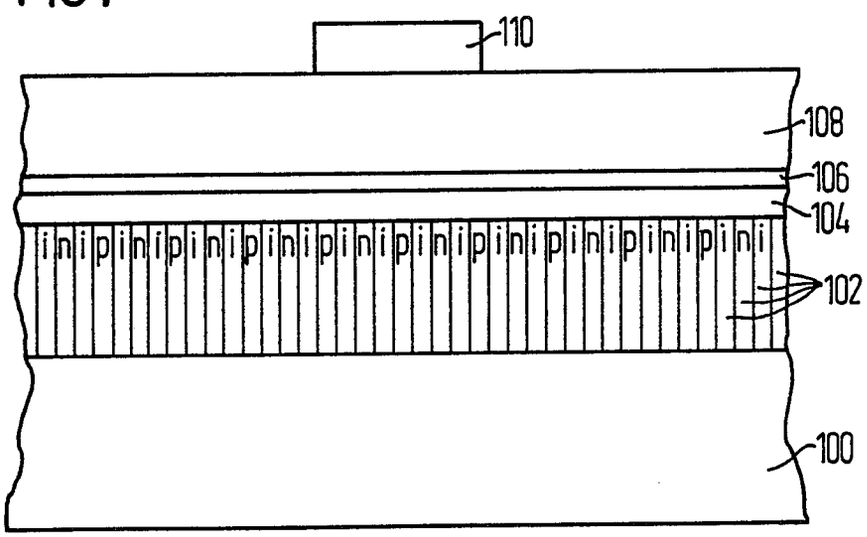
(71) Applicant: **Siemens Aktiengesellschaft Berlin und München**
**Wittelsbacherplatz 2**
**D-8000 München 2(DE)**

(72) Inventor: **Kohn, Erhard, Dr.**
**6 State Park Drive**
**Titusville NJ 08560(US)**
Inventor: **Hofmann, Karl R., Dr.**
**4 Schuh Road**
**Kingston NJ 08528(US)**

## (54) Modulation doped high electron mobility transistor with n-i-p-i structure.

(57) A modulation-doped field effect transistor includes an undoped semiconductor layer (104) and an arrangement (106, 108) for supplying charge carriers into a region of the semiconductor layer (104) adjacent one side. An arrangement (102) is provided for locally modulating the charge carrier density in another region adjacent the other side of the semiconductor layer (104) in a repeating pattern of alternations so as to inhibit current flow in the direction of the alternations.

FIG1




EP 0 301 260 A1

# MODULATION DOPED HIGH ELECTRON MOBILITY TRANSISTOR WITH n-i-p-i STRUCTURE

The present invention relates to field effect transistors and more particularly to modulation-doped high electron mobility field effect transistors.

Field effect transistors (FET'S) using gallium arsenide (GaAS) are known to be capable of high speed operation. Devices using gallium arsenide/aluminum gallium arsenide (GaAs/AlGaAs) heterostructures form a two-dimensional electron gas (2DEG). In such devices the donor impurities are confined away from the active channel in which electrons may flow. This separation of donor impurities from the electron layers causes the device to exhibit extremely high electron mobilities and thereby to be capable of extremely fast operation, for example, in high speed switching.

Nevertheless, since the electrons in the device must still transit the channel length, an ultimate switching speed depending on the channel length will exist, so long as the conductivity modulation of the device is achieved by varying the carrier density in the channel.

In accordance with a first aspect of the invention, a modulation-doped field effect transistor comprises a first semiconductor layer being substantially undoped, an arrangement on one side of the first semiconductor layer for supplying charge carriers into a first region of the first semiconductor layer adjacent the one side of the semiconductor layer, and an arrangement for locally modulating hole and electron density in a second region of the first semiconductor layer adjacent another side thereof in a repeating pattern of alternations so as to substantially inhibit conduction therethrough in the direction of the alternations.

In accordance with a second aspect of the invention, the modulation doped field effect transistor includes a gate arrangement for shifting the charge carriers between the first and second regions.

In accordance with a third aspect of the invention, the arrangement for locally modulating doping comprises alternating p and n doped semiconductor regions adjacent the second region.

In accordance with a fourth aspect of the invention, the arrangement for supplying charge carriers comprises a second semiconductor layer adjacent the first region.

In accordance with a fifth aspect of the invention, the first semiconductor layer is gallium arsenide and the second semiconductor layer is aluminum gallium arsenide.

In accordance with a sixth aspect of the invention, the first and second semiconductor layers are separated by a third semiconductor layer of aluminum gallium arsenide, the third semiconductor layer being thin compared with the first and second semiconductor layers.

In accordance with a seventh aspect of the invention, the alternating p and n doped semiconductor regions are formed in respective layers of aluminum gallium arsenide.

In accordance with an eighth aspect of the invention, a modulation-doped field effect transistor includes a first semiconductor layer being substantially undoped, a second semiconductor layer of a first conducting type, formed over the first semiconductor layer, and a gate electrode arrangement formed over the second semiconductor layer for controlling conduction through a conduction channel formed in the first semiconductor layer. The transistor includes a third semiconductor layer of the first conductivity type and a fourth semiconductor layer of a second conductivity type formed next the third semiconductor layer, the third and fourth semiconductor layers having respective ends on one side thereof abutting the first semiconductor layer.

In accordance with an ninth aspect of the invention, the third and fourth semiconductor layers form part of a plurality of semiconductor layers of Al Ga As in a sandwich structure of alternating p and n conductivity type semiconductor layers, the plurality of layers having respective ends on the one side abutting the first semiconductor layer and having respective ends on the other side abutting the fifth semiconductor layer.

In accordance with a tenth aspect of the invention, a sixth semiconductor layer of substantially undoped AlGaAs is interposed between the first and second semiconductor layers, the sixth semiconductor layer being relatively thin compared with the first and second semiconductor layers.

In accordance with an eleventh aspect of the invention, a semiconductor layer of AlGaAs of substantially intrinsic conductivity is interposed between each one of the plurality of semiconductor layers and the next, such that a repeating pattern of conductivities is formed in the sandwich structure of n-conductivity, intrinsic-conductivity, p-conductivity, and intrinsic-conductivity semiconductor layers.

In accordance with a further aspect of the invention, a modulation-doped field effect transistor comprises a first-semiconductor layer being substantially undoped, and a second semiconductor layer of a first conductivity type, formed over the first layer. The transistor further includes a gate electrode formed over the second semiconductor layer for controlling conduction through a conduction channel formed in the first semiconductor lay-

er, the conduction channel forming a main controllable-conduction path of the transistor, and a plurality of semiconductor layers of the first conductivity type and a second conductivity type, in a layered structure with the first and second conductivity types alternating. The plurality of semiconductor layers has respective ends on one side thereof abutting the first semiconductor layer such that the plurality of semiconductor layers on the one hand and the first and second layers on the other hand are in substantially mutually perpendicular planes with the first and second conductivity types in the plurality of semiconductor layers alternating progressively along a length direction of the conduction channel, the layers in the plurality being of sufficient thickness to prevent substantially conduction through the plurality of semiconductor layers in a direction perpendicular to the planes of the plurality of semiconductor layers.

The invention will next be described in greater detail, with reference to the drawing, in which:

FIG. 1 shows a cross-sectional view, not to scale, of a four-terminal modulation doped field effect transistor structure in accordance with the invention; and

FIG. 2 shows a cross-sectional view, not to scale, of a vertical field effect transistor structure in accordance with the invention. Features in FIG. 2 corresponding to features in FIG. 1 are designated by the same reference numeral augumented by 100.

In the transistor structure of FIG. 1, 100 is a substrate layer of gallium arsenide (GaAs). Adjoining substrate layer 100 is a region generally designated in Fig. 1 as 102, comprising a composite of aluminum gallium arsenide (AlGaAs) layers lying in planes substantially perpendicular to the plane of substrate 100. The layers are arranged in a sequence of n-doped, intrinsic (i), p-doped (p), intrinsic (i), n-doped, intrinsic materials, and so on, in the same repeating group sequence of n-i-p-i. While more than one such n-i-p-i group is utilized in the exemplary embodiment, the total number of such groups is not, in itself, a primary consideration. The lateral thickness of the n-i-p-i layers is made sufficiently large to substantially prevent superlattice behavior.

Adjoining n-i-p-i region 102 in a plane generally parallel to the plane of substrate 100 is a layer 104 of substantially undoped GaAs. Accordingly, layer 100 and layer 104 include n-i-p-i region 102 therebetween, the planes of the n-i-p-i region being substantially perpendicular to the planes of layer 100 and layer 104. Adjoining layer 104 is a layer 106 of substantially undoped AlGaAs, referred to herein as spacer 106. Spacer 106 is a relatively thin layer. Adjoining spacer 106 is a layer 108 of n-doped AlGaAs which forms a gate dielectric for a gate 110 which is of a conductive material and is adjacent layer 108.

To summarize, the layer arrangement comprises semi-insulating substrate 100, n-i-p-i region 102, undoped GaAs layer 104, undoped AlGaAs spacer 106, n-doped AlGaAs layer 108, and conductive gate 110.

In operation, layer 108 performs the function of an electron donor, contributing electrons which, having passed through spacer 106, form a two dimensional electron gas, commonly referred to in the literature as 2DEG, in at least that portion of undoped GaAs layer 104 which adjoins spacer 106 and which can be thought of as the active channel.

The thickness of spacer 106 provides a compromise since increasing the thickness leads to higher electron mobility but will also cause lower electron densities in the active channel. Spacer 106 may also be dispensed with altogether, as will be described later.

To the extent of separating mobile carriers from the supplying dopant atoms, the present arrangement resembles known selectively doped hetero-junction transistors (SDHT), also referred to as high electron mobility transistors (HEMT) in which such separation is achieved by using the band-gap discontinuity in the conduction band of two epitaxially grown layers of different composition and doping (e.g. AlGaAs and GaAs).

With no bias applied between layer 104 and n-i-p-i region 102, the density of holes and electrons in layer 104 will be formed or modulation doped in a pattern corresponding to the n-i-p-i layers. Accordingly, current cannot flow in a horizontal direction at this interface, i.e. parallel to the interface. Thus, if n-i-p-i region 102 is allowed to float electrically, and a potential difference is applied in a horizontal direction, that is, in a direction along the plane of layer 104 substantially no current will flow in response to such an electric field applied between the ends of layer 104, for example by way of source and drain electrodes, not shown in FIG. 1.

On the other hand, when a positive bias voltage is applied to gate electrode 110, electron current responsive to a horizontally applied potential difference can flow horizontally in the upper portion of layer 104, that is, the portion distal from n-i-p-i region 102. The transition from non-conduction to conduction in layer 104 and vice versa occurs as a result of the 2DEG in layer 104 being switched from near the bottom interface to the top interface and vice versa. Since the thickness dimension of layer 104 is extremely small in comparison with the lateral dimensions, such switching is very fast in comparison with the classical FET action and does not suffer from the effects of transit time delay. No gate current or substrate current will flow, other than capacitive displacement current. The device

described therefore functions as a very fast switch, a small vertical shift of the electron current between the upper and lower interfaces being sufficient to effect switching.

Thus, so long as the electrons are confined to the vicinity of the top horizontal interface between layer 104 and spacer 106, the device in accordance with the present invention functions similarly to a conventional HEMT. On the other hand, when the electron wave is towards the lower interface, the heterojunction between layer 104 and n-i-p-i region 102, then the channel current depends on the condition at this lower interface where horizontal mobility is constrained, as has been described. Moreover, transfer of the electron wave from the top interface to the lower interface, achieved by a relatively high negative bias on gate 110 can also occur as a result of a relatively high positive bias on susbtrate 100, used thus as a back gate, in contrast to top gate 110. Also, such a transfer will result from a high positive potential being applied to one end of layer 104, corresponding to a high positive applied drain voltage. Thus, as the applied drain voltage is first increased from a low value, the horizontal or drain current through layer 104 will at first increase in the aforementioned normal FET manner. Thereafter, as the electron wave is shifted toward the lower interface responsive to a higher drain voltage, the drain current will decrease, corresponding to a negative incremental or differential resistance. Such a characteristic is useful in high frequency oscillators and in logic switching. In the device in accordance with the present invention, the negative resistance is moreover controllable by changing the gate potential.

The transistor structure of FIG. 2 has a vertical configuration and represents a convenient configuration for fabrication. Adjacent a semi-insulating substrate 200 is an n-doped GaAs substrate 201 which is provided with drain contacts 212, 212′ and adjoins n-i-p-i region 202. Undoped GaAs layers 204, 204′ adjoin n-i-p-i region 202 on respective sides thereof to provide active channel areas. N-doped layers 208, 208′ adjoin layers 204, 204′, respectively and support respective gate electrodes 210, 210′. A source region 214 surmounts n-i-p-i region 202 in a plane parallel to the plane of the n-i-p-i layers and has an electrode 216 coupled thereto.

The transistor in accordance with the present invention has at least two principal fields of application. One field is as a high speed logic switch element, e.g. as an inverter. Another application is as a microwave oscillator, using differential negative resistance controllable by gate bias.

While the invention has been described in terms of preferred embodiments, various changes which do not depart from the scope of the claims following will suggest themselves to one skilled in the art. For example, the intrinsic layers in n-i-p-i region 102 or 202 are not essential, since appropriate modulation doping can also be produced by an n-p-n-p-n-etc. sequence.

## Claims

1. A modulation-doped field effect transistor including a first semiconductor layer being substantially undoped, a second semiconductor layer of a first conducting type, formed over said first semiconductor layer, and gate electrode means formed over said second semiconductor layer for controlling conduction through a conduction channel formed in said first semiconductor layer, comprising:

a third semiconductor layer of said first conductivity type; and

a fourth semiconductor layer of a second conductivity type formed next said third semiconductor layer, said third and fourth semiconductor layers having respective ends on one side thereof abutting said first semiconductor layer.

2. A modulation-doped field effect transistor according to Claim 1 wherein said first semiconductor layer is gallium arsenide (GaAs), and said second, third, and fourth layers are aluminum gallium arsenide (AlGaAs).

3. A modulation-doped field effect transistor according to Claim 2 wherein said first conductivity type is n and said second conductivity type is p.

4. A modulation-doped field effect transistor according to Claim 3 including a fifth layer of a semi-insulating semiconductor, said third and fourth semiconductor layers having respective ends on the other side thereof abutting said fifth semiconductor layer.

5. A modulation-doped field effect transistor according to Claim 4 wherein said third and fourth semiconductor layers form part of a plurality of semiconductor layers of AlGaAs in a sandwich structure of alternating p and n conductivity type semiconductor layers, said plurality of layers having respective ends on said one side abutting said first semiconductor layer and having respective ends on said other side abutting said fifth semiconductor layer.

6. A modulation-doped field effect transistor according to Claim 5 wherein a sixth semiconductor layer of substantially undoped AlGaAs is interposed between said first and second semiconductor layers, said sixth semiconductor layer being relatively thin compared with said first and second semiconductor layers.

7. A modulation-doped field effect transistor according to Claim 5, wherein a semiconductor layer of AlGaAs of substantially intrinsic conductivity is interposed between each one of said plurality of semiconductor layers and the next, such that a repeating pattern of conductivities is formed in said sandwich structure of n-conductivity, intrinisc-conductivity, p-conductivity, and intrinsic-conductivity semiconductor layers.

8. A modulation-doped field effect transistor according to Claim 6 wherein a semiconductor layer of AlGaAs of substantially intrinsic conductivity is interposed between each one of said plurality of semiconductor layers and the next, such that a repeating pattern of conductivities is formed in said sandwich structure of n-conductivity, intrinisc-conductivity, p-conductivity, and intrinsic-conductivity semiconductor layers.

9. A modulation-doped field effect transistor comprising:

a first-semiconductor layer being substantially undoped;

a second semiconductor layer of a first conductivity type, formed over said first layer;

gate electrode means formed over said second semiconductor layer for controlling conduction through a conduction channel formed in said first semiconductor layer, said conduction channel forming a main controllable conduction path of said transistor; and

a plurality of semiconductor layers of said first conductivity type and a second conductivity type, in a layered structure with said first and second conductivity types alternating, said plurality of semiconductor layers having respective ends on one side thereof abutting said first semiconductor layer such that said plurality of semiconductor layers on the one hand and said first and second layers on the other hand are in substantially mutually perpendicular planes with said first and second conductivity types in said plurality of semiconductor layers alternating progressively along a length direction of said conduction channel, said layers in said plurality being of sufficient thickness to prevent substantially conduction through said plurality of semiconductor layers in a direction perpendicular to the planes of said plurality of semiconductor layers.

10. A modulation-doped field effect transistor according to Claim 9 including a third semiconductor layer, being substantially undoped and being interposed between said first and second layers.

11. A modulation-doped field effect transistor according to Claim 10 including a fourth semiconductor layer of semi-insulating conductivity, said plurality of semiconductor layers having respective ends thereof, on a side thereof opposite said one side thereof, abutting said fourth semiconductor layer.

12. A modulation-doped field effect transistor according to Claim 10 wherein said first semiconductor layer is gallium arsenide, said second, third, and fourth semiconductor layers are aluminum gallium arsenide.

13. A modulation-doped field effect transistor according to Claim 10 wherein said third semiconductor layer is thin compared with said first and second semiconductor layers.

14. A modulation-doped field effect transistor comprising:

a first semiconductor layer being substantially undoped;

means on one side of said first semiconductor layer for supplying charge carriers into a first region of said first semiconductor layer adjacent said one side of said semiconductor layer; and

means for locally modulating doping of holes and electrons in a second region of said first semiconductor layer adjacent another side thereof in a repeating pattern of alternations so as to substantially inhibit conduction therethrough in the direction of said alternations.

15. A modulation-doped field effect transistor according to Claim 14 including gate means for shifting said charge carriers between said first and second regions.

16. A modulation-doped field effect transistor according to Claim 15 wherein said means for locally modulating doping comprises alternating p and n doped semiconductor regions adjacent said second region.

17. A modulation-doped field effect transistor according to Claim 15 wherein said means for supplying charge carriers comprises a second semiconductor layer adjacent said first region.

18. A modulation-doped field effect transistor according to Claim 15 wherein said first semiconductor layer is gallium arsenide and said second semiconductor layer is aluminum gallium arsenide.

19. A modulation-doped field effect transistor according to Claim 18 wherein said first and second semiconductor layers are separated by a third semiconductor layer of aluminum gallium arsenide, said third semiconductor layer being thin compared with said first and second semiconductor layers.

20. A modulation-doped field effect transistor according to Claim 16 wherein said alternating p and n doped semiconductor regions are formed in respective layers of aluminum gallium arsenide.

FIG1

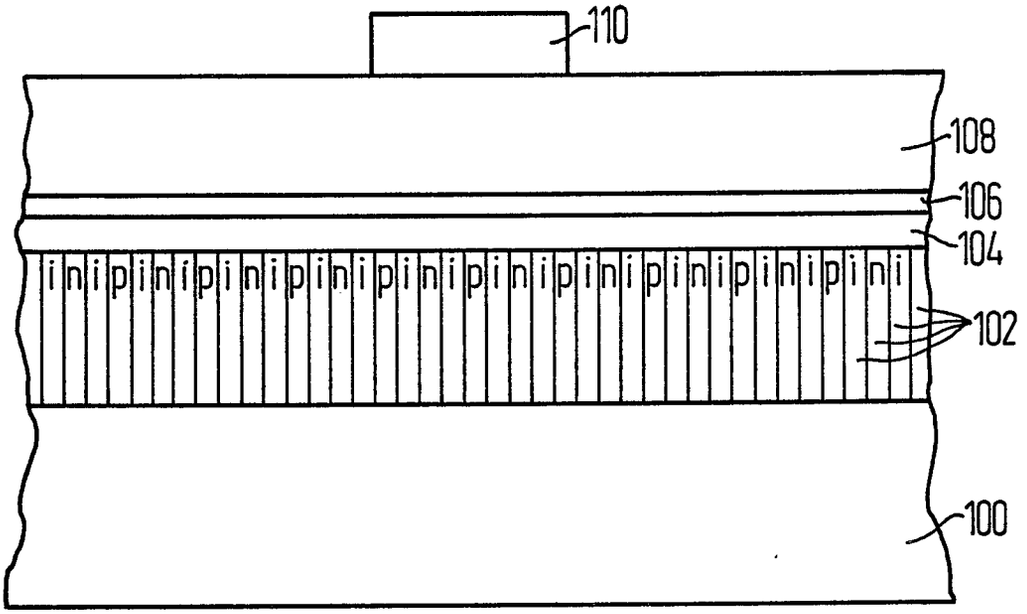
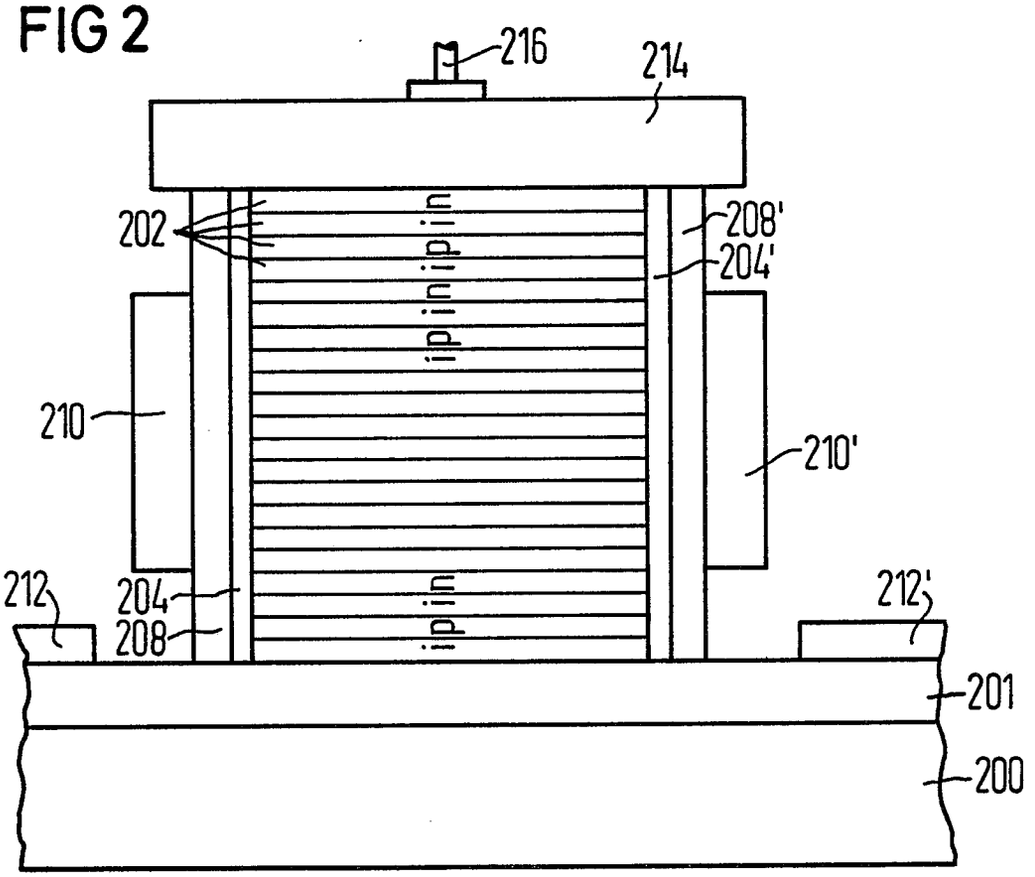

110
108
106
104
102
100

FIG 2


216
214
202
208'
204'
210
210'
212
204
208
212'
201
200

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 88 11 0412

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
|---|---|---|---|
| A | EP-A-0 091 831 (SAKAKI)<br>* Whole document * | 1-4,9, 11,12, 14,15, 17,18 | H 01 L 29/80<br>H 01 L 29/205<br>H 01 L 29/36<br>H 01 L 29/10 |
| A | EP-A-0 056 904 (FUJITSU LTD)<br>* Page 6, lines 15-25; page 8, line 21 - page 10, line 19 * | 1,9,14, 16 | |
| A | GB-A-2 171 250 (SONY CORP.)<br>* Page 2, lines 20-26; figures 5-7 * | 1-4,9, 11,12, 14,15, 17,18 | |
| A | JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 23, no. 2, February 1984, pages L61-L63, Tokyo, JP; K. INOUE et al.: "A new highly-conductive (AlGa)As/GaAs/(AlGa)As selectively-doped double-heterojunction field-effect transistor (SD-DH-FET)"<br>* Whole document * | 1-4,6,9 -15,17- 19 | TECHNICAL FIELDS SEARCHED (Int. Cl.4) |
| A | MICROELECTRONICS JOURNAL, vol. 13, no. 3, May/June 1982, pages 5-22, Benn Electronics Publications Ltd, Luton, GB; K. PLOOG et al.: "Growth and properties of new artificial doping superlattices in GaAs"<br>* Pages 5,6, paragraph 1; pages 12,13, paragraph 3.2; figure 1 * | 1,5,7-9 ,14,16 | H 01 L |

-/-

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 14-10-1988 | MORVAN D.L.D. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number

EP 88 11 0412

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int. Cl.4) |
|---|---|---|---|
| A | APPLIED PHYSICS LETTERS, vol. 47, no. 12, 15th December 1985, pages 1324-1326, American Institute of Physics, Woodbury, New York, US; Y.-C. CHANG et al.: "A new one-dimensional quantum well structure" * Whole document * | 1,2,5,9,12,14,17,18,20 | |

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| THE HAGUE | 14-10-1988 | MORVAN D.L.D. |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)