



(12)

## EUROPEAN PATENT APPLICATION

(21) Application number: 88307964.2

(51) Int. Cl.5: G06F 11/00

(22) Date of filing: 26.08.88

(30) Priority: 04.09.87 US 93179

(43) Date of publication of application:  
08.03.89 Bulletin 89/10

(84) Designated Contracting States:  
DE FR GB IT

(88) Date of deferred publication of the search report:  
10.04.91 Bulletin 91/15

(71) Applicant: DIGITAL EQUIPMENT  
CORPORATION  
146 Main Street  
Maynard, MA 01754(US)

(72) Inventor: Bruckert, William F.  
13 Mashpee Circle  
Northboro Massachusetts 01532(US)  
Inventor: Bissett, Thomas D.

21 Olesen Road  
Derry New Hampshire 03038(US)  
Inventor: Mazur, Dennis  
14 Saybrook Road  
Worcester Massachusetts 01604(US)  
Inventor: Munzer, John  
131 Kent Street  
Brookline Massachusetts 02146(US)  
Inventor: Bernaby, Frank  
28 Lela Avenue  
Haverhill Massachusetts 01830(US)  
Inventor: Bhatia, Jay H.  
384A Great Road, No. 304  
Acton Massachusetts 01720(US)

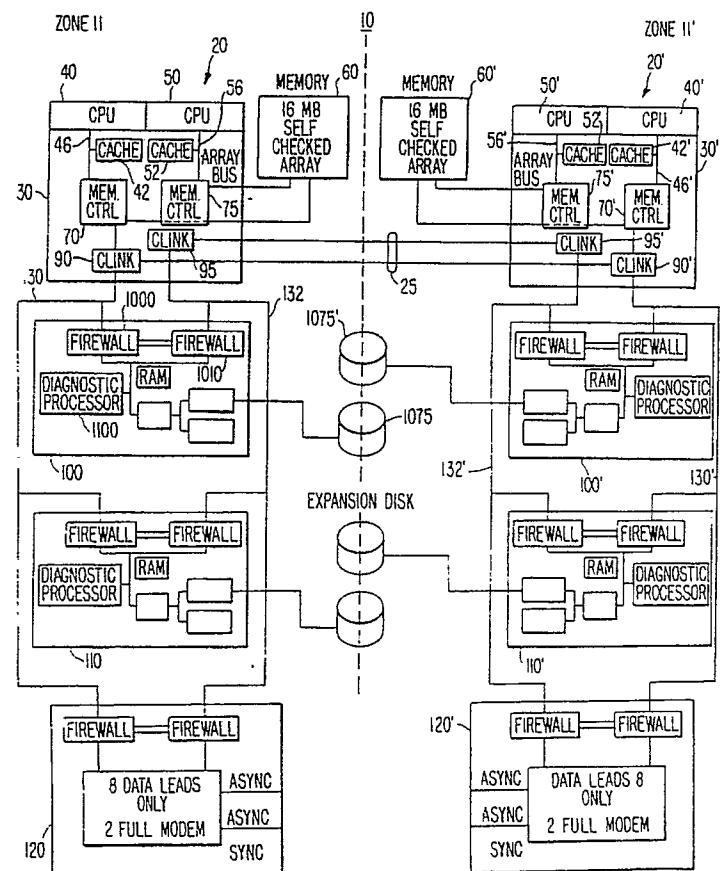
(74) Representative: Goodman, Christopher et al  
Eric Potter & Clarkson St. Mary's Court St.  
Mary's Gate  
Nottingham NG1 1LE(GB)

(54) Fault tolerant computer system with fault isolation and repair.

(57) A fault tolerant computer system has a central processing system which includes at least one set of data pathways, and executes a series of data processing instructions including the transfer of messages along the plurality of data pathways. At least one set of transaction data storage devices are coupled to the data pathways for storing a predetermined number of successive messages transferred most recently on the data pathways. Error checking

devices are included for detecting the presence of errors in the central processing system. Error storage devices are coupled to the transaction data storage devices and the error checking devices for causing the transaction data storage devices to cease storing additional messages in response to the detection of errors by the error checking device.

FIG. 1.





DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)		
A	EP-A-0 077 154 (STRATUS COMPUTER, INC.) * Page 26, line 29 - page 32, line 6; page 58, line 26 - page 60, line 24; page 77, lines 15-20 * - - -	1,9	G 06 F 11/00		
A	PATENT ABSTRACTS OF JAPAN, vol. 9, no. 137 (P-363)[1860], 12th June 1985; & JP-A-60 019 247 (NIPPON DENKI K.K.) 31-01-1985 * Abstract * - - -	1-3,9,10			
A	IEEE MICRO, vol. 4, no. 6, December 1984, pages 34-43; R. EMMERSON et al.: "Fault tolerance achieved in VLSI" * Page 36, column 2, line 9 - page 41, column 1, line 17 * - - -	1-3,7,9, 10			
A	US-A-4 380 058 (WAKAI) * Whole document * - - -	1-3,9,10, 19			
A	US-A-3 725 880 (SACHS) * Abstract; column 1, lines 30-63 * - - -	1,9,17			
A	US-A-4 030 074 (GIORCELLI) * Abstract; column 1, line 39 - column 8, line 48 * - - - -	1,4,9			
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)		
			G 06 F 11		
The present search report has been drawn up for all claims					
Place of search	Date of completion of search	Examiner			
The Hague	28 January 91	HERREMAN, G.L.O.			
CATEGORY OF CITED DOCUMENTS					
X: particularly relevant if taken alone					
Y: particularly relevant if combined with another document of the same category					
A: technological background					
O: non-written disclosure					
P: intermediate document					
T: theory or principle underlying the invention					
E: earlier patent document, but published on, or after the filing date					
D: document cited in the application					
L: document cited for other reasons					
&: member of the same patent family, corresponding document					