(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 308 997 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **88117268.8**

(51) Int. Cl.4: **G07F 3/02 , G07D 5/08**

(22) Date of filing: **05.11.84**

(30) Priority: **04.11.83 GB 8329533**
05.03.84 GB 8405721

(43) Date of publication of application:
29.03.89 Bulletin 89/13

(60) Publication number of the earlier application in accordance with Art.76 EPC: **0 146 251**

(84) Designated Contracting States:
AT BE CH DE FR GB IT LI LU NL SE

(71) Applicant: **MARS INCORPORATED**
6885 Elm Street
McLean Virginia 22101-3883(US)

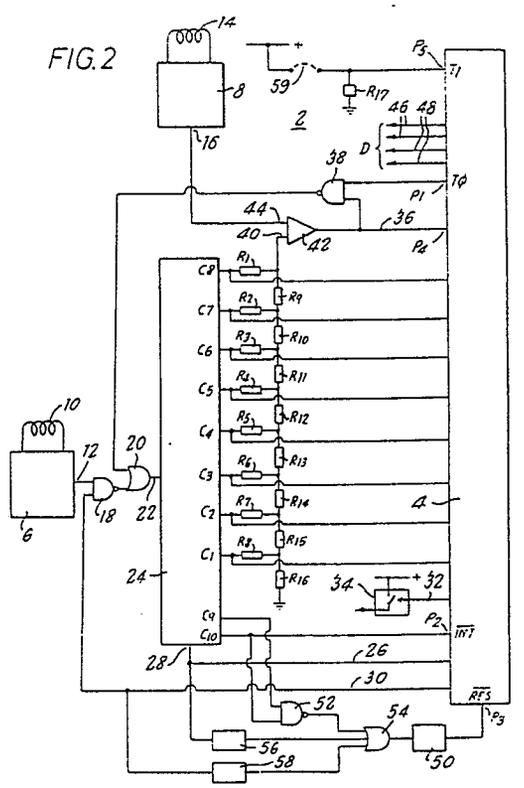
(72) Inventor: **Shouksmith, Eric**
26 Launcestone Close Earley
Reading Berkshire, RG6 2RY(GB)
Inventor: **Roberts, Mark Jeremy**
High Line Mansion Lane
Iver Bucks, SL0 9RG(GB)
Inventor: **Dean, Robert**
16 Mayflower Way
Franham Common Bucks, SL2 3TX(GB)

(74) Representative: **Burke, Steven David et al**
R.G.C. Jenkins & Co. 26 Caxton Street
London SW1H 0RJ(GB)

(54) Coin validators.

(57) In a coin validator, coins are checked to determine whether they are travelling too quickly through a sensing station to permit reliable validation, and, if so, they are rejected.

FIG.2



EP 0 308 997 A2

COIN VALIDATORS

This invention relates to coin validators.

US-A-3797628 discloses a coin validator in which the velocity of an inserted coin is normalised and then caused to alter in accordance with the properties of the coin. The token velocity is measured in order to determine whether the coin is acceptable.

In accordance with the invention, there is provided a coin validator which does not normalise the speed of coins delivered to a sensing station thereof, characterised by means responsive to a value indicative of the speed at which a coin is travelling through said sensing station for providing a signal indicating that the coin is not acceptable in response to determining that the coin has travelled too fast through the sensing station.

It is thus possible to check whether the coin is passing through the sensing station at a speed which is too fast to enable reliable validation. It will be noted that the validator is testing the suitability of the coin's flight for validation, rather than the arrangement in US-A-3797628 in which velocity is measured as a test of a coin's properties.

The coin speed may be detected by measuring the interval between the coin passing two separate sensors and/or by measuring the rate of change of an output signal of a single sensor. Such an arrangement is particularly valuable in small coin validators where the distance between a coin entry slot and the coin sensors is short and therefore there is severe risk that the coin's motion when it reaches the sensor will not have stabilised to such an extent as to ensure accurate test results.

Arrangements embodying the invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 schematically illustrates a coin passageway of a coin validator in accordance with the invention;

Fig. 2 is a schematic circuit diagram of the coin validator;

Fig. 3 is a circuit diagram of an arrival sensor of the validator;

Fig. 4 is a circuit diagram of a material sensor in a modified embodiment of the validator;

Fig. 5 is a schematic diagram of the circuit of the modified embodiment; and

Figs. 6A and 6B are views of opposite sides of a printed circuit board carrying a testing coil used in each embodiment of the validator.

Referring to Figs. 1 and 2, the validator 2 has a main processor 4 which uses an arrival/diameter sensing circuit 6 and a material/thickness sensing circuit 8 for detecting the arrival of coins and for testing those coins and providing signals indicating whether a coin is genuine, and if so the type of the coin.

The arrival/diameter sensing circuit 6 has a sensing coil 10 connected in an oscillator circuit to be described in more detail subsequently.

The coil 10 is situated at one side of a coin passageway 7. The passageway 7 is inclined and canted so that coins, such as that shown at 9, travel down the passageway 7 in the direction A with their faces in contact with the side of the passageway on which the coil 10 is located. The circuit 6 is so arranged that the signal appearing at the output 12 of the circuit 6 has a frequency which alters as a coin passes the coil 10, and which peaks at a level predominantly dependent upon the diameter of the coin.

The material/thickness sensing circuit 8 has a coil 14 disposed at the opposite side of the coin passageway 7 from the coil 10. The coil 14 is connccted in an oscillator circuit, and the circuit is so arranged that the signal appearing at the output terminal 16 is attenuated in response to a coin passing the coil 14. The peak level of attenuation is predominently dependent upon the material from which the coin is made, and the thickness of the coin. Because the coin contacts the side of the passageway 7 opposite to that on which the coil 14 is located, the spacing of the coin from the coil will depend upon coin thickness, so that it is ensured that this will have a significant effect on the output of circuit 8.

The processor 4 is a CMOS 8048 (or CMOS 8049) microprocessor. This has terminals P1, P2, P3, P4 and P5, which can be used as, respectively, a clock output terminal, an interrupt input terminal, a reset input terminal, an input/output terminal and a testable input terminal. There are also address/data bus terminals D. The remaining terminals referred to below are further input/output terminals which, unlike the terminal P4 which is used at different times as both an input and an output, are only required to perform a single input or output function in the particular circuit shown. The processor 4 also has power supply terminals, clock input terminals etc. which are not shown in Fig 2.

The processor 4 has in its instruction set a HALT instruction, which when executed causes the processor to enter a quiescent state, in which no processing operations are carried out and the power consumption is substantially reduced. The processor can be switched back to an active state by a signal on the interrupt terminal P2.

The validator is installed in a pay telephone.

Under normal circumstances the entire validator is switched off. When the handset is lifted, parts of the validator circuit, including the processor 4 and arrival/diameter sensing circuit 6, but excluding the material/thickness sensing circuit 8, are switched on.

The processor 4 then executes an initialisation routine, following which a HALT instruction is executed so that the processor enters a quiescent state.

The oscillations appearing at the output terminal 12 of the arrival/diameter sensing circuit 6 are delivered via gates 18 and 20 to the clock input 22 of a counter 24. The counter has output terminals C1 to C10. The counter counts the pulses until a signal appears at count output C10. This signal is delivered to the interrupt terminal P2 of the processor 4 in order to cause the processor to enter its active state. The processor then proceeds to issue on line 26 a clear signal which is delivered to the clear terminal 28 of the counter 24. The processor also delivers on line 30 a signal for closing the gate 18.

The processor 4 then temporarily opens the gate 18 for a predetermined duration. The counter 24 is thus caused to count the pulses appearing at the output terminal 12 of the circuit 6. The final count, which appears at the count terminals C1 to C8, is noted by the processor 4 which has input/output terminals connected to those count terminals, before the counter 24 is cleared by the processor.

The processor 4 has a memory into which the count is stored, the arrangement being such that the memory always stores the previous count measured in this way. The processor determines that a coin has arrived at the coil 10 if the second count exceeds the first by more than a predetermined number. Thus, a coin is detected in response to an increasing frequency appearing at the output terminal 12.

Assuming that a coin has not been detected, the processor 4, after clearing the counter 24, opens the gate 18 and executes the HALT instruction. The processor 4 will then adopt its quiescent state until a signal appears once more at the count terminal C10.

The processor is thus regularly caused to enter its active state in order to determine whether or not a coin has arrived, and if not the processor re-enters its quiescent state. This may occur at intervals of, for example, 5 milliseconds, the processor being active for a period of less than 1 millisecond during each of these intervals. The average current consumption of the processor 4 is thus low.

Assuming that the arrival of a coin is detected, the processor 4 then continues to sample the frequency of the signal appearing at the terminal 12. The frequency continuously increases until a peak is reached, following which the frequency decreases until an idling level is reached, after the coin has left the coil. The processor 4 recognises and stores the peak and idle levels, and thereafter calculates the ratio of these two levels in order to produce a diameter-indicating value.

At some stage, in response to detecting the arrival of a coin, the processor issues on line 32 a signal for operating a power switch 34. This causes the power supply to be connected to the material/thickness sensor circuit 8.

The processor 4 may be arranged to switch on the material/thickness sensor circuit 8 immediately after the detection of the arrival of a coin to ensure that the operation of circuit 8 has stabilised by the time the coin reaches coil 14. Alternatively, to conserve power, the processor 4 may be arranged to switch on the circuit 8 after detection of the peak in the output frequency of the signal at terminal 12, or possibly when the processor 4 has detected that the frequency has dropped to an idling level.

As a further alternative, the processor 4 may be arranged to check that the diameter value is appropriate for a genuine coin of a denomination which the validator is arranged to accept before switching on the circuit 8. In this may, the crcuit 8 will not be operated unless the coin has an acceptable diameter, and thereby pov;er consumption is further reduced.

Once the diameter value has been calculated and the circuit 8 switched on, the processor 4 issues a signal on line 30 to close the gate 18, so that no more pulses from the circuit 6 can reach the counter 24. The counter is cleared, and the processor issues a signal on line 36 to open a gate 38. This permits the gate to pass pulses from the terminal P1 via the gate 20 to the clock input terminal 22 of the counter 24.

The counter 24 thus counts up at a constant, predetermined rate. The count terminals C1 to C8 are connected via resistors R1 to R8 to respective points on a series resistor network R9 to R16 coupled between ground and one input 40 of a comparator 42. The other input 44 of the comparator 42 is connected to the output terminal 16 of the circuit 8.

The resistors R1 to R16 act as potential dividers in such a manner that a signal at any one of the count output terminals C1 to C8 will produce, at the input terminal 40 of the comparator 42, a voltage corresponding to the respective count terminal. The effect of this is to cause the voltage at the terminal 40 to increase progressively in a stepwise manner as the count reached by the counter 24 increases. Thc resistors are of close tolerance to ensure an even distribution of the voltages produced as the count increases.

After the processor issues the signal from terminal P4 which opens the gate 38, the terminal is switched so that it now behaves as an input terminal. As the voltage at the input terminal 40 of the comparator 42 increases, it will eventually rise past the voltage at terminal 44 from the circuit 8. At this time, the output of comparator 42 will switch logic levels, thus closing gate 38 and preventing further pulses from reaching the counter 24. This change in logic levels will also be sent to terminal P4 of the processor 4, which is detected by the processor 4 and used to indicate that the count output terminals C1 to C8 should be read. The count will be a digital representation of the analog voltage at terminal 16 of the circuit 8.

The counter 24 is then cleared, the terminal P4 switched to behave as an output terminal, and the gate 38 re-opened so as to permit the processor 4 to take a further measurement of the output signal appearing at terminal 16 of the circuit 8.

The comparator 42 has an open-collector output so that this and the terminal P4 can be directly connected to the gate 38, whereby each can control gate 38, without interfering with each other.

The processor 4 repeatedly measures the output appearing at terminal 16, and determines from these measurements the idle value. This is done before the coin reaches the sensor coil 14, and may be initiated by the circuit 6 sensing the departure of the coin from coil 10. Then as the attenuation increases during the movement of the coin past the sensor, the peak value of the signal is determined. This is preferably achieved by storing successive measurement values. The processor detects when these values alter in such a manner as to indicate that the attenuation is decreasing due to the coin leaving the sensor. The processor then averages the stored values, preferably ignoring the more recent measurements so that the values used represent measurements taken when the coin was substantially at the mid-point of its travel past the sensor. For example, the processor may be arranged to take the average of the first, say, four of the last twelve measurements. Of course, instead of taking an average measurement by summing a predetermined number of values and then dividing by that number, so as to compare the resulting value with a stored range, the processor could simply sum the values without dividing the result; the stored ranges would be correspondingly greater.

The ratio of the idle and peak values is determined in order to produce a thickness/material-indicating value. The idle value is measured before the peak so that the decision as to whether an accept/reject gate should be opened can be made very soon after the peak has been reached, and therefore little space is required between the coil 14 and this gate.

At the end of the thickness/material testing operation, the circuit 8 is switched off, the counter 24 is cleared and the gate 18 is re-opened to allow the pulses appearing at output terminal 12 of circuit 6 to reach the counter 24.

For each of the denominations of coins which the validator 2 is designed to accept, the processor 4 stores information defining a diameter range and a material/thickness range. For example, the processor 4 may store upper and lower limits of the respective ranges, or alternatively may store a single value from which the processor can calculate, using a stored or predetermined tolerance, the appropriate range.

The processor 4 compares the two measurements, i.e. the diameter value and the thickness/material value, with the ranges for the respective coins, and determines that a valid coin of a particular denomination has been received if both values fall within the appropriate ranges for that denomination. In that case, the processor 4 produces on one or both of data lines 46 an ACCEPT signal, and on lines 48 a binary signal indicating the denomination of the coin.

The coin validator 2 is intended for installation in various types of machines, e.g. gaming machines. In some of these, it is desired that the machine be capable of accepting a first range of coins (e.g. 5p, 10p, 20p and 50p U.K. denomination coins), and in other machines a different range (e.g. 10p, 20p, 50p and £1 coins). To cater for this without requiring different types of validator to be manufactured, the validator is arranged to recognise all five coins and generate ACCEPT signals on lines 46 in accordance with the range of coin denominations within which a received coin lies. Thus, if the denomination of a received coin falls within both ranges (e.g. for 10p, 20p and 50p coins) an ACCEPT signal is generated on both lines 46, and the coin denomination indicated by the data on lines 48. If the coin denomination lies in only one range (e.g. 5p), then only one of the lines 46 (corresponding to that range of denominations) carries the ACCEPT signal while the lines 48 carry data representing the denomination 5p. When a coin denomination which belongs only to the other range is received (e.g. a £1 coin), the same data on lines 48 can be generated, but this time the ACCEPT signal is generated on the other of the lines 46.

Accordingly, the same validator can be installed in any of the above types of machines, and in each case it is merely necessary to select which of the lines 46 is to be used in accordance with the range of denominations which the machine is intended to accept.

There is a danger that the processor 4 may

"hang-up", i.e. may cease to operate properly, for example due to electrical noise or interference. To avoid problems caused by this faulty operation, the validator 2 has a reset pulse generator 50, which produces a pulse of predetermined length to reset the processor 4 in the event that any one of three conditions indicative of "hang-up" occurs.

As mentioned above, the output of counter terminal C10 is used to deliver a signal to interrupt terminal P2 of processor 4, which causes the processor to issue a signal on line 26 to clear the counter 24. If this does not occur, due to faulty operation of the processor 4, the counter will not be cleared and will continue to count in response to pulses from the crcuit 6. Eventually, an output signal will appear at terminal C9 of the countcr 24, and the simultaneous appearance of signals at terminals C9 and C10 will be detected by a gate 52, which will deliver an activating signal via a gate 54 to the circuit 50 to cause resetting of the processor 4.

The gate 54 has two further inputs connected to respective detection circuits 56 and 58. Each of these receives a signal at its input and delays that signal, but the signal appears at the output only if the input signal lasts for more than a predetermined amount of time. Circuit 56 is connected to the clear terminal 28 of the counter 24, so that if after issuing a signal to clear the counter the processor suddenly begins to behave incorrectly, the signal at the clear input terminal 28 will persist longer than it should, and this will be detected by the circuit 56 which will issue a signal via gate 54 to circuit 50 to cause resetting of the processor 4.

The circuit 58 has its input connected to the line 30 which carries the signal issued by the processor 4 to close the gate 18. The longest time for which the gate 18 is closed occurs when the processor is measuring the output of circuit 8. The delay of circuit 58 is set to be longer than this time. If the processor 4 begins to behave incorrectly during the thickness/material measuring operation, and the gate 18 thus remains closed, this will be detected by the circuit 58 and cause resetting of the processor.

Even if the processor 4 begins to behave improperly, it may nevertheless execute an interrupt routine, initiated by the signal delivered to terminal P2, in a correct manner. To detect this situation, the processor 4 is arranged to set a number of internal flags while executing the arrival detection routine. During the interrupt routine, the processor 4 checks to see that these flags are set. If they are not, because the main routine was not being executed properly, the processor 4 executes an instruction which causes it to be reset.

The validator is preferably made in such a way that the coin measurements which are made produce fairly predictable results for given denominations, so that the parameter ranges stored by the processor 4 do not have to be specially worked out for each validator. However, to accommodate slight variations between validators, and changes in a particular validator due to ageing or drift, the sensing circuits 6 and 8 can be adjusted in respect of frequency and/or gain to vary their outputs.

To facilitate the making of adjustments, the processor 4 can be switched into a test mode by connecting a link 59 between a power supply rail and the testable input terminal P5, which terminal is normally held at a low potential by a resistor R17 connected to ground. At the same time, the operator connects a device to the data lines D to display the potentials on these lines.

After switching the validator into the test mode, the operator inserts a coin of a particular denomination (e.g. 10p), and determines what signals are produced on the data lines 46 and 48 in response thereto. The inserted coin is preferably specially selected so that its properties are of an average value with respect to the normal variations expected of coins of that denomination.

The processor 4 operates as described up to and including the obtaining of digital values representing the measurements made by the sensing circuits 6 and 8. At that time the processor checks the terminal P5, and if this is found to be high the processor then executes a test routine instead of continuing with the validation operations described above.

In the test routine, the values derived from the sensing circuits 6 and 8 are compared with a special set of "test ranges", instead of with the normal acceptability ranges. These test ranges correspond to the ranges used to determine whether an acceptable coin of the particular denomination (e.g. 10p) has been received, except that they are narrower than the acceptability ranges.

In the test mode, the processor's output on data lines 46 and 48 is in a different format, and has a different meaning, from the outputs in the normal validation operation. In the test mode, if both measured properties upon insertion of the coin are within the respective test ranges, a high-level logic signal is applied to all the output lines 46 and 48. If the value derived from the sensing circuit 6 exceeds or falls below the respective range, the lines 46 are caused to carry a binary value of "10" or "01", respectively. Similarly, if the value derived from sensing circuit 8 exceeds or falls below its respective test range, the value produced on lines 48 is "10" or "01", respectively. An output value of "0000" on lines 46 and 48 is reserved for situations in which the sensing circuits 6 and 8 produce incorrect values which are clearly not due merely to poor adjustment (e.g. values

resulting from two coins being detected at the same time, a poor coin flight path, etc.) so that the operator will be able to take appropriate action.

Referring now to Fig. 3, the arrival/diameter sensing circuit 6 comprises the coil 10 connected in a Colpitt's oscillator circuit. In the particular configuration used here, an amplifier formed by a transistor 60 has a feedback loop including the coil 10 connected between its collector and base. The coil 10 is connected in series with an adjustment circuit comprising variable resistor 61 connected in parallel with inductance 63. Capacitors 62 and 64 are each connected between, on the one hand, a respective end of the circuit formed by components 10, 61 and 63, and on the other hand, ground. The variable resistor 61 is used for the adjustment made during the test mode.

Resistors 66, 68 and 70 are provided for biasing the transistor 60 into conduction. The load on the transistor 60 is distributed between a collector impedance (formed by a resistance RL and an inductance LL) and the resonant circuit formed by the components 10, 61, 62, 63 and 64.

Thus, the output voltage appearing across the capacitor 62 is dependent to a large extent on the fixed impedance RL and LL. Thus, although the passage of a coin in proximity to the coil 10 will cause some attenuation of this voltage, the degree of attenuation will be relatively small, because the load impedance does not change, compared with a circuit such as those used in the above-mentioned British Patent Specification No. 2093620, in which the coil is connccted to the collector current path and therefore has a very substantial effect on the output voltage. The incorporation of inductance LL increases the stability of the output voltage with changes in frequency.

Accordingly, the circuit 6 can be arranged so that it normally consumes a low level of current, but nevertheless will provide an output signal which will not disappear even when a coin is in close proximity to the coil 10. This makes the circuit particularly suitable for use as an arrival sensing circuit. To reduce cost and power consumption, the circuit is, as mentioned above, also used for measuring purposes. It has been found that if the coil 10 is suitably arranged for diameter measurement, and the frequency of the output rather than the amplitude is used for measurement purposes, good discrimination can be achieved with the same low operating current as is used for arrival sensing.

A modified version of the above embodiment will now be described with particular reference to Figures 4 and 5. This embodiment operates in a similar manner to the one described above, and similar reference numbers will be used for similar parts, except for the points set out below.

In the previously described embodiment, the sensing circuit 8 produced an output whose amplitude was sensed in order to provide an indication of the material and thickness of the coin. In the embodiment of Figures 4 and 5, the sensor is used for providing an output which is predominantly dependent upon the material of the coin, and somewhat less dependent upon thickness. In this case there are two coils 14 and 14′ (the latter of which is shown in phantom in Figure 1) positioned on respective sides of the coin passageway. As in the earlier embodiment, the amplitude of the output of the sensing circuit 8 is used for measurement purposes; however in the present embodiment the frequency of the output is used as an additional measurement. In total, there are therefore three measurements, which are compared with respective stored ranges, and as a consequence of this the rejection of non-genuine coins is made much more reliable.

Figure 4 shows the circuit 8, which is additionally suitable for use in the first-described embodiment. The circuit has a standard oscillator configuration, using a transistor 100. The two coils 14 and 14′, which are in field-aiding relationship,are connected in series with each other and with a variable inductance 102. The inductances are connected in the collector path of the transistor 100. The emitter path includes a variable resistor 104.

The output of the circuit 8 is indicated at 106, and is taken from the collector of transistor 100. As a coin passes between the sensors 14 and 14′, both the frequency and amplitude of the output signal vary.

These parameters can be adjusted using the variable inductance 102 and the variable resistor 104. Preferably the frequency is adjusted first using the variable inductance 102, as this will also have an effect on amplitude.

Referring to Figure 5, in this embodiment the microprocessor 4 is of the Motorola 6805 family. This has a plurality of ports which can be used as input or output terminals. In the arrangement shown, terminals I1 to I3 are used as input terminals, and terminals 01 to 011 are used as output terminals.

The microprocessor has an internal counter which can be clocked at regular intervals so that it acts as a timer the operation of which can be initiated or halted by the application of a signal to terminal T1. Alter natively, the counter can be used to count pulses appearing on terminal T1. This internal counter is used in place of the counter 24 of Figure 2.

The microprocessor 4 can operate a switch 150 which selectively delivers the output pulses of sensing circuit 6 to a divide-by-four circuit 152 formed of two flip-flops. The output of circuit 152 is delivered to the terminal T1. The internal counter

can thus be used for counting pulses from the circuit 6 and hence measuring the frequency of the output. The states of the flip flops in circuit 152 are detected on input lines I2 and I3 so that two extra bits of resolution can be achieved. When counting is commenced, the circuit 152 is released from its set state by changing the signal appearing on output terminal 05. After the measuring operation, the circuit 152 is held in a set state which allows the input terminal T1 to receive other signals, as will be described.

In particular, the output of sensing circuit 8 is delivered via another microprocessor-controlled switch 154 to terminal T1 so that the frequency of this output can be measured. In this case the divide-by-four circuit 152 is not required as the coils 14, 14′ are driven at a substantially lower frequency than the coil 10.

The output of the sensing circuit 8 is also delivered via a rectifying circuit 156 to a comparator 158. Another input of the comparator 158 is connected to a junction between a constant current charging circuit 160 and a capacitor 162.The charging circuit 160 can be switched on or off by an output terminal 02 of the microprocessor 4.

In operation, in order to measure the amplitude of the output of sensing circuit 8, the microprocessor switches on the charging circuit 60 and at substantially the same time starts the internal counter, which is acting in its timer mode. This causes the voltage on the capacitor 162 to rise linearly. As soon as this voltage equals that from the rectifying circuit 156, the output of comparator 158 switches polarity, which is detected at input terminal I1. The microprocessor senses this, and determines the count reached by the internal timer, which is digital representation of the amplitude of the output of sensing circuit 8.

The output of the comparator 158 is delivered to the timer terminal T1 via a microprocessor-controlled switch 164. This is to ensure that the operation of the timer is halted immediately the output of the comparator 158 changes state; this avoids problems caused by the delay in the microprocessor first detecting the change in state at terminal I1 and then halting the timer.

Thus, the internal counter measures (a) frequency of output of sensing circuit 6, (b) frequency of output of sensing circuit 8, and (c) amplitude of output of sensing circuit 8.

The circuit operates substantially as described with reference to Figure 2. However, after the coin starts to leave the coil 10, the microprocessor 4 first measures the amplitude of the output of sensing circuit 8, then measures its frequency, and then once more measures the amplitude. The two amplitude measurements are averaged to obtain the idle amplitude value. The frequency measurement takes place over a sufficiently long time that any slight fluctuations in frequency do not affect the result.

Subsequently, amplitude measurements are repeatedly taken. As the coin enters the space between coils 14 and 14′, the amplitude will start to decrease. Successive amplitude measurements are compared, and once the amplitude stops decreasing, a frequency measurement is made. Thereafter, a succession of further amplitude measurements are made, and when they indicate that the coin is leaving the coils 14, 14′, a plurality of these measurements (preferably excluding the most recent measurements) are averaged to obtain the peak amplitude value.

This operation gives rise to three measurement values, each comprising the ratio of an idle value with the peak value, which are compared with respective ranges to determine whether the coin is valid, and if so the denomination of the coin.

If the coin is valid, an ACCEPT signal is delivered on output terminal 07, and the denomination of the coin is indicated by the signals on lines 08 and 09.

The microprocessor 4 also times the interval between the coin arriving at the coil 10 and departing from the coils 14, 14′. If this interval is less than a predetermined value, it is indicative of a coin which is travelling too fast for accurate measurement, and the coin is therefore rejected. Also, the microprocessor checks the successive values of the frequency of the sensing circuit 6, and successive values of the amplitude of sensing circuit 8, and if either of these is altering too rapidly the coin is rejected on the basis that it is travelling either too fast or in an unstable manner.

When an operator wishes to test the operation of the validator, he operates a switch or connects a link to issue a pulse to an interrupt terminal INT of the microprocessor 4 (instead of using a test terminal T1 as in Fig. 2). This causes the microprocessor to execute an interrupt routine which results in signals being generated on a serial data output line 010 in response to a coin passing the coils 10, 14, 14′. The operator inserts a coin having known characteristics, such as a coin of a particular denomination which has been chosen so as to have substantially exactly average properties. The microprocessor compares the three measurements produced by this coin with special ranges which are narrower than those normally used for this denomination of coin, and as a consequence the data on output line 010 indicates what adjustments need to be made to the sensing circuits 6 and 8.

The operator has a test device connected to receive the data from output terminal 010 and clock pulses from output terminal 011. The device includes logic circuitry which decodes the data so as

to provide a display indicating whether and in which manner any of the components 61 (Fig. 3), 102 and 104 (Fig. 4) need adjustment.

The switches 150, 154 and 164 of Fig. 5 may be simply logic gates, such as NAND gates.

Referring to Figs. 6A and 6B, in conjunction with Fig 1, a preferred form of the coil 10 will now be described. The coil is formed by a printed circuit etched on both sides of a double-sided printed circuit board 80. Fig. 6A shows the side 82 of the board 80 which in use is more closely adjacent the coin path, and Fig. 6B shows the opposite side 84. The board 82 is located in a plane parallel to the side walls of the passageway 7.

On each side, the printed circuit board has been etched to form a spiral conductive pattern having an overall substantially circular configuration.

Referring to Fig. 6A, the side 82 carries two terminal portions 86 and 88. The conductive path starts from the terminal portion 86 and then spirals inwardly to an inner contact portion 94.

The terminal portions 86 and 88 are positioned directly opposite corresponding terminal portions on the side 84 which are respectively labelled 86′ and 88′, and may if desired be connected thereto by respective plated through-holes. The inner contact portion 94 is connected via a plated through-hole to a corresponding contact portion 94′ on the side 84. From there, the printed circuit pattern spirals outwardly to terminal portion 88′.

Thus, the terminal portions 86 and 88′ form the opposite ends of the coil 10. In use, the field created by the portion of the coil 10 on side 82 will extend in the same direction as the field produced by the part of the coil on the side 84.

The respective parts of the coil 10 on the opposite sides of the board 80 can be positioned very accurately with respect to the coin path, so that there is good consistency in the measurements produced by the coil 10 from validator to validator. Thus, only minor adjustments using the variable resistor 61 of Fig. 3 are needed.

The bottom edge of the coil 10 is located at or preferably slightly below the bottom of the coin path so that if a coin passing the coil 10 tends to bounce there is little or no effect upon the coil area covered by the coin and hence upon the measured value.

The term "coin" has been used herein to cover not only genuine coins but also non-genuine coins or other items which might be received by the validator.

Claims

1. A coin validator which does not normalise the speed of coins delivered to a sensing station thereof, characterised by means (4) responsive to a value indicative of the speed at which a coin is travelling through said sensing station for providing a signal indicating that the coin is not acceptable in response to determining that the coin has travelled too fast through the sensing station.

2. A validator as claimed in claim 1, wherein said signal providing means (4) is operable in response to a value indicative of the total travel time through the sensing station.

3. A validator as claimed in claim 1 or 2, wherein said signal providing means (4) is operable in response to a value indicative of the rate of change of a signal produced in response to a coin coming into proximity to a coin-testing sensor (14,14′).

FIG. 1

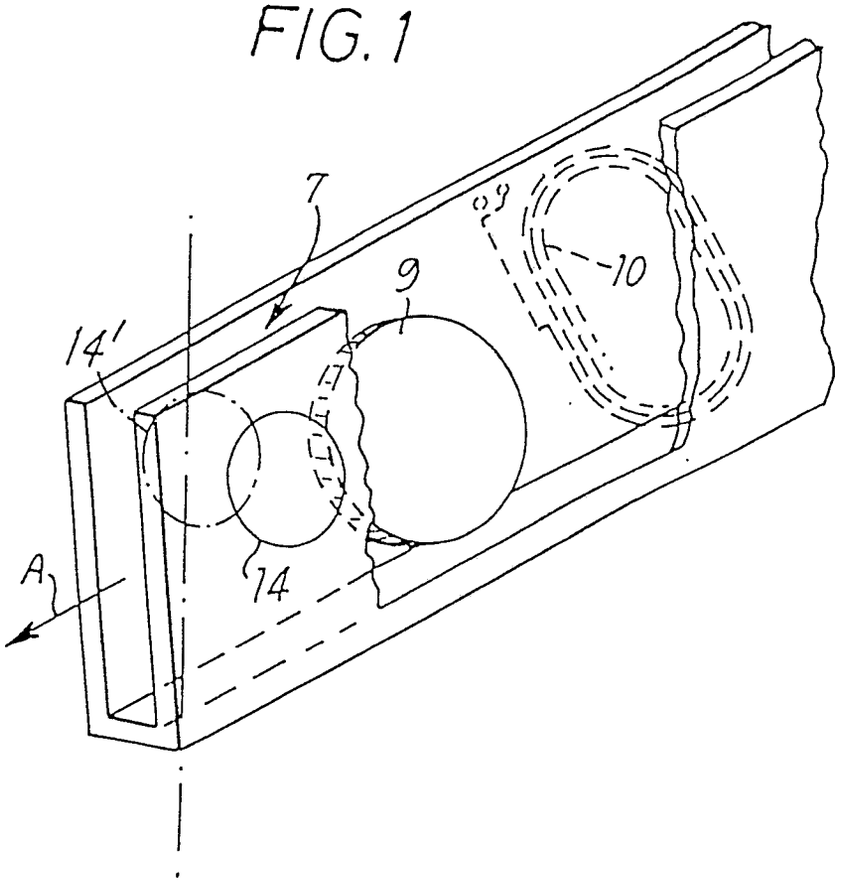


FIG. 3

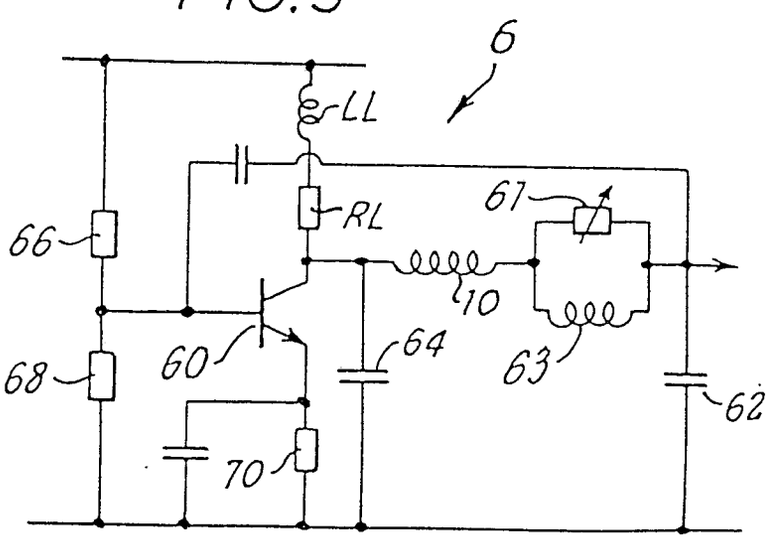


FIG. 2

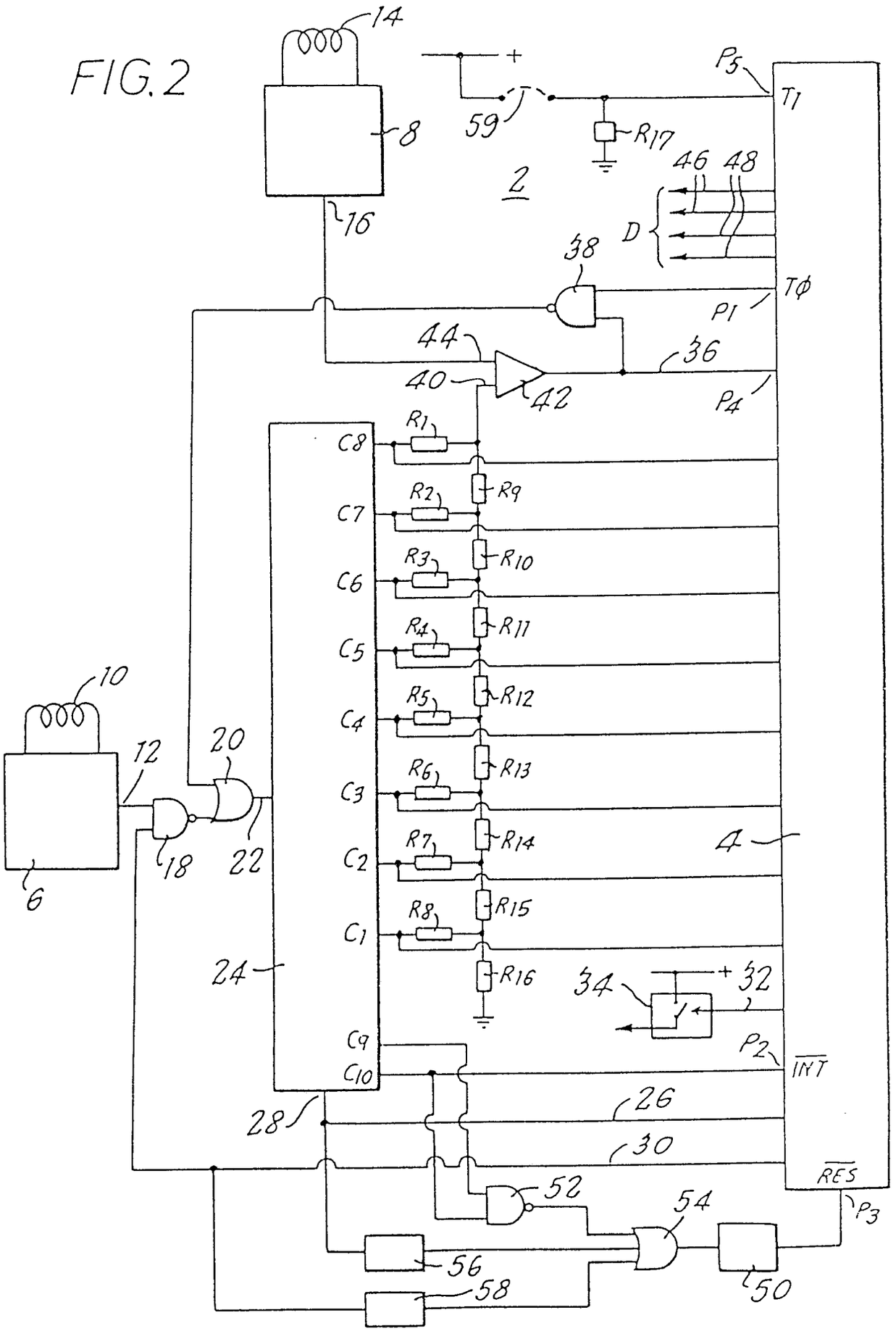

14
8
16
59
R17
2
P5
T1
46
48
D
38
TΦ
P1
44
36
40
42
P4
C8
R1
R9
C7
R2
R10
C6
R3
R11
C5
R4
R12
C4
R5
R13
C3
R6
R14
C2
R7
R15
C1
R8
R16
24
4
34
32
C9
C10
P2
INT
26
28
30
RES
P3
52
54
56
58
50
10
12
20
18
22
6

FIG. 4

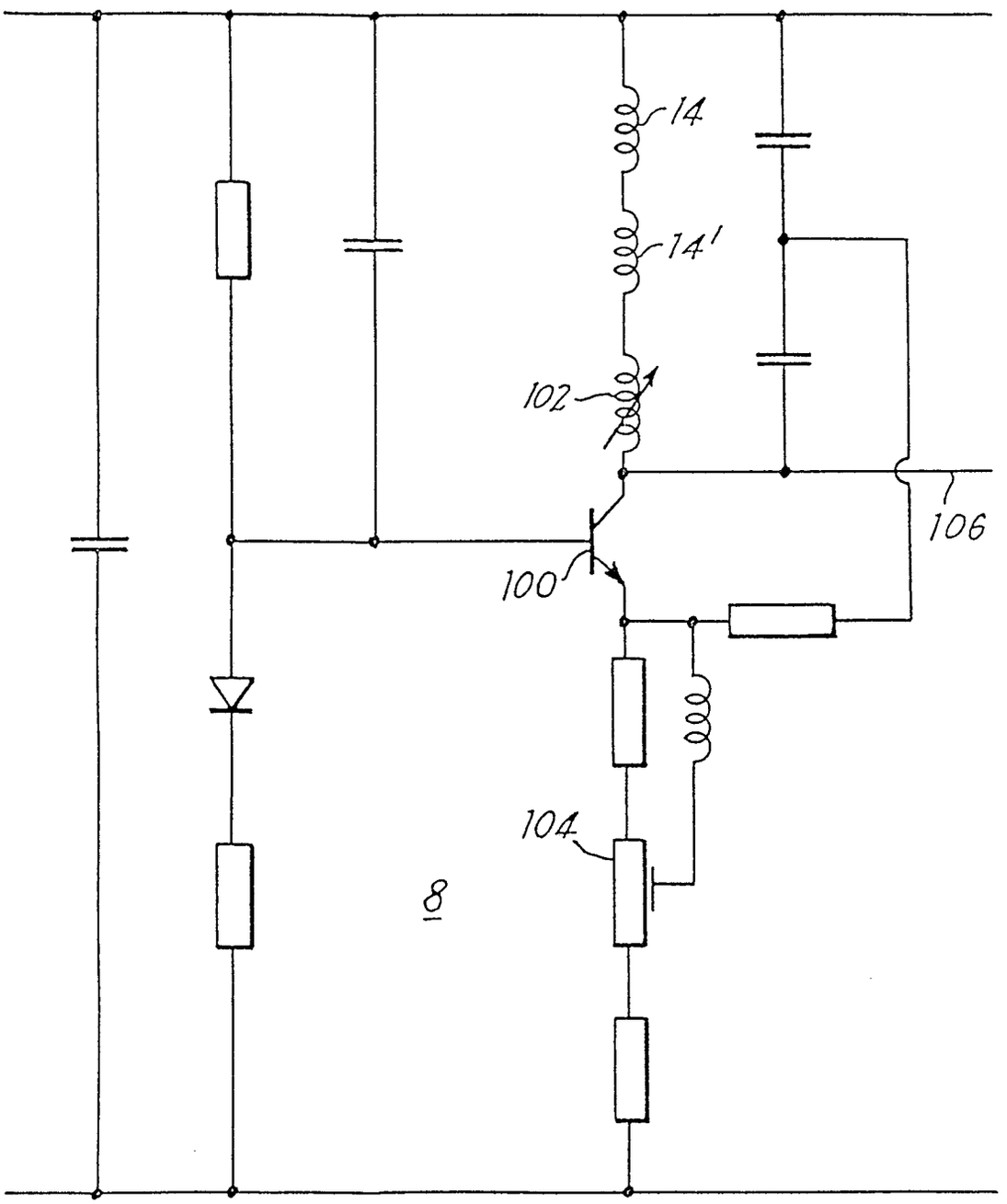
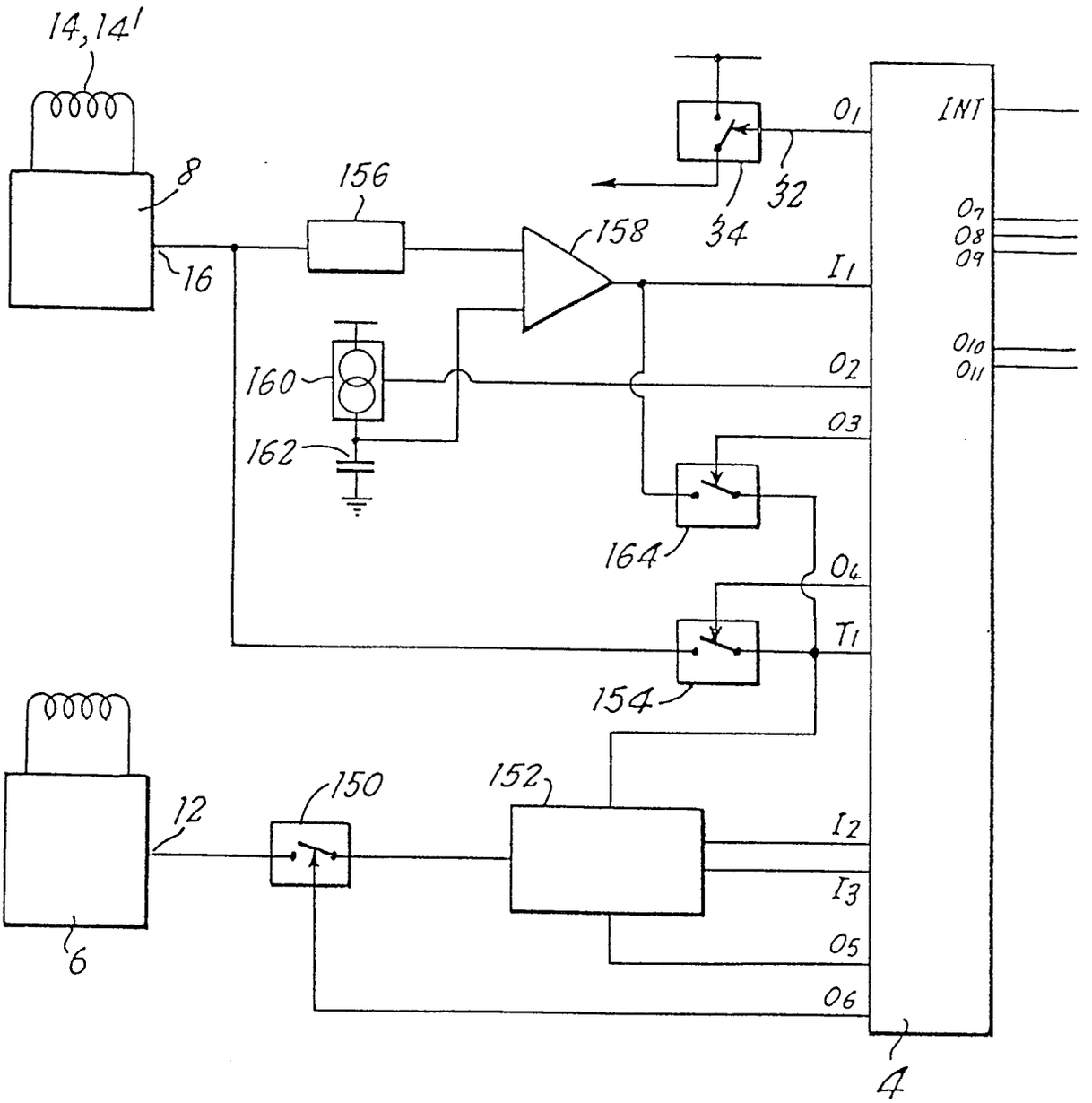


FIG. 5


14, 14'
8
16
156
158
160
162
164
154
150
152
12
6
4
32
34
O1
O2
O3
O4
O5
O6
O7
O8
O9
O10
O11
INT
I1
I2
I3
T1

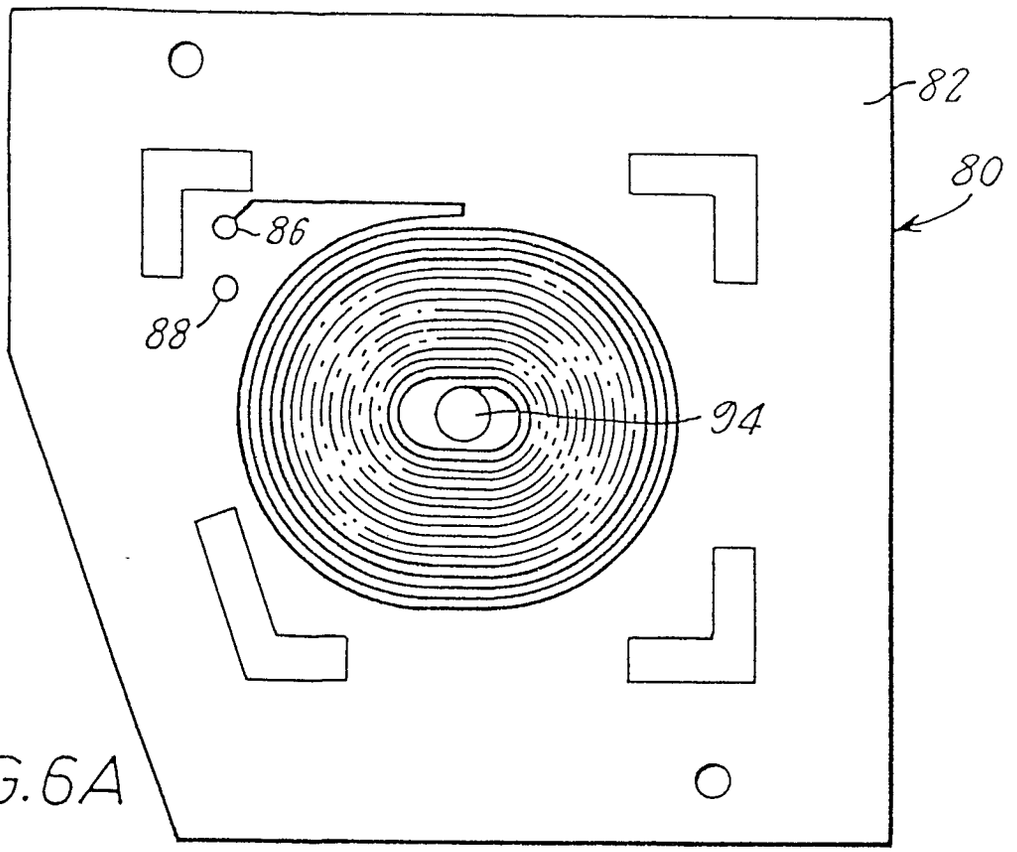


FIG.6A

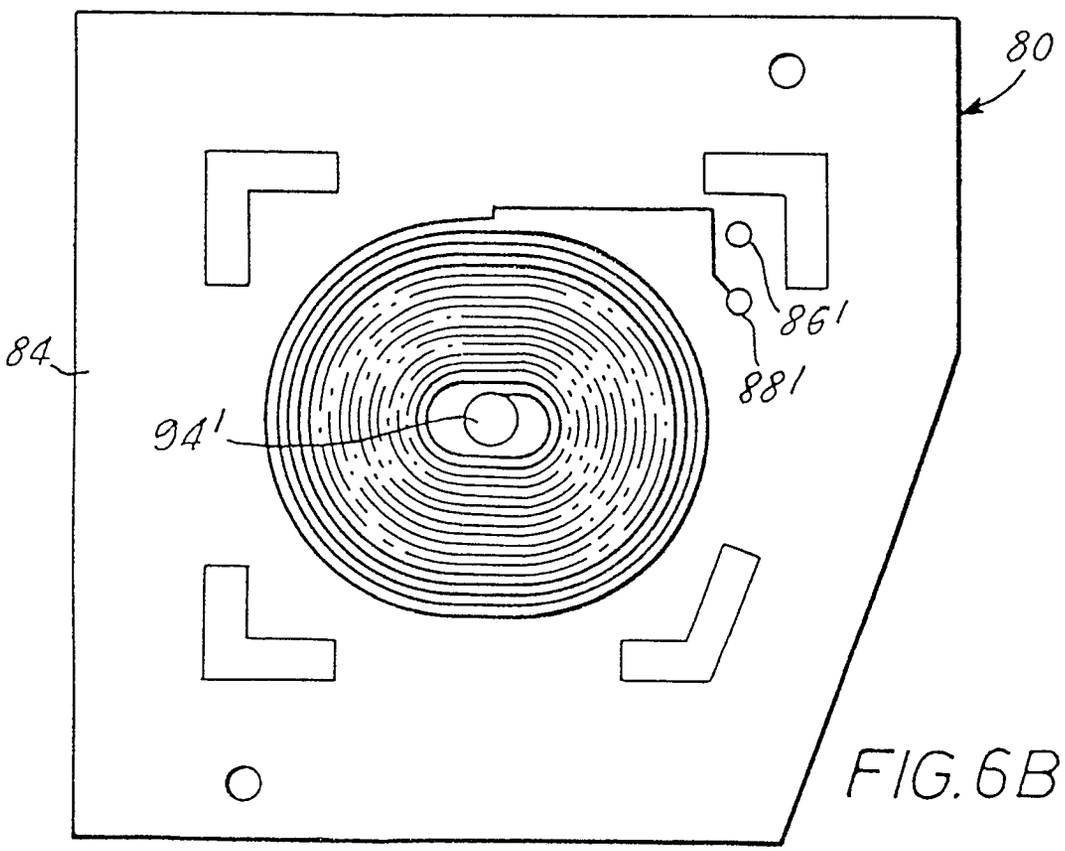


FIG.6B