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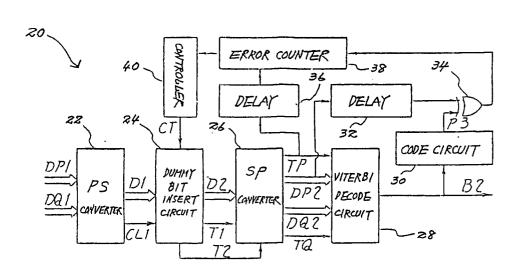
#### (54) Decoder.

The decoder is capable of decoing on a maximum likelihood basis coded symbols of equivalently high coding rate which are produced by deleting those code bits which are located at particular positions in a time sequence of convolutional symbols of low coding rate. The decoder includes a serial-to-parallel (SP) converter for converting a serial data sequence from a dummy bit inserter into parallel sequences. The frequency division phase of the SP converter is

determined by a second timing signal which the dummy bit inserter produces in synchronism with a dummy bit insertion phase. As code synchronization is established, frequency division phase synchronization is automatically established. This eliminates the need for the repetitive trial for frequency division phase synchronization only and thereby reduces a synchronization capture time.

FIG. 3







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