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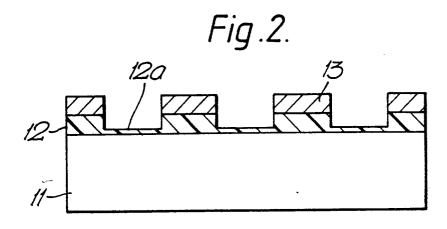
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94 Plasma etching process.

© A polysilicon layer or a single crystal silicon substrate is plasma etched in a two staged process. The first stage was a non-selective anisotropic etch to define a desired pattern by etching part way through the polysilicon. The second stage was a selective etch to secure remaining polysilicon and expose the substrate.

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PLASMA ETCHING PROCESS.

This invention relates to plasma or dry etching process, and in particular to a plasma etching process for the treatment of polycrystalline silicon (polysilicon).

A recent development in semiconductor technology is the introduction of devices incorporating both field effect transistors and bipolar transistors on a common single crystal silicon substrate. A particularly advantageous form of this technology employs polysilicon for the formation of field effect transistor gates and bipolar transistor emitters. Devices incorporating those features are described for example in our published specification No. 2, 173, 638 (P.D. Scovell et al 15-13-8). The use of polysilicon for this purpose requires the use of a selective etching process that will selectively remove polysilicon without significant attack of the underlying single crystal silicon. The etchant materials currently employed for this purpose have only a moderate selectivity. In addition, the isotropic etching characteristics of the materials currently used causes significant undercut of the polysilicon. This is clearly undesirable as it limits the accuracy with which circuit features may be defined and in turn limits the packing density of devices on the chip. A further disadvantage of conventional etchants is that they function by reactive ion etching (RIE). This results in radiation damage of devices formed in the single crystal substrate.

The object of the invention is to minimise or to overcome these disadvantages.

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According to the invention there is provided a process for selectively etching a polysilicon layer provided on a single crystal silicon substrate, the method including exposing selected regions of the polysilicon layer to a first non-selective anisotropic plasma so as to etch said regions but without exposing the substrate, and exposing said selected regions to a second selective isotropic plasma whereby the remaining polysilicon is removed from said regions without significant attack of the substrate.

According to the invention there is further provided, a process for selectively etching a polysilicn layer provided on a single crystal substrate, the method including masking the layer, exposing the unmasked regions of the layer to a first non-selective anisotropic plasma etch comprising sulphur hexafluoride or a mixture of sulphur hexafluoride (SF₆) containing at least 20 volume per cent of oxygen whereby a major portion of exposed polysilicon is removed, exposing the structure to a second selective isotropic plasma etch comprising sulphur hexafluoride containing a trace quantity of oxygen whereby the remaining polysilicon is removed without significant attack of the single crystal substrate.

An exposure of the structure to an isotropic etch is restricted to the final stages of etching, there is very little undercut of the polysilicon layer.

We have found that a plasma comprising sulphur hexafluoride displays a significant degree of selectivity between polycrystalline and single crystal silicon, whilst a plasma comprising a mixture of sulphur hexofluoride and at least 20 per cent oxygen display a high degree of anistropy. By performing the major portion of the etching process with an anistropic plasma, the problems of undercut is avoided. The remainder of the polysilicon is then etched with the selective isotropic plasma without significant risk of damage to the underlying substrate.

An embodiment of the invention will now be described with reference to the accompaning drawings in which Figure 1 to 3 illustrate successive stages in the formation of a polysilicon pattern on a single crystal substrate.

Referring to the drawings, a single crystal silicon substrate 11 (Figure 1) is provided with a surface layer 12 of polycrystalline silicon (polysilicon). A photolithographic mask 13 is applied to the polysilicon layer and the structure is exposed to a radio frequency plasma comprising a mixture of sulphir hexafluoride and oxygen. This provides anisotropic ecthing of the exposed polysilicon down towards the substrate. Most of the polysilicon is removed from the exposed regions leaving only a thin layer 12a (Figure 2) in those regions. As this process is anisotropic there is substantially no undercut of the unexposed polysilicon regions. Thus, the device features can be accurately defined.

Typically we employ 20 to 40 volume percent of oxygen, and preferably 25 percent of oxygen, in the gas mixtures. Etching may be performed at pressures of 0.4 to 1.0 torr. The etching site for this first anisotropic, stage is about 8000 A (800 um) per minute.

The anisotropic etching process is followed by a second selective isotropic etching process. The partially etched structure is exposed to a radio frequency plasma comprising pure sulphur hexafluoride or sulphur containing trace quantities of oxygen. The oxygen concentration in this isotropic plasma should not exceed 5 volume percent.

This plasma removes the remaining polysilicon from the exposed regions to form the structure shown in Figure 3. As this etch is selective, there is very little attack of the substrate. In particular, we have found a sulphur hexafluoride plasma at a pressure of 2 torr has a selectivity between polysilicon and single crystal

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silicon of about 5:1. The etch rate of polysilicon under these conditions is 215A/min whilst that of single crystal silicon is only 42A/min. Typically we employ pressures of 0.8 to 3.0 torr. After completion of the second etching stage the mask 13 is removed and the structure of Figure 3 may then be further processed to form a finished device.

Of the two etching stages, only the first stage displays significant ion etching. During this first stage the substrate is protected from radiation damage by the remaining polysilicon. The first stage ensures accurate defination of the polysilicon pattern whilst the second stage is required to remove only a thin silicon layer and thus displays no significant undercutting of the polysilicon pattern.

The following example illustrates the invention.

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Example

A single crystal silicon wafer was provided with a surface coating of polysilicon 7500 A (750 um) in thickness. The polysilicon was provided with a photolithographic mask and was then anisotropiccally etched in a plasma containing sulphur hexafluoride and oxygen under the following conditions:-

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0.450 torr.		
135 scc/min		
61 scc/min		
13.56 MHz		
100 watts		
88 cm ²		
36 seconds		
4000 A (400 um)		

The partially etched wafer was then exposed to a plasma containing pure sulphur hexafluoride to effect isotropic selective etching of the remaining polysilicon. The etching conditions were as follows:-

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Pressure	2.0 torr.	
SF₅ flow rate	90 scc/min	
Generator frequency	13.56 MHz	
Generator power	60 watt	
Etch time	16.5 min	
Etch depth	3500 A (350 um)	

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Examination of the wafer after completion of the second etching stage revealed substantially no undercutting and subsequently no erosion of the underlying substrate. This Example demonstrates the feasibility of the etching process described above.

In the above Example the gas flow rate has been expressed in standard cc/minute, i.e. that gas flow rate are reduced to equivalent flow rates at atmospheric pressure.

Whilst the above process has been described with particular reference to devices incorporating both bipolar and field effect transistors, it is not of course limited to this application but may be generally employed in semiconductor fabrication.

Claims

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- 1. A process for selectively etching a polysilicon layer provided on a single crystal silicon substrate, the method including exposing selected regions of the polysilicon layer to a first non-selective anisotropic plasma so as to etch said regions but without exposing the substrate, and exposing said selected regions to a second selective isotropic plasma whereby the remaining polysilicon is removed from said regions without significant attack of the substrate.
- 2. A process for selectively etching a polysilicn layer provided on a single crystal substrate, the method including masking the layer, exposing the unmasked regions of the layer to a first non-selective anisotropic plasma etch comprising sulphur hexafluoride (SF₆) containing at least 20 volume per cent of oxygen

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whereby a major portion of exposed polysilicon is removed, exposing the structure to a second selective isotropic plasma etch comprising sulphur hexafluoride or a mixture of sulphur hexafluoride and a trace quantity of oxygen whereby the remaining polysilicon is removed without significant attack of the single crystal substrate.

- 3. A process as claimed in Claim 1 or 2, characterised in that the first etching stage is performed at a pressure of 0.4 to 1.0 torr.
- 4. A process as claimed in claims 1, 2 or 3, characterised in that the second etching stage is performed at a pressure of 0.8 to 3.0 torr.
 - 5. A semiconductor device treated by a process as claimed in any one of the preceding claims.
- 6. A semiconductor device as claimed in claim 5 and incorporating both bipolar and field effect transistors.

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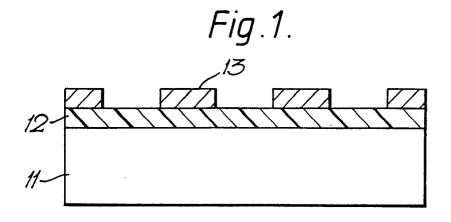
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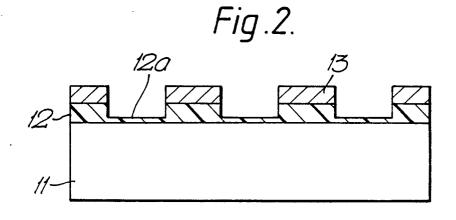
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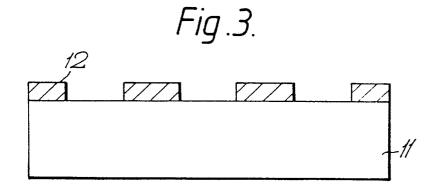
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EUROPEAN SEARCH REPORT

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i		DERED TO BE RELEVA	Relevant	CLASSIFICATION OF THE	
Category	Citation of document with ii of relevant pa	ndication, where appropriate, ssages	to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)	
Y	EP-A-0 149 683 (SO * Figures 22,23; pa page 16, line 12 *		1,4-6	H 01 L 21/31 H 01 L 21/285	
Y	PATENT ABSTRACTS OF 94 (E-171)[1239], 2 JP-A-58 16 533 (NIP 31-01-1983 * Whole document *	Oth April 1983; &	1,4,5		
D,Y	GB-A-2 173 638 (ST * Abstract *	C)	6		
A	EXTENDED ABSTRACTS, pages 750-752, abst BENNETT et al.: "Po flexible diode reac * Page 750, paragra paragraph 3 *	ract no. 301; R.S. lycide etching in a tor"	1-6		
A	EXTENDED ABSTRACTS, October 1985, page 313; G.C. CHERN et poly-si etching" * Whole document *	474, abstract no.	2	TECHNICAL FIELDS SEARCHED (Int. Cl.4)	
A	EXTENDED ABSTRACTS, 1984, page 135, abs Pennington, New Yor al.: "The effect of with O2, H2, N2 and	k, US; R. PINTO et dilution of SF6	1-6		
	The present search report has b	een drawn up for all claims			
	Place of search	Date of completion of the search	<u> </u>	Examiner	
THE	HAGUE	24-05-1989	GOR:	[P.	
X: par Y: par doc A: tecl O: nor	CATEGORY OF CITED DOCUMENTS T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filling date Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filling date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document				

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