

12

EUROPEAN PATENT APPLICATION

21 Application number: **89301981.0**

51 Int. Cl.⁴: **H 01 L 21/20**

H 01 L 29/205, H 01 L 29/267

22 Date of filing: **28.02.89**

30 Priority: **01.03.88 JP 45820/88**

43 Date of publication of application:
06.09.89 Bulletin 89/36

84 Designated Contracting States: **DE FR GB**

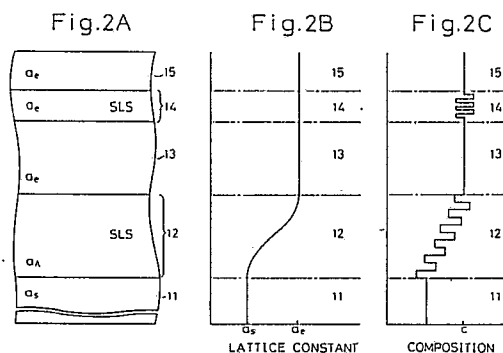
71 Applicant: **FUJITSU LIMITED**
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

72 Inventor: **Okuda, Hiroshi**
781-6, Tomuro
Atsugi-shi Kanagawa 243 (JP)

74 Representative: **Billington, Lawrence Emlyn et al**
HASELTINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT (GB)

54 **Semiconductor substrate comprising wafer substrate and compound semiconductor layer.**

57 A semiconductor substrate including a top epitaxial compound layer comprising: a single-crystalline semiconductor wafer substrate (11); a strained layer superlattice (SLS) structure layer (12) having a lattice constant varying from that of the wafer substrate (11) to that of the top compound semiconductor layer (15) and formed on the wafer substrate (11); a semiconductor buffer layer (13) having the same lattice constant as that of the top compound semiconductor layer (15) and formed on the SLS structure layer (12); another SLS structure layer (14) for filtering dislocations having a fixed lattice constant equal to that of the top semiconductor layer (15) and formed on the buffer layer (13); and the top semiconductor layer (15) formed on the another SLS structure layer (14).



Description

SEMICONDUCTOR SUBSTRATE COMPRISING WAFER SUBSTRATE AND COMPOUND SEMICONDUCTOR LAYER

The present invention relates to a semiconductor substrate for a production of semiconductor transistor devices or photonic devices, and more particularly, to a compound semiconductor substrate comprising a single-crystalline semiconductor wafer substrate, a compound semiconductor epitaxial layer, and a strained layer superlattice (SLS) structure layer between the wafer layer and the epitaxial layer.

Generally, a single-crystalline wafer of a binary compound semiconductor, such as GaAs and InP, is used as a substrate for epitaxial growth of a compound semiconductor layer thereon.

For the epitaxial growth of a good quality compound semiconductor layer on the wafer substrate, it is necessary to coincide the lattice constant of the compound semiconductor epitaxial layer with that of the wafer substrate, which considerably limits the composition range of the epitaxial layer.

Recently, it has become necessary to form (grow) a compound semiconductor layer having a different lattice constant from that of the wafer substrate for semiconductor lasers having a relatively short emission wavelength. On the other hand, proposals have been made for producing GaAs grown on Si (GaAs/Si) substrates corresponding to a single-crystalline GaAs substrate, enlarging the wafer size, increasing the mechanical strength and thermal conductivity, and reducing costs, compared with the single-crystalline GaAs substrate. The GaAs has a lattice constant larger than that of Si by about 40%.

Where such a compound semiconductor layer including the GaAs layer is grown, an SLS structure layer is integrated as a buffer between the substrate and the grown layer, for the following reasons:

(1) The SLS buffer layer reduces dislocations in the grown compound semiconductor layer by preventing an extension of threading dislocations from the substrate into the compound semiconductor layer, due to the strain field in the SLS; and

(2) The SLS buffer layer allows the epitaxial growth of the compound semiconductor layer having a different lattice constant from that of the substrate by absorbing a lattice mismatch without generating threading dislocations, due to an alternate expansion and contraction of strained very thin layers of SLS.

However, SLS buffer layers having both the satisfactory effects of (1) filtering of dislocations and (2) compensation of a lattice mismatch, have not yet been developed.

Figures 1A, 1B and 1C are fragmented sectional views of trial compound semiconductor substrate comprising at least a single-crystalline compound semiconductor wafer substrate, an SLS buffer layer, and an epitaxial compound semiconductor layer.

In these drawings, 1 indicates a GaAs (single-crystalline) wafer substrate having a lattice constant a_s , 2 indicates an $\text{In}_x\text{Ga}_{1-x}\text{P}$ graded layer, the component ratio "x" of which decreases from the wafer

substrate side upward, 3 indicates an SLS structure layer of $\text{In}_{0.24}\text{Ga}_{0.76}\text{P}$ - $\text{In}_{0.76}\text{Ga}_{0.24}\text{P}$, and 4 indicates an epitaxially grown $\text{In}_{0.3}\text{Ga}_{0.7}\text{P}$ layer having a lattice constant a_e . Reference 5 indicates an SLS structure layer having a lattice constant a_1 approximate to that (a_s) of the wafer substrate 1, 6 indicates an SLS structure layer having a lattice constant a_2 approximate to that (a_e) of the $\text{In}_{0.3}\text{Ga}_{0.7}\text{P}$ layer 4, and 7 indicates generated threading dislocations. Reference 8 indicates an SLS structure layer having the same lattice constant as that of the GaAs wafer substrate, and 9 indicates an epitaxially grown In Ga P layer having the same lattice constant.

In the first compound semiconductor substrate shown in Fig. 1A, the lattice constant a_s of the wafer substrate 1 is not equal to the lattice constant a_e of the $\text{In}_{0.3}\text{Ga}_{0.7}\text{P}$ layer 4 and the $\text{In}_x\text{Ga}_{1-x}\text{P}$ graded layer 2 compensates this lattice mismatch. The wafer substrate 1 has a dislocation density on the order of $\sim 10^4 \text{ cm}^{-2}$, and the graded layer 2 has a dislocation density on the order of $\sim 10^8 \text{ cm}^{-2}$, since dislocations are newly generated in the graded layer 2. The SLS structure layer 3 reduces the dislocations, but the dislocation density is still on the order of $\sim 10^6 \text{ cm}^{-2}$. Since dislocation in the epitaxial grown $\text{In}_{0.3}\text{Ga}_{0.7}\text{P}$ layer 4 follow the dislocations in the SLS structure layer 3, the layer 4 has a dislocation density on the order of $\sim 10^6 \text{ cm}^{-2}$. Furthermore, the compound semiconductor substrate is warped to some extent.

In the second compound semiconductor substrate shown in Fig. 1B, the lattice constants have the relationship " $a_e > a_2 > a_1 > a_s$ or $a_e < a_2 < a_1 < a_s$ ", and dislocations are unavoidably newly generated in the lower SLS structure layer 5. Although the upper SLS structure layer 6 reduces a dislocation density, the $\text{In}_{0.3}\text{Ga}_{0.7}\text{P}$ layer 4 has a dislocation density about 2 orders higher in magnitude than that of the wafer substrate 1. In this case, warping of the second compound semiconductor substrate is remarkably reduced.

In the third compound semiconductor substrate shown in Fig. 1C, since the SLS structure layer 8 substantially reduces dislocations, the epitaxially grown In Ga P layer 9 has a remarkably reduced dislocation density. Nevertheless, the lattice constants of the wafer substrate 1 and the layers 8 and 9 are the same, and thus the SLS structure layer 8 has the filtering effect but no compensation effect.

As mentioned above, interposition of an SLS structure layer or combined SLS structure layers between the wafer substrate and the epitaxial compound semiconductor layer cannot simultaneously attain the two above effects.

Embodiments of the present invention may provide a compound semiconductor substrate including an epitaxially grown compound semiconductor layer having a different lattice constant from that of a single-crystalline wafer substrate, and a low dislocation density.

Embodiments of the present invention may also

improve a buffer between the wafer substrate and the epitaxial compound semiconductor layer.

According to the present invention there is provided a semiconductor substrate including a top epitaxial compound semiconductor layer comprising: a single-crystalline semiconductor wafer substrate; a first strained layer superlattice (SLS) structure layer having a lattice constant varying from that of the wafer substrate to that of the top compound semiconductor layer, and formed on said wafer substrate; a compound semiconductor buffer layer having the same lattice constant as that of the top compound semiconductor layer, and formed on the SLS structure layer; a second SLS structure layer for filtering dislocations having a fixed lattice constant equal to that of the top compound semiconductor layer, and formed on the buffer layer; and the top semiconductor layer formed on the second SLS structure layer.

The wafer substrate may be composed of a compound semiconductor (e.g., GaAs, InP) or of silicon (Si).

Embodiments of: the present invention will be described below, by way of example only, with reference to the accompanying drawings, in which:

Figs. 1A to 1C are fragmented sectional views of trial semiconductor substrates;

Fig. 2A is a fragmented sectional view of a compound semiconductor substrate according to the present invention;

Fig. 2B is a graph of lattice constant variation of the substrate of Fig. 2A;

Fig. 2C is a graph of composition variation of the substrate of Fig. 2A;

Fig. 3A is a graph of lattice constant variation of an SLS structure layer formed on a wafer substrate;

Fig. 3B is a graph of composition variation of the SLS structure layer of Fig. 3A; and

Fig. 4A is a graph of lattice constant variation of another type SLS structure layer formed on the wafer substrate;

Fig. 4B is a graph of composition variation of the SLS structure layer of Fig. 4A;

Fig. 5 is a partially enlarged sectional view of the substrate of Fig. 2A.

Fig. 6A is a partially enlarged sectional view of the substrate of Fig. 2A;

Fig. 6B is a graph of lattice constant of the layers of Fig. 6A; and

Fig. 6C is a graph of composition variation of the layers of Fig. 6A.

Referring to Figs. 2A, 2B and 2C, a compound semiconductor substrate according to the present invention comprises a single-crystalline semiconductor wafer substrate 11, a first SLS structure layer 12, a compound semiconductor buffer layer 13, a second SLS structure layer 14, and a top compound semiconductor epitaxial layer 15.

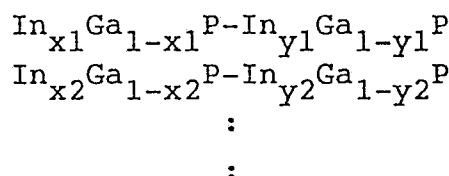
The wafer substrate 11 has a lattice constant a_s and is a compound semiconductor (e.g., GaAs) wafer or a silicon (Si) wafer. The top epitaxial layer 15 has a desired lattice constant a_e (e.g., for a desired emission wavelength of a semiconductor laser) and is composed of a binary, ternary or quaternary III-V

compound semiconductor, such as GaAs, InGaP (e.g., $\text{In}_{0.25}\text{Ga}_{0.75}\text{P}$, InP, InGaAsP and InGaAlP).

The first SLS structure layer 12 has a lattice constant gradually varying from the " a_s " of the wafer substrate 11 to the " a_e " of the top epitaxial layer 15, as shown in Figs. 2B and 3A.

Where the $\text{In}_{0.25}\text{Ga}_{0.75}\text{P}$ layer 15 is epitaxially grown above the GaAs wafer substrate 11, the SLS structure layer 12 consists of, e.g., $\text{In}_x\text{Ga}_{1-x}\text{P}$ - $\text{In}_y\text{Ga}_{1-y}\text{P}$ with the composition ratios "x" and "y" varying from 0.63 to 0.38 and from 0.37 to 0.12, respectively, as shown in Fig. 2C and 3B. Each of the InGaP thin layers has a thickness of from 5 to 30 nm, preferably 20 nm. The periodic number of the $\text{In}_x\text{Ga}_{1-x}\text{P}$ - $\text{In}_y\text{Ga}_{1-y}\text{P}$ SLS is from 10 to 50, preferably 30.

As shown in Figs. 4A and 4B, it is possible to form the first SLS structure layer 12, the lattice constant of which varies stepwise, of SLS layers 12A, 12B, ... having different lattice constants a_{A1} , a_{A2} , ... of, e.g.:



Where the $\text{In}_{0.25}\text{Ga}_{0.75}\text{P}$ layer 15 is epitaxially grown above the GaAs wafer substrate 11, the SLS structure layer 12 consists of:

a 15-period GaP (10 nm)- $\text{Ga}_{0.83}\text{In}_{0.17}\text{P}$ (10 nm) SLS layer 12A;

a 15-period $\text{Ga}_{0.91}\text{In}_{0.09}\text{P}$ (10 nm)- $\text{Ga}_{0.75}\text{In}_{0.25}\text{P}$ SLS layer 12B; and

a 15-period $\text{Ga}_{0.91}\text{In}_{0.09}\text{P}$ (10 nm)- $\text{Ga}_{0.67}\text{In}_{0.33}\text{P}$ SLS layer 12C.

The first SLS structure layer 12 changes its lattice constant and has the effects whereby strain caused by lattice constant variation is relieved and the upward propagation of dislocations is suppressed.

As shown in Fig. 5, the strain relief is attained by introducing small dislocations 16, and a threading dislocation 17 generated in the layer 12 is bent to prevent it from extending to the surface of the layer 12.

The compound semiconductor buffer layer 13 has a lattice constant equal to the " a_e " of the top epitaxial layer 15, is epitaxially grown on the SLS structure layer 13, and is composed of a binary, ternary or quaternary III-V compound semiconductor, such as GaAs, InGaP (e.g., $\text{In}_{0.75}\text{Ga}_{0.25}\text{P}$), GaAsP (e.g., $\text{GaAs}_{0.5}\text{P}_{0.5}$), InP and InGaAsP. The buffer layer 13 has a thickness of 0.1 to 3 μm , preferably from 0.3 to 2 μm , and is sufficiently large for the total thickness of the SLS structure layers 12 and 14, since the buffer layer 13 fixes (stabilizes) the lattice constant (a_e) changed by the SLS structure layer 12, absorbs residual internal stress, and serves as a substrate having the lattice constant " a_e " for the second SLS structure layer 14. Where the $\text{In}_{0.25}\text{Ga}_{0.75}\text{P}$ layer 15 is epitaxially grown above the

GaAs wafer substrate 11, preferably the $\text{GaAs}_{0.5}\text{P}_{0.5}$ buffer layer is 1 μm thick.

The second SLS structure layer 14 (Figs. 2A and 6A) has a fixed lattice constant " a_e " equal to that of top epitaxial layer 15, as shown in Figs. 2B and 6B. Where the $\text{In}_{0.25}\text{Ga}_{0.75}\text{P}$ layer 15 is epitaxially grown, the SLS structure layer 14 consists of, e.g., $\text{In}_x\text{Ga}_{1-x}\text{P}-\text{In}_y\text{Ga}_{1-y}\text{P}$ with the composition ratios " x " and " y " being 0.35 and 0.14, respectively, as shown in Figs. 2C and 6C. Each of the InGaP thin layers has a thickness of 5 to 30 nm, preferably 15 nm, and the periodic number of the $\text{In}_x\text{Ga}_{1-x}\text{P}-\text{In}_y\text{Ga}_{1-y}\text{P}$ SLS is from 5 to 30, preferably 10.

When the strained lattice constant of a SLS is equal to that of the substrate (i.e., the fixed lattice constant of the SLS structure layer 14 is equal to that of the buffer layer 13), it is possible to prevent a generation of new dislocations and to effectively reduce (filter) the dislocation density, unless the thickness of each thin layer of SLS exceeds a certain critical thickness. Therefore, the SLS structure layer 14 prevents an extension of threading dislocations to the surface of the layer 14.

The layers 12 to 15 are formed by a conventional metalorganic chemical vapor deposition (MOCVD) process or molecular beam epitaxy (MBE) process.

A GaAs/Si substrate with SLS can be composed of a Si single-crystalline silicon wafer 11; a first SLS structure layer 12 of a 40 period $\text{GaAs}_{1-x}\text{P}_x$ (20 nm)- $\text{GaAs}_{1-y}\text{P}_y$ (20 nm) with the composition ratios " x " and " y " varying from 0 to 0.8 and from 0.2 to 1, respectively; a GaAs buffer layer 13 about 1 μm thick; a second SLS structure layer 14 of a 15 period $\text{GaAs}_{0.8}\text{P}_{0.2}$ (15 nm)-GaAs (15 nm); and a GaAs epitaxial layer 15. In this case, it is possible to adopt $\text{In}_x\text{Ga}_{1-x}\text{As}-\text{GaAs}_{1-y}\text{P}_y$ SLS for the SLS structure layer 14.

As will be apparent from the above, the combination of the first SLS structure layer for compensating a lattice mismatch and a relating thick compound semiconductor buffer layer and the second SLS structure layer for filtering dislocations, attains the top compound semiconductor epitaxial layer having a lattice constant different from that of the wafer substrate and an extremely low density of crystal defects, i.e., low dislocation density. Since it is possible to design the changing of lattice constant and inhibition of dislocation propagation individually, the first and second SLS structures can be optimized for these purposes, respectively.

It will be obvious that the present invention is not restricted to the above-mentioned embodiments and that many variations are possible for persons skilled in the art without departing from the scope of the invention.

Claims

1. A semiconductor substrate including a top epitaxial semiconductor layer comprising:
 - a single-crystalline semiconductor wafer substrate;
 - a first strained layer superlattice structure layer having a lattice constant varying from that of

said wafer substrate to that of said top semiconductor layer and formed on said wafer substrate;

a compound semiconductor buffer layer having the same lattice constant as that of said top semiconductor layer and formed on said strained layer superlattice structure layer;

a second strained layer superlattice structure layer for filtering dislocations having a fixed lattice constant equal to that of said top semiconductor layer and formed on said buffer layer; and

the top semiconductor layer formed on said second strained layer superlattice structure layer.

2. A semiconductor substrate according to claim 1, wherein said wafer substrate is composed of a compound semiconductor.

3. A semiconductor substrate according to claim 2, wherein said compound semiconductor is GaAs.

4. A semiconductor substrate according to claim 1, wherein said wafer substrate is composed of silicon.

5. A semiconductor substrate according to claim 4, wherein said top semiconductor layer is composed of GaAs.

6. A semiconductor substrate according to any preceding claim, wherein the lattice constant of said first strained layer superlattice structure layer varies continuously.

7. A semiconductor substrate according to any of claims 1 to 5, wherein the lattice constant of said first strained layer superlattice structure layer varies stepwise.

8. A semiconductor substrate according to any preceding claim, wherein each of layers of said strained layer superlattice structure layer has a thickness of from 5 to 30 nm.

9. A semiconductor substrate according to any preceding claim, wherein said buffer layer has a thickness of from 0.1 to 3 μm .

Fig.1A

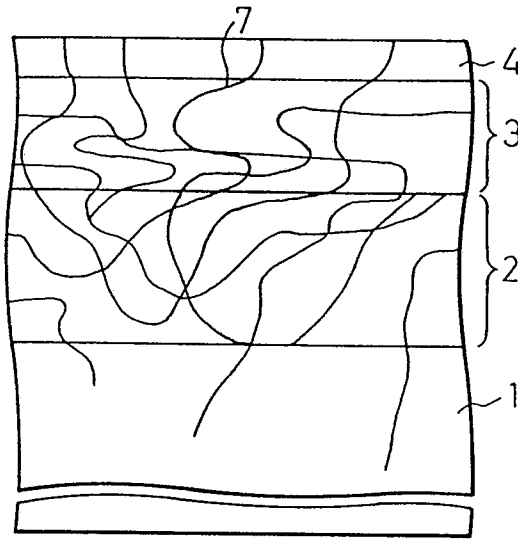


Fig.1B

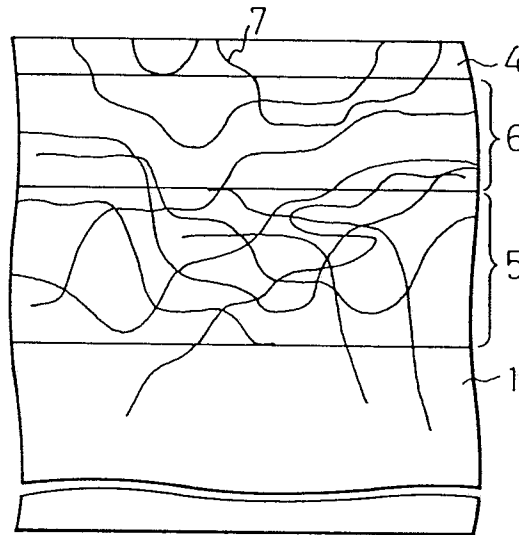


Fig.1C

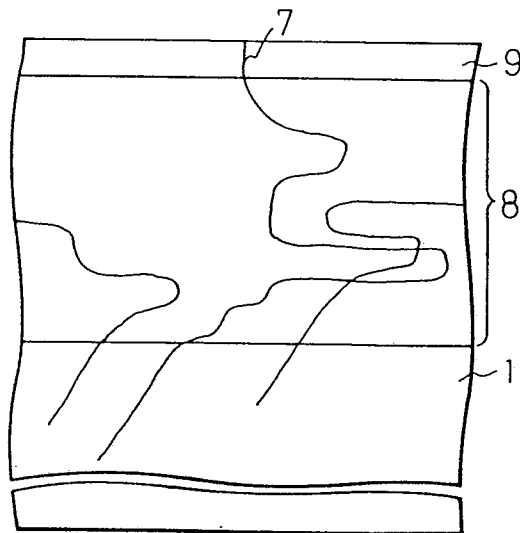


Fig.2A

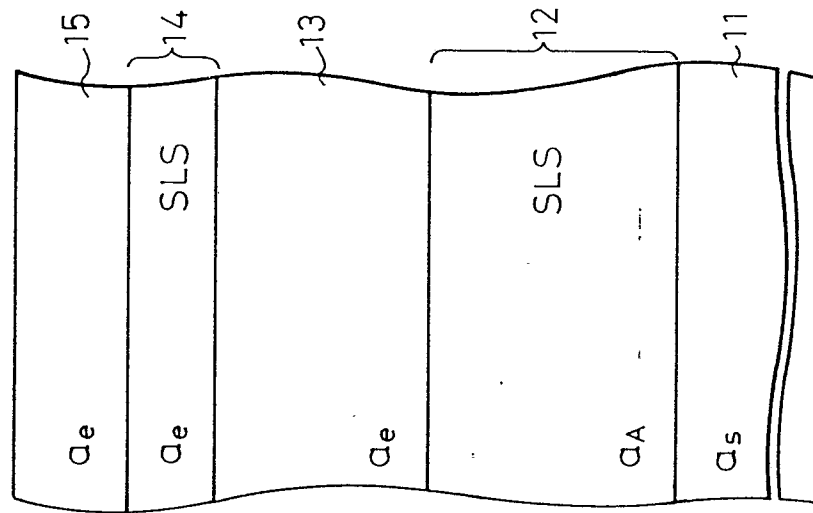


Fig.2B

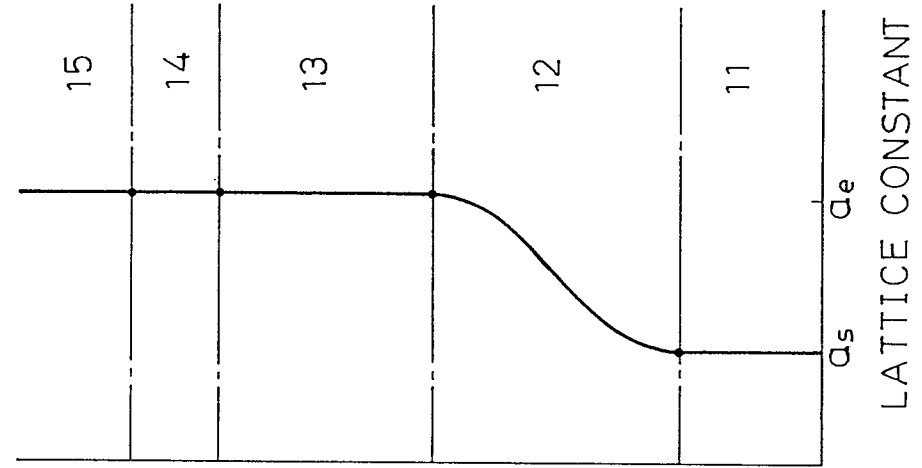


Fig.2C

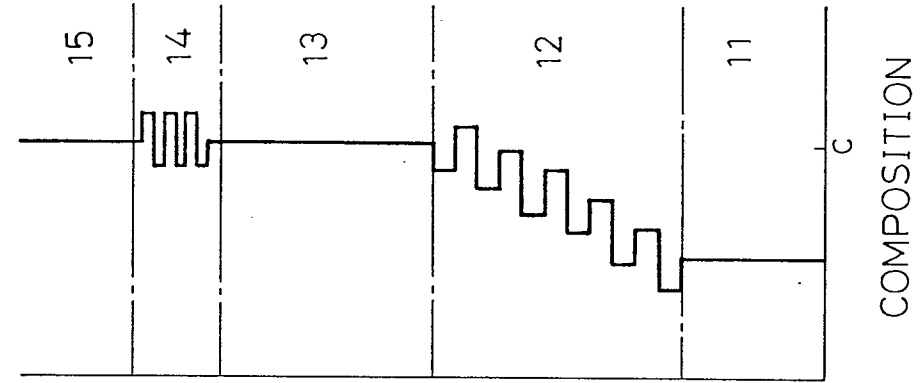


Fig.3A

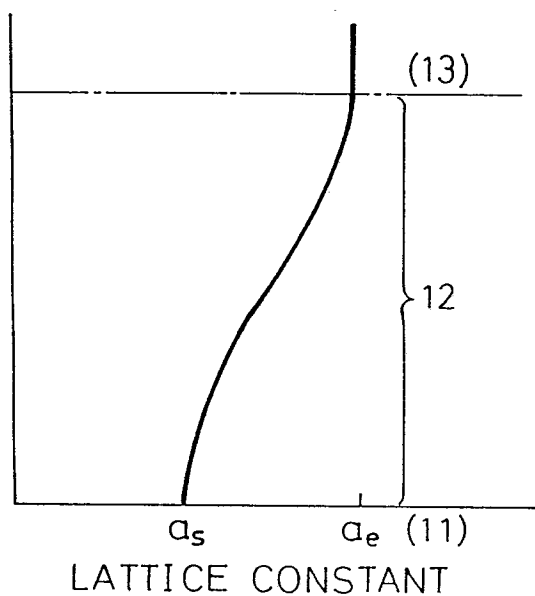


Fig.3B

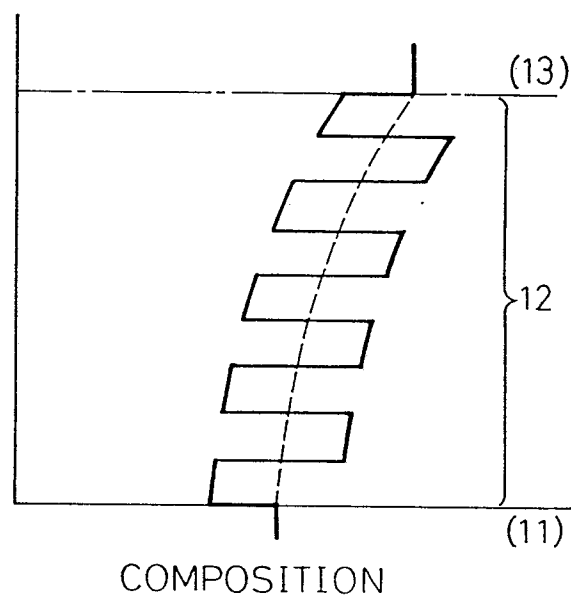


Fig.4A

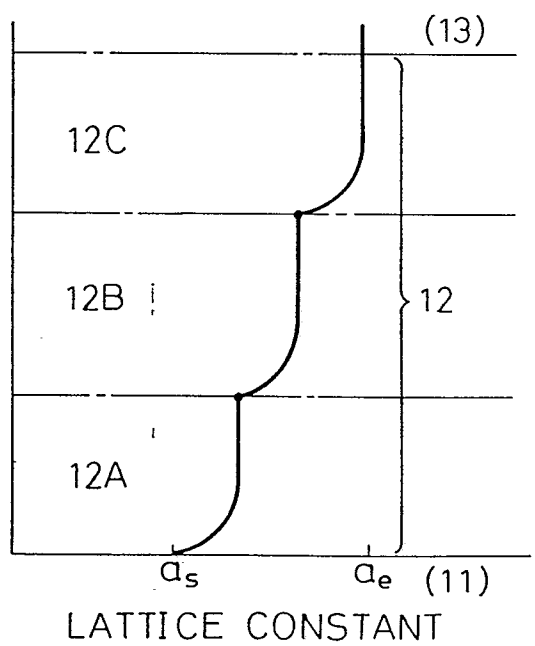


Fig.4B

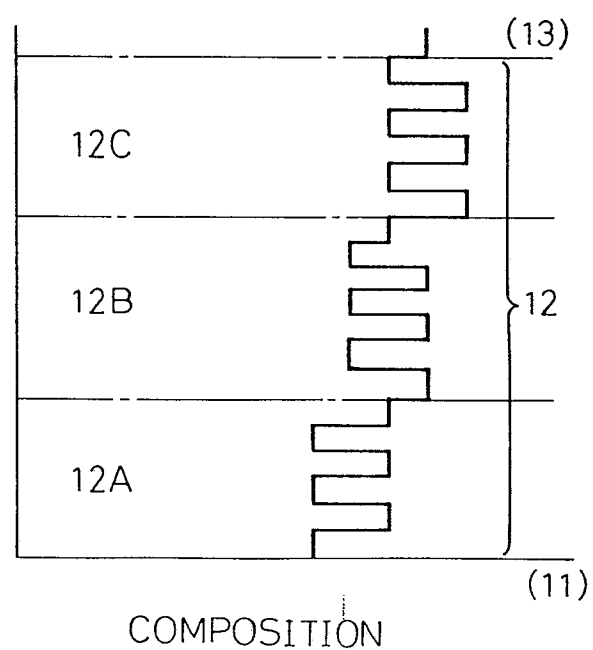


Fig.5

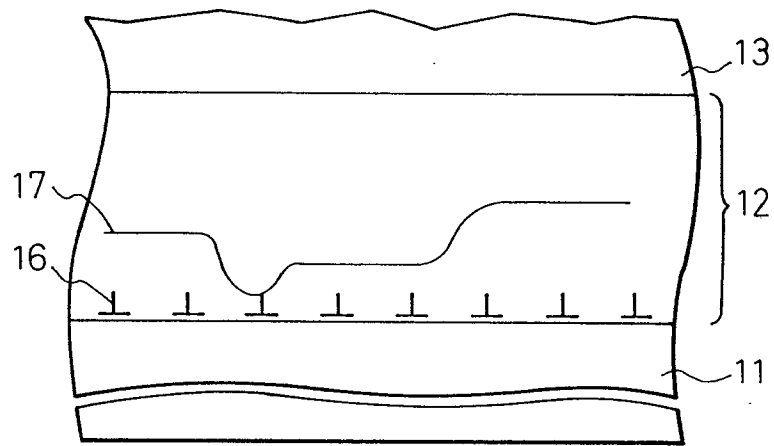


Fig.6A

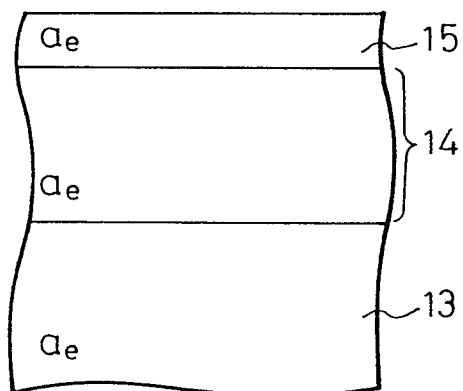
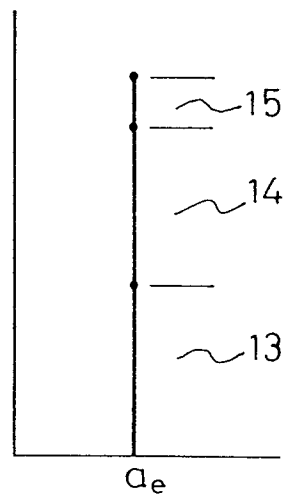
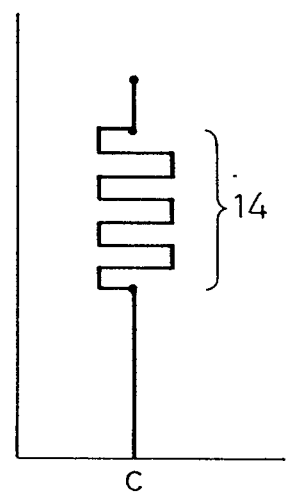


Fig.6B



LATTICE CONSTANT

Fig.6C



COMPOSITION



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	JOURNAL OF VACUUM SCIENCE & TECHNOLOGY/SECTION B, vol. 5, no. 4, July/August 1987, pages 1156-1161, American Vacuum Society, Woodbury, NY, US; J.S. AHEARN et al.: "Control of dislocations in GaAs grown on Si(211) by molecular beam epitaxy" * Abstract; page 1156: "A.MBE growth"; figure 1 *	1,4	H 01 L 21/20 H 01 L 29/205 H 01 L 29/267
A	PATENT ABSTRACTS OF JAPAN, vol. 10, no. 285 (E-441)[2341], 27th September 1986; & JP-A-61 104 611 (MATSUSHITA ELECTRIC IND. CO., LTD) 22-05-1986 * Abstract *	1	
A	SEMICONDUCTOR SCIENCE & TECHNOLOGY, vol. 2, no. 11, November 1987, pages 705-709, IOP Publishing Ltd, Bristol, GB; B. LAMBERT et al.: "High-mobility vertical transport in graded-gap GaAs/AlGaAs superlattices"		TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	EP-A-0 177 903 (DAIDOTO KUSHUKO K.K.)		H 01 L
A	APPLIED PHYSICS LETTERS, vol. 51, no. 18, 2nd November 1987, pages 1428-1430, American Institute of Physics, New York, NY, US; S. SEN et al.: "Observation of resonant tunneling through a compositionally graded parabolic quantum well"		
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 23-05-1989	Examiner GELEBART Y.C.M.
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	