

EUROPEAN PATENT APPLICATION


 Application number: 88104241.0


 Int. Cl. 4: **F02P 3/045**


 Date of filing: 17.03.88


 Date of publication of application:
 20.09.89 Bulletin 89/38


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DE FR IT SE


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Control circuit for a transistorised ignition system.


 A circuit for controlling dwell angle in a transistorised ignition system having an induction-type pulse generator comprises a comparator (K1) arranged to compare the voltage from the induction-type pulse generator (30) with a reference voltage. The comparator switches between two states to provide output pulses for controlling the dwell angle. The circuit includes a capacitor C1 which charges and discharges to vary the reference voltage. The output from the comparator is used to control the reference voltage input to the comparator such that when the comparator is in one state the reference voltage is held at a fixed level and when the comparator is in its other state the reference voltage is varied as a result of the charging or discharging of the capacitor.

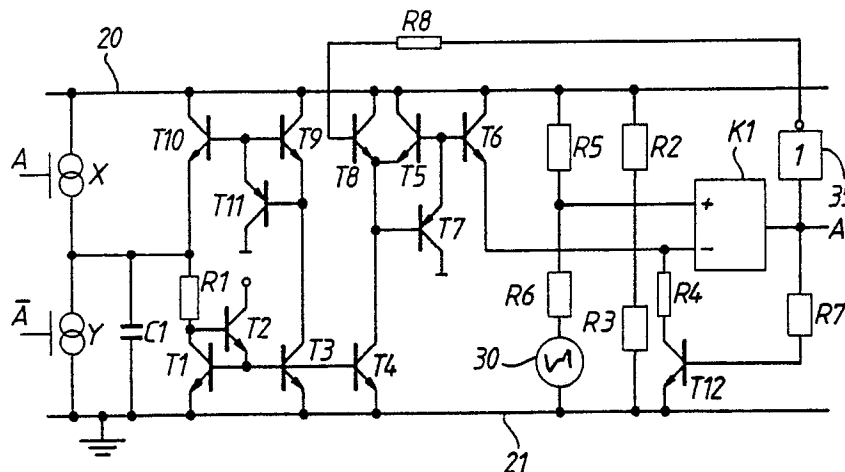


Fig.1.

Control Circuit for a Transistorised Ignition System

The present invention relates to a control circuit for a transistorised ignition system of the type including an induction-type pulse generator.

In an ignition system of this type, a control signal derived from the output voltage of the induction-type pulse generator is used to control the voltage applied to the primary winding of the ignition coil. The time during which current flows through the primary winding is known as the dwell period and is proportional to the angle of rotation of the distributor cam on the distributor shaft from the time contact is made to the time contact is broken. This angle is known as the dwell angle and can be controlled by the control signal.

For satisfactory operation the primary current must have reached a given level at the ignition point. On the other hand it is desirable to minimise the dwell period in order to shorten the time the current control circuit for the winding must operate within its control range and minimise power dissipation.

Since the frequency of rotation of the distributor cam increases with increasing engine speed, at high engine speeds it is necessary to increase the dwell angle with increasing speed to ensure that the primary current reaches a sufficiently high level. However, under certain engine operating conditions it is possible to reduce the dwell angle with increasing engine speed in order to reduce power dissipation, and still obtain sufficient ignition energy. For example, dwell angle reduction is advantageous at relatively low engine speeds after start up when the spark is being advanced.

The present invention is particularly concerned with a control circuit which operates to reduce the dwell angle at low speeds in order to reduce power loss at low speeds, e.g. idling. US-A-4,176,645 discloses a motor ignition system control circuit for maintaining energy storage in the spark coil constant over a wide speed range. In this circuit an integrator, in the form of a capacitor, shifts the control thresholds of a threshold switch which controls the interrupter for the spark coil. The threshold switch is a comparator. The capacitor charges and discharges in response to signals from a monitoring resistor in series with the spark coil primary winding and the interrupter switch. While the interrupter switch is open the capacitor output voltage remains constant. While current flows through the interrupter circuit the integrator increases the control threshold until the primary winding reaches a predetermined level and then decreases the control voltage until the interrupter switch re-opens. The rate of charging and discharging of the capacitor and hence the operation of the threshold switch

depend on engine operating conditions.

This is a complex circuit which is arranged to reduce dwell angle with increasing speed during initial acceleration after start up and increase dwell angle with increasing speed at high engine speeds.

The present invention provides a circuit for controlling the dwell angle in a transistorised ignition system having an induction-type pulse generator, the circuit including a comparator arranged to compare the voltage from the induction-type pulse generator with a reference voltage and to switch between two states to provide output pulses for controlling the dwell angle, and a capacitor arranged to vary the reference voltage such that the length of the output pulses varies in dependence on the pulse generator frequency, characterised in that a reference bias voltage is provided and in that the output from the comparator is used to control the reference voltage input to the comparator such that when the comparator is in one state the reference voltage is held at a fixed level and when the comparator is in its other state the reference voltage is a combination of the reference bias voltage and a voltage derived from the charging or discharging of the capacitor whereby to limit the period the comparator is in said other state.

Since the reference voltage of the comparator is fixed for one of the comparator output states, one of the switching levels (either ON or OFF) of the comparator remains constant and only the other switching level is varied. The following edge of the pulse, in the preferred embodiment, is used for ignition timing and so the relative timing of the OFF state of the comparator remains constant with the switching ON of the comparator being varied.

In the circuit of US-A-4,176,645, while the threshold switch is on the interrupter switch is closed and the capacitor charges and discharges until the threshold switch is turned off. The capacitor output voltage is then held while the interrupter switch is open. The next switch on threshold depends on the output voltage held at the capacitor during the previous opening of the interrupter switch.

In contrast, in the present invention the varying output of the capacitor is added to a bias voltage and applied to one input of the comparator as the voltage from the induction type pulse generator is applied to the other. The capacitor will charge or discharge at a set rate depending on the circuit characteristics. The state of the comparator will change when the two voltages cross. Thus, the charge will depend on the rate of change of the pulse generator voltage, which will in turn depend on its frequency. Thus, in the preferred embodi-

ment of the present invention the variable switching level of the comparator (as opposed to the fixed level) actually varies as the pulse generator voltage is applied to the integrator and thus the level at which the integrator actually switches depends on the pulse generator frequency. However, due to the bias reference voltage at low speeds where the capacitor is fully discharged, the comparator is prevented from switching until the voltage from the pulse generator exceeds the bias voltage.

Preferably the comparator is used to control switch means arranged to prevent the voltage of the comparator from being input to the comparator when the comparator is in said one state. The comparator output is preferably arranged to control switch means such as a transistor, arranged to clamp the reference voltage to a fixed level when the comparator is in said one state.

The output pulses from the comparator are preferably used to control the charging and discharging of the capacitor such that when the comparator is in one state the capacitor discharges and when the comparator is in the other state the capacitor charges.

In contrast to the arrangement shown in US-4,176,645, the capacitor charge and discharge states correspond to the on/off states of the comparator. In one of these states the capacitor output is not actually supplied to the comparator input.

An embodiment of the invention will now be described by way of example only and with reference to the accompanying drawings in which:

Fig. 1 is a circuit diagram of a first embodiment of the invention, and Figure 2 shows the waveforms of voltages at different places in the circuit of Fig. 1 on parallel time axes.

The control circuit illustrated in Fig. 1 includes two constant current supplies X and Y connected in series between a first voltage lead 20 and a second voltage lead 21 which is grounded. A capacitor C1 is connected between the junction of current sources X and Y and the ground supply rail. The current sources provide currents to charge and discharge capacitor C1 via a resistor R1.

The circuit includes three current mirrors, the first comprising transistors T1, T2 and T3, the second comprising transistors T5, T6 and T7 and the third comprising transistors T9, T10 and T11. In each current mirror configuration two of the transistors are coupled base to base with the third transistor having its emitter connected to the base-to-base junction of the other two transistors. Each current mirror circuit provides an output current which substantially reproduces the circuit's input current. Thus, for example, the output collector current from T6 is substantially equal to the input collector current to T5.

Resistor R1 is connected to the input of the

first current mirror circuit consisting of transistors T1, T2, T3. The third current mirror circuit T9, T10, T11 is connected to the first such that the emitter of T10 is connected to the collector of T1 and the base of T2 via R1 and the emitter of T9 is connected to the collector of T3. The base of T3 is connected to the base of a further transistor T4 such that T3 conducts when the first current mirror operates.

The output of an induction type pulse generator 30 is connected to the non-inverting input of a comparator K1 via a resistor R6. A resistor RS is connected between the supply rail and the non-inverting input of comparator K1. The values of R5 and R6 are selected to provide the appropriate level of signal on the non-inverting input of the comparator K1.

The emitter of transistor T6, i.e. the output of the second mirror circuit, is connected to the junction of two resistors R2 and R3 which are connected in series across the supply rails 20 and 21. The junction of the resistors is also connected to the inverting input of comparator K1. A further resistor R4 has one terminal connected to the inverting input of comparator K1 and its other terminal connected to rail 21 via a transistor T12. T12 is switched on by the output of comparator K1 via a resistor R7.

The output of comparator K1 is supplied via an inverter 35 and a resistor R8 to the base of a transistor T8 which is connected collector-to-collector and emitter-to-emitter to the transistor T5 of the second current mirror. When transistor T8 is switched on a base current is supplied to transistor T7 to render the second current mirror operational.

As shown in Fig. 1, the constant current sources X and Y are controlled by the output of comparator K1 and the inverted output of K1 respectively.

The operation of the circuit is as follows:

On the occurrence of an output representing logic level zero from the comparator K1, the following edge of the square wave pulses in Fig. 2(d), the inverted output signal supplied to transistor T8 via resistor R8 causes T8 to be switched on and thus current mirror T5, T6, T7 is operative. The capacitor C1 starts to discharge under the control of current source Y and a current flows through resistor R1. With transistor T8 switched on, this current is reflected to the junction of resistors R2 and R3 via the current mirrors T1, T2, T3 and T5, T6, T7. Resistors R2 and R3 form a potential divider which applies a constant minimum voltage level to the inverting input of the comparator. The voltage derived from discharging capacitor C1 is added to the voltage level at the junction of R2, R3 when transistor T8 is switched on. As can be seen from a comparison of Figs. 2(c) and 2(d) when the output

from the comparator K1 represents logic level zero the input voltage to the inverting terminal of K1 simply reflects the voltage at C1.

It should be noted here that the horizontal line shown in Figure 2c does not represent zero voltage, but rather a reference voltage. In the embodiment of the invention shown here this reference voltage will be a positive potential.

Current is reflected back to capacitor C1 by the third current mirror T9, T10, T11 to compensate for losses originating through resistor R1.

As soon as the output from comparator K1 changes state, which occurs when the voltages of its inputs are equal, hysteresis is introduced due to the operation of transistor T12. A voltage across R7 causes transistor T12 to conduct, thus providing a short circuit from the junction of resistors R2 and R3 to ground. Thus, with the output from K1 in this state the voltage at its non-inverting input is held at a fixed level below the operating level of the comparator. Since the inverted output of comparator K1 is also supplied to transistor T8, transistor T8 is switched off when transistor T12 is switched on and thus current mirror T5, T6, T7 is blocked and the voltage at C1 is not reflected at the junction of resistors R2, R3. As shown in Fig. 2(c), this ensures a sharp change at the voltage of the inverting input of comparator K1 when the output of K1 changes state and also causes the capacitor C1 to charge from current source X as indicated in Fig. 2(b).

The induction type pulse generator supplies an alternating voltage at the non-inverting input of comparator K1 whose frequency increases with increasing speed of the engine. As the wavelength of the alternating voltage decreases the point along the voltage curve at which comparator K1 changes state will be shifted because capacitor C1 will have had less time to charge or discharge. This is clear from Fig. 2 which shows two voltage waveforms of different frequency. The point along the voltage curve at which the output of comparator K1 changes from logic "0" to logic "1" occurs at a higher point on the voltage curve for the second waveform. When the output of comparator K1 is at logic "1" the voltage at the inverting input stays constant and thus the point on the voltage curve at which the comparator output returns to logic "0" is independent of the alternating voltage frequency.

At low engine speeds, however, power dissipation would be high due to the long dwell angle and long pulse duration. The circuit described above reduces the dwell period at low engine speeds due to the presence of the potential divider R2, R3 which ensures that there is always a bias voltage available at the inverting input of the comparator K1 even when the capacitor C1 has fully discharged. This is clearly shown in Fig. 2(c) at the

area of the waveform diagram circled and marked A. The effect of the bias voltage is to maintain the comparator circuit in the OFF condition for longer than it would otherwise be. In other words, the position of the rising edge of the pulses in Fig. 2(d) is controlled to ensure that there is a maximum dwell period limit introduced during normal running of the engine.

Once the engine speeds up to an extent so that the effect of the maximum dwell period limit is overcome, control of the dwell period and hence dwell angle is carried out by other circuitry which may be conventional.

The present invention is concerned only with the control of dwell angle and dwell period at low engine speeds in order to reduce power dissipation. The circuitry described above thus is only part of a larger ignition control circuit.

Claims

1. A circuit for controlling the dwell angle in a transistorised ignition system having an induction-type pulse generator (30), the circuit including a comparator (K1) arranged to compare the voltage from the induction-type pulse generator (30) with a reference voltage and to switch between two states to provide output pulses for controlling the dwell angle, and a capacitor (C1) arranged to vary the reference voltage such that the length of the output pulses varies as a function of the pulse generator frequency, characterised in that a reference bias voltage is provided and in that the output from the comparator (C1) is used to control the reference voltage input to the comparator such that when the comparator is in one state the reference voltage is held at a fixed level and when the comparator is in its other state the reference voltage is a combination of the reference bias voltage and a voltage derived from the charging or discharging of the capacitor whereby to limit the period during which the comparator is in said other state.

2. A circuit as claimed in claim 1 in which, during said other state of the comparator the varying output voltage of the capacitor is applied to one input of the comparator as the voltage from the induction-type pulse generator is applied to the other.

3. A circuit as claimed in claim 1 or 2 in which the comparator output is used to control switch means (T8) arranged to prevent the voltage of the capacitor from being supplied to the comparator when the comparator is in said one state.

4. A circuit as claimed in claim 1, 2 or 3 in which the comparator output is arranged to control switch means (T12) arranged to remove the bias

voltage and clamp the reference voltage to the fixed level when the comparator is in said one state.

5. A circuit as claimed in any preceding claim in which the output pulses from the comparator are used to control the charging and discharging of the capacitor such that when the comparator is in one state the capacitor discharges and when the comparator is in the other state the capacitor charges.

6. A circuit as claimed in claim 5, in which the capacitor is connected to two constant current sources (X, Y), one of which is connected by the output pulses of the comparator and the other of which is controlled by inverted output pulses from the comparator.

7. A circuit as claimed in any preceding claim in which at least one current mirror circuit is provided for conveying the capacitor voltage to the comparator input.

8. A circuit as claimed in claim 7 in which at least one current mirror circuit provided for conveying the capacitor voltage to the comparator circuit is arranged to be blocked when the comparator is in said one state.

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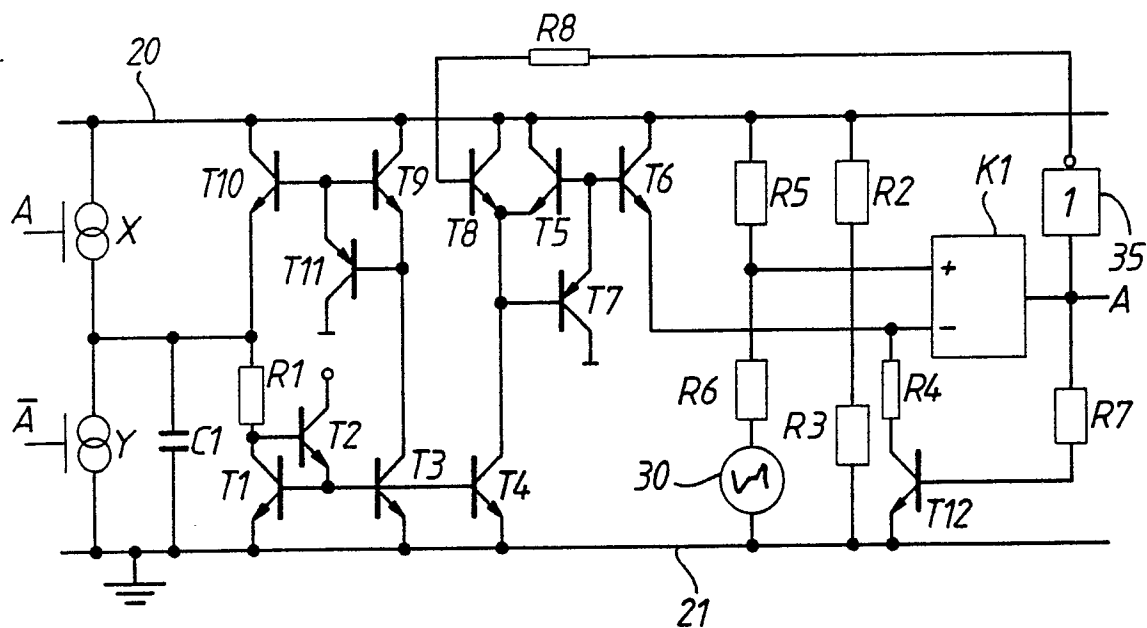


Fig. 1.

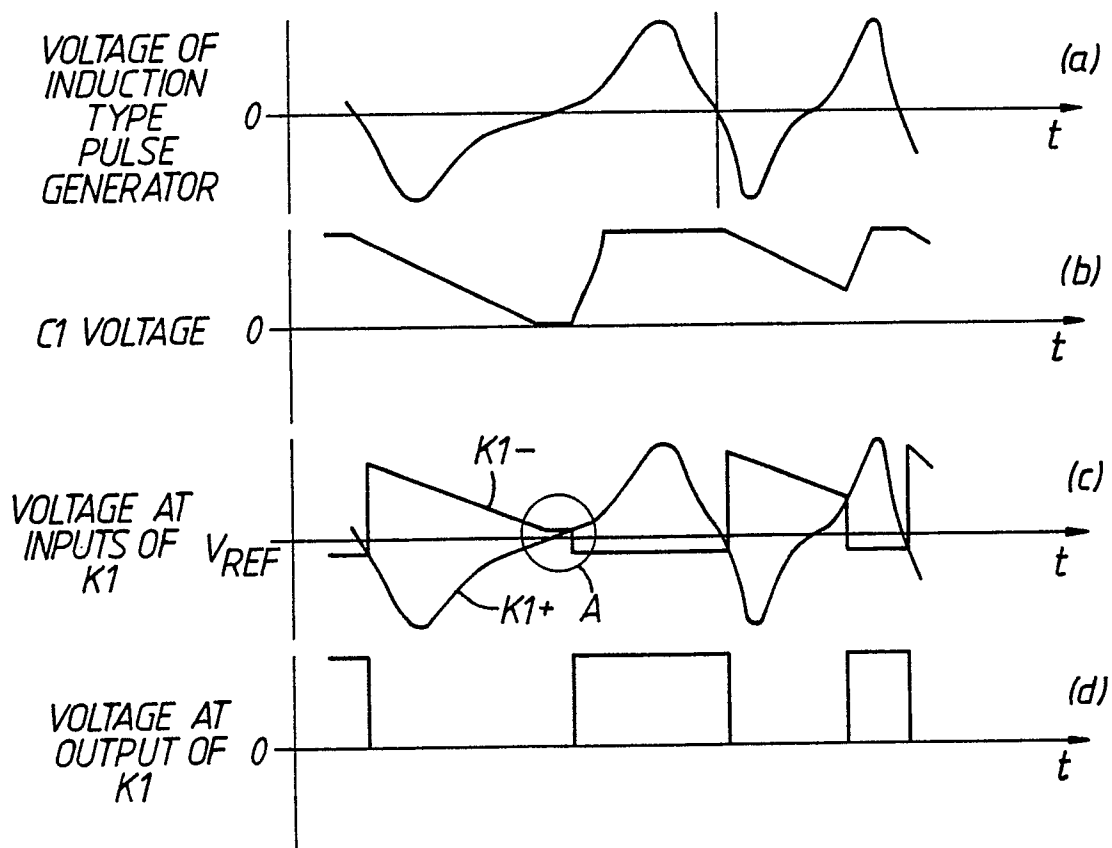


Fig. 2.



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
A	US-A-4 429 235 (W. MINNER) * Front page; figures 2e - 2g; column 6, lines 1-62 *	1-3,5	F 02 P 3/045
A	US-A-4 552 118 (H. FUKAYA) * Figure 1; column 3, lines 33-44 *	1,2	
A	EP-A-0 191 418 (NIPPONDENSO CO., LTD)		
A	US-A-3 838 672 (R.C. RICHARDS et al.)		
A	US-A-4 440 130 (Y. TAGUCHI et al.)		
A	US-A-4 434 779 (N. YAMAMOTO et al.)		
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. Cl.4)
			F 02 P
Place of search		Date of completion of the search	Examiner
THE HAGUE		08-11-1988	LEROY C.P.
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