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(54) **FLAT LIQUID CRYSTAL DISPLAY UNIT AND METHOD OF DRIVING THE SAME.**

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(56) References cited :
EP-A- 0 197 551
EP-A- 0 260 747
DE-A- 3 630 012
GB-A- 2 081 018
JP-A- 49 398

(56) References cited :
JP-A- 87 250
JP-A- 100 467
JP-A- 100 467
JP-A- 162 794

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Description

The present invention relates to flat liquid crystal display devices having a plurality of display pixels at intersecting points of scanning and signal electrodes arranged in the form of a matrix, and methods of driving such devices.

In a prior art flat display device, as shown in Japanese Patent Laid-Open JP-A-53 038 935 and Japanese Patent Laid-Open JP-A-58 052 686, a driving circuit is connected to one end of transparent electrodes to drive a display panel.

However, as a larger capacity of dot matrix type liquid crystal panel is required, the width of the transparent electrodes gets less and the length of the transparent electrodes gets greater, so that the electrode resistance R and the capacitance C from the output terminal of the driving circuit to the far end of the electrodes increases, which results in a decrease in quality of the picture. When a liquid crystal panel has 640 x 400 dots and is driven at 1/200 duty cycle, R = 10 to 60 KΩ, and C = 800 to 2000 pF, the delay time of the respective picture elements from the change of the driving waveform until the stabilisation of the waveform is several or several tens of μs. This delay time cannot be neglected relative to a scanning time of 60 to 80 μs. Due to the delay time, the effective driving voltage applied to respective picture elements is displaced from the predetermined value obtained by the voltage standard method. As a result, unevenness of colour contrast is generated as shown in Figure 2. The quality of the picture is reduced so much that it may be difficult to distinguish the non-selected and selected regions. Figure 2 illustrates the results of the use of an embodiment of the prior art, wherein unevenness of colour contrast is generated between non-selected regions 11 and 12, when alternate horizontal lines are ON. There are two upper areas above the portions 11 and 12, respectively. In the lefthand area above portion 11, each alternate horizontal line is ON when selected and in the righthand area above portion 12, alternate horiztonal lines are ON when selected but not aligned with those in the the lefthand area. Thus odd-numbered lines in the lefthand area are lit up, whilst even numbered lines in the righthand area are lit up. If the lengths of the lines in the lefthand area are the same as the lengths of the lines in the righthand area, there is no unevenness of colour or brightness. If, however, as shown, the lines in the righthand area are noticeably shorter than the lines in the lefthand area, the lefthand area becomes lighter than the righthand area which becomes darker in contrast. This effect is greater as the resistance of the scanning electrodes increases. If, however, the thickness of the transparent electrodes is increased in order to reduce the resistance thereof, a problem arises called "inferior alignment". On the surface of the liquid crystal material in contact with the transparent electrode, the liquid crystal molecules are aligned in a specific direction, but at the edge of the electrode there is a discontinuity which, if the electrode is thick, produces a difference of surface level which prevents some of the surface molecules from being aligned in the specific direction. Thus, there is a defective orientation which is not generated when the electrode is thin. The cost of manufacturing the panel is also increased. The treatment time depends upon the thickness of the deposited electrode and etching time is similarly dependent. Both problems arise from increased thickness of electrodes.

It has been proposed, therefore, in JP-A-57-100467 and GB-A-2081018 to drive the electrodes of the liquid crystal panel from both ends thereof, thereby to provide a liquid crystal display device having a high quality of pictures and having a little unevenness of colour contrast.

However, with such an arrangement, there is a problem when power is applied to the device at power-on. The driving circuits connected to opposite ends of the electrodes are not immediately stable and the output voltages may differ. These outputs are connected to each other through a transparent electrode and as the liquid crystal driving voltage is 20 to 40 volts in this case, a current of several hundred microamperes to several milliamperes is applied per output. Such a current has a bad effect upon the driving circuits and the liquid crystal panel.

According to the present invention, therefore, a flat liquid crystal display device having a plurality of display pixels at intersecting points of scanning and signal electrodes arranged in the form of a matrix, including equally controlled first and second driving circuits, the first driving circuits being connected to drive the scanning electrodes from one end and the second driving circuits being connected to drive the scanning electrodes from the other end, and is characterised by means responsive to a power-on signal for a predetermined period from power-on, to control the first and second driving circuits to give equal outputs.

Preferably, the device includes equally controlled third and fourth driving circuits, the third driving circuits being connected to drive the signal electrodes from one end and the fourth driving circuits being connected to drive the signal electrodes from the other end, and is characterised by means responsive to a power-on signal for a predetermined period from power-on, to control the third and fourth driving circuits to give equal outputs.

The present invention extends to a method of controlling the first and second driving circuits by a power-on signal for a predetermined period from power-on to give equal outputs. The present invention further extends to a method of controlling the third and fourth driving circuits by a power-on signal for a predetermined period from power-on to give equal outputs.

The scope of the present invention is defined by the appended claims; and how it can be carried into effect is hereinafter particularly described with reference to the accompanying drawings in which:-

Figure 1 is a block diagram of an embodiment of a flat liquid crystal display device according to the present invention;

Figure 2 is a diagrammatic front view of a prior art LCD, explanatory of uneven colour contrast;

Figure 3 is an equivalent circuit diagram of a liquid crystal display device to which the present invention is applicable; and

Figure 4 is a diagram of a driving circuit forming part of a device according to the present invention.

In the embodiment of the invention shown in Figure 1, the picture elements or pixels are formed at the crossing or intersecting points of scanning and signal electrodes arranged in the form of a matrix. The liquid crystal display device has transparent electrodes (such at ITO) which are driven by pairs of scanning and signal driving circuits, the amplitudes of the voltages applied to opposite ends of the electrodes being equal. The signal driving circuits are started by a shift signal XSCL input to a shift register 2, the display data XD is switched from parallel to series, is synchronised with a signal LP by a latch 3, and is converted through a level shifter 4 to a liquid crystal driving waveform including the four voltage levels of the voltage standard method by a driver 5.

In the scanning driving circuits, the shift register 6 receives a start pulse YD and is operated by a shift clock, and the output of the shift register 6 is converted through a level shifter 7 to a liquid crystal driving waveform including the four voltage level by a driver 8.

When the power is applied to the liquid crystal display device, the circuits operate under unstable conditions, and the output voltages of the two driving circuits which are connected to each other through a transparent electrode are different from each other. Since the liquid crystal driving voltage is 20 - 40 V in this case, a current of several hundred μA -several mA is applied per one output, so that the current gives bad effect to the driving circuit and the liquid crystal panel. Thereupon, the driver of the driving circuit used in the liquid crystal display device of the present invention is provided with a circuit for controlling the output for a predetermined time by a prohibit signal INH at the time of power-on until the condition of the driving circuit is stabilised, in order to prevent the driver output from being shorted at the time of power-on.

Fig. 3 is an equivalent circuit according to a dot matrix liquid crystal display device of the present invention. In Fig. 3, a 5 x 3 matrix panel is driven from both terminals of the scanning electrodes. In Fig. 3, the picture elements Ⓐ and Ⓑ are elements most far from the terminals of the present invention and some of the prior art, respectively. Ⓑ in the prior art, is single-sided driven from left side. The following is the resistance values between the driving circuit and the portions A and B:

$$Ⓐ : (3rC + RC) \times 1/2\ \Omega$$

$$Ⓑ : 5rC + RC\ \Omega$$

Herein, r_C and r_S are electric resistances between picture elements, and R_C and R_S are output resistances of the driving circuits. R_C is more or less than 1 kΩ and when the picture elements are increased and the number of elements rC becomes several hundreds or more, the value of R_C can be neglected substantially. Therefore, the more the number of picture elements is increased, the more the resistance ratio Ⓐ : Ⓑ approaches 1 : 4 . On the other hand, since the capacitor C coupled to the electrodes is not changed, this means that the picture quality obtained according to the driving method of the present invention is the same as that of the prior driving method wherein the resistance of the transparent electrodes is one quarter. Otherwise, if the picture quality of the present invention is the same as that of the prior art, this means that a liquid crystal cell having twice size can be realized and the high resolution of the liquid crystal display device can be realized.

Fig. 4 shows one embodiment of the scanning driving circuit. In Fig. 4, the circuits which are surrounded by a dotted line 42 show the driving circuits for one bit and are used for driving one terminal of an electrode. That is, the output of the driving circuit 42 is to one terminal of a scanning electrode, as in figure 3. The portion surrounded by the dotted line 43 shows circuits of high voltage portions relative to logic portions. In Fig. 4, the shift register which is operated by a shift clock SCK comprises a D type flip flop 21. A signal LP shown in Fig. 1 is input as the shift clock signal SCK to CK of the flip-flop 21. A start pulse YD is input as signal Qn-1 to Dn of the flip flop 21 which is the first stage of the shift register. The output Qn of the flip-flop 21 is a signal Dn+1 input to the flip flop 21 of the second stage by the shift clock signal SCK. The output Qn of the flip flop 21 is transmitted to the input $\bar{I}$ of a level shifter 23a through NOR gate 24 and through NOR gate 24 and inverter 25 to the input I of the shifter 23a. The NOR gate 24 acts to forcibly change the driver output OUT to an equal electric level with respect to the other terminal of the electrode upon the signal INH. The output O of the level shifter 23a is connected to the gate electrode of transfer gate 26 of co-compensative transistors and to one input of a NOR gate 32. The output $\bar{O}$ of the shifter 23a is connected to the gate electrode of transfer gate 27 and to one input of NAND gate 31. The NOR gate 32 and NAND gate 31 act to change the non-selected potential to A.C. The frame signal FR and the signal INH are combined in NOR gate 36 whose output is fed to input $\bar{I}$ of level shifter 23b, and through inverter 37 to input I. Output O of shifter 23b is connected through inver-

ter 38 to the other input terminals of the gates 31 and 32. The outputs of the gates 31 and 32 are connected to the gates of the transfer gate 28 of a P channel transistor and the transfer gate 29 of a N channel transistor, respectively, to control the output of the non-selected levels V_1 and V_4.

On the other hand, the selected potentials (V_0, V_5) are multiplexed by the transfer gate 40 of a P channel transistor and the transfer gate 41 of a N channel transistor in each of which a FR signal given from the output O of the level shifter 23b acts as a gate input, and then are supplied to the source electrodes of the co-compensative transfer gates 26 and 27. In the transfer gates 26, 27, 28 and 29, the outputs O, $\overline{O}$ of the level shifter 23a work as gate inputs. When the signal INH is "high", the gate 26 is conductive and thus the driver output OUT is kept at level V_5. Therefore, when in Fig. 1 the display device and, in particular, the driving circuit is ON, if the INH signal is "high", the outputs of both drivers 8 have equal levels, so that the outputs of the drivers are shortened to each other through the transparent electrodes, thereby making it possible to prevent the flow of large current flowing between the drivers. As a matter of course, the level of the equal potential may be not only V_5 but also V_O, V_1, V_4. When none of the voltages V_O, V_1, V_4, V_5, is applied, there is a high impedance. Further, it is possible to use the circuit used in a scanning side driving circuit for the short preventing circuit of the signal side driving circuit.

On the other hand, if the driving method of the present invention has TAB construction wherein a semiconductor IC for driving is bonded to a flexible tape or COG (Chip on Glass) construction, the driving circuits connected to both terminals of the liquid crystal cell are stored easily. In particular, COG construction is superior in that the wires between the driving circuit and electrodes, and connecting resistance become a minimum. Further, even if the driving method of the present invention is only applied to the scanning electrodes, such a construction is effective in preventing the phenomenon shown in Fig. 2. Namely, since the amplitude of the driving voltage of the scanning electodes is about 5 to 10 times larger than that of the signal electrodes, the delay time of the charge/discharge time is likely to have an effect on the picture quality. This method is most available for the colour liquid crystal cell which has narrow electrode pitches.

Further, the electrode resistances of the signal electrodes are reduced by making the transparent electrode films thicker or coupling different metal of low resistance to the transparent electrodes and the electrode resistances of the scanning electrodes are reduced equivalently. The picture quality can be improved by such reductions economically.

A simple matrix type LCD in the liquid crystal display devices is explained above. The deterioration of the picture quality which may be generated in dependance with the resistances of the picture electrodes can be improved by the method of the present invention. Therefore, the method of the present invention is widely applicable for active type LCD having TFT (thin film of transistor) or MIM (metal-insulator-metal), or for flat display till PDP (plasma display panel) wherein high current flows, or ELD (electro luminescence display).

As mentioned above, according to the present invention, the transparent electrode resistance values are reduced to one quarter equivalently, therefore it has the following advantages:

(a) Since in a passive type liquid crystal cell, the voltage applied to the liquid crystal approaches a predetermined value which is obtained by the voltage standard method, even if the display device has a medium or small capacitance and is driven by the 2-frame A.C. driving method, it is possible to obtain a high contrast display.

(b) A large scale panel display having fine pitch electrodes can be obtained without deterioration of the picture quality.

(c) Since it is not necessary to reduce the output resistance of the driving circuit excessively, it is possible to obtain an IC having more pins and a lower cost than those of the prior art.

(d) Since the thickness of the transparent electrode (ITO) is thinner, it is possible to obtain panels which are low in cost.

Claims

1. A flat liquid crystal display device having a plurality of display pixels at intersecting points of scanning electrodes and signal electrodes arranged in the form of a matrix (1), including equally controlled first and second driving circuits (8), the first driving circuits being connected to drive the scanning electrodes from one end and the second driving circuits being connected to drive the scanning electrodes from the other end, characterised by means responsive to a power-on signal (INH) for a predetermined period from power-on, to control the first and second driving circuits to give equal outputs.

2. A device as claimed in claim 1, including equally controlled third and fourth driving circuits (5), the third driving circuits being connected to drive the signal electrodes from one end and the fourth driving circuits being connected to drive the signal electrodes from the other end, characterised by means responsive to a power-on signal (INH) for a predetermined period from power-on, to control the third and fourth driving circuits to give equal outputs.

3. A device as claimed in claim 1 or 2, wherein each first driving circuit includes an output terminal (OUT) connected to the one end of a scanning electrode and a transistor which outputs a predetermined level voltage to the output terminal in response to the power-on signal, and each second driving circuit includes an output terminal connected to the other end of a scanning electrode and a transistor which outputs the predetermined voltage level to the output terminal in response to the power-on signal.

4. A device as claimed in claim 3, as appendant to claim 2, wherein each third driving circuit includes an output terminal connected to the one end of a signal electrode and a transistor which outputs a predetermined voltage level to the output terminal in response to the power-on signal, and each fourth driving circuit includes an output terminal connected to the other end of a signal electrode and a transistor which outputs the predetermined voltage level to the output terminal in response to the power-on signal.

5. A method of operating a flat liquid crystal display device having a plurality of display pixels at intersecting points of scanning and signal electrodes arranged in the form of a matrix, using equally controlled first and second driving circuits (8) connected to drive opposite ends of the scanning electrodes, characterised by providing a power-on signal (INH) for a predetermined period from power-on to control the first and second driving circuits to give equal outputs.

6. A method as claimed in claim 5, wherein the device includes equally controlled third and fourth driving circuits (5) connected to drive opposite ends of the signal electrodes, characterised by providing a power-on-signal (INH) for a predetermined period from power-on to control the third and fourth driving circuits to give equal outputs.

Patentansprüche

1. Flache Flüssigkristallanzeigevorrichtung mit einer Vielzahl von Anzeigepixeln an Schnittpunkten von Abtastelektroden und Signalelektroden, die in Form einer Matrix (1) angeordnet sind, mit gleichermaßen gesteuerten ersten und zweiten Treiberschaltungen (8), wobei die ersten Treiberschaltungen zum Treiben der Abtastelektroden vom einen Ende und die zweiten Treiberschaltungen zum Treiben der Abtastelektroden vom anderen Ende angeschlossen sind, **gekennzeichnet durch** eine Einrichtung, die auf ein Energie-Ein-Signal (INH) für eine vorbestimmte Zeitdauer vom Energieeinschalten ab anspricht, um die ersten und die zweiten Treiberschaltungen zur Abgabe gleicher Ausgangssignale zu steuern.

2. Vorrichtung nach Anspruch 1, mit gleichermaßen gesteuerten dritten und vierten Treiberschaltungen (5), wobei die dritten Treiberschaltungen zum Treiben der Signalelektroden vom einen Ende und die vierten Treiberschaltungen zum Treiben der Signalelektroden vom anderen Ende angeschlossen sind, **gekennzeichnet durch** eine Einrichtung, die durch ein Energie-Ein-Signal (INH) für eine vorbestimmte Zeitdauer vom Energieeinschalten ab anspricht, um die dritten und vierten Treiberschaltungen zur Abgabe gleicher Ausgangssignale zu steuern.

3. Vorrichtung nach Anspruch 1 oder 2, wobei jede erste Treiberschaltung einen Ausgangsanschluß (OUT) aufweist, der mit dem einen Ende einer Abtastelektrode verbunden ist und mit einen Transistor, der auf das Energie-Ein-Signal hin eine Spannung mit vorbestimmtem Spannungswert an den Ausgangsanschluß gibt, und wobei jede zweite Treiberschaltung einen mit dem anderen Ende einer Abtastelektrode verbundenen Ausgangsanschluß aufweist und einen Transistor, der auf das Energie-Ein-Signal hin den vorbestimmten Spannungswert an den Ausgangsanschluß gibt.

4. Vorrichtung nach Anspruch 3 in Verbindung mit Anspruch 2, wobei jede dritte Treiberschaltung einen mit dem einen Ende einer Signalelektrode verbundenen Ausgangsanschluß aufweist und einen Transistor, der auf das Energie-Ein-Signal hin einen vorbestimmten Spannungswert an den Ausgangsanschluß gibt, und wobei jede vierte Treiberschaltung einen mit dem anderen Ende einer Signalelektrode verbundenen Ausgangsanschluß aufweist und einen Transistor, der auf das Energie-Ein-Signal hin den vorbestimmten Spannungswert an den Ausgangsanschluß gibt.

5. Verfahren zum Betreiben einer Flüssigkristallanzeigevorrichtung mit einer Vielzahl Anzeigepixeln an Schnittpunkten von Abtast- und Signalelektroden, die in Form einer Matrix angeordnet sind, wobei gleichermaßen gesteuerte erste und zweite Treiberschaltungen (8) verwendet werden, die zum Treiben entgegengesetzter Enden der Abtastelektroden geschaltet sind, **dadurch gekennzeichnet,** daß ein Energie-Ein-Signal (INH) für eine vorbestimmte Zeitdauer vom Energieeinschalten ab erzeugt wird, um die ersten und zweiten Treiberschaltungen so zu steuern, daß sie gleiche Ausgangssignale abgeben.

6. Verfahren nach Anspruch 5, wobei die Vorrichtung gleichermaßen gesteuerte dritte und vierte Treiberschaltungen (5) aufweist, die zum Treiben entgegengesetzter Enden der Signalelektroden geschaltet sind, **dadurch gekennzeichnet,** daß ein Energie-Ein-Signal (INH) für eine vorbestimmte Zeitdauer vom Energieeinschalten ab erzeugt wird, um die dritten und vierten Treiberschaltungen zur Abgabe gleicher Ausgangssignale zu steuern.

Revendications

1. Un dispositif d'affichage plat à cristaux liquides, comportant une pluralité de pixels d'affichage aux points d'intersection des électrodes de balayage et des électrodes de signal agencées sous la forme d'une matrice (1), comprenant des premier et deuxième circuits d'attaque pilotés de façon identique (8), les premiers circuits d'attaque étant connectés pour exciter les électrodes de balayage depuis une extrémité, et les deuxièmes circuits d'attaque étant connectés pour exciter les électrodes de balayage à partir de l'autre extrémité, caractérisé par des moyens sensibles à un signal de mise sous tension (INH) pendant une durée prédéterminée, à partir de la mise sous tension, afin de contrôler les premiers et deuxièmes circuits d'attaque pour donner des signaux de sortie égaux.

2. Un dispositif selon la revendication 1, comprenant des troisième et quatrième circuits d'attaque pilotés de façon identique (5), les troisièmes circuits d'attaque étant connectés pour exciter les électrodes de signal à partir d'une extrémité et les quatrièmes circuits d'attaque étant connectés pour exciter les électrodes de signal à partir de l'autre extrémité, caractérisé par des moyens sensibles à un signal de mise sous tension (INH) pendant une durée prédéterminée à partir de la mise sous tension, afin de commander les troisièmes et quatrièmes circuits d'attaque pour qu'ils donnent des signaux de sortie égaux.

3. Un dispositif selon la revendication 1 ou 2, dans lequel chacun des premiers circuits d'attaque comprend une borne de sortie (OUT) connectée à l'une des extrémités d'une électrode de balayage et un transistor qui émet en sortie une tension de niveau prédéterminée à la borne de sortie en réponse au signal de mise sous tension, et chacun des deuxième circuits d'attaque comprend une borne de sortie connectée à l'autre extrémité d'une électrode de balayage et un transistor qui fournit en sortie le niveau de tension prédéterminé à la borne de sortie en réponse au signal de mise sous tension.

4. Un dispositif selon la revendication 3, en relation à la revendication 2, dans lequel chacun des troisièmes circuits d'attaque comprend une borne de sortie connectée à une extrémité d'une électrode de signal et un transistor qui fournit en sortie un niveau de tension prédéterminé à la borne de sortie en réponse au signal de mise sous tension, et chacun des quatrièmes circuits d'attaque comprend une borne de sortie connectée à l'autre extrémité d'une électrode de signal et un transistor qui fournit en sortie le niveau de tension prédéterminé à la borne de sortie en réponse au signal de mise sous tension.

5. Un procédé pour assurer le fonctionnement d'un dispositif d'affichage plat à cristaux liquides comportant une pluralité de pixels d'affichage aux points d'intersection d'électrodes de balayage et d'électrodes de signal agencé sous la forme d'une matrice, utilisant des premiers et seconds circuits d'attaque (8) pilotés de façon identique, connectés pour exciter des extrémités opposées des électrodes de balayage, caractérisé par la fourniture d'un signal de mise sous tension (INH) pendant une durée prédéterminée, à partir de la mise sous tension, pour commander les premiers et deuxièmes circuits d'attaque afin qu'ils fournissent des signaux de sortie égaux.

6. Un procédé selon la revendication 5, dans lequel le dispositif comprend des troisièmes et quatrièmes circuits d'attaque (5) pilotés de façon identique, connectés pour exciter les extrémités opposées des électrodes de signal, caractérisé par la fourniture d'un signal de mise sous tension (INH) pendant une durée prédéterminée à partir de la mise sous tension, pour commander les troisième et quatrième circuits d'attaque, afin qu'ils fournissent des signaux de sortie égaux.

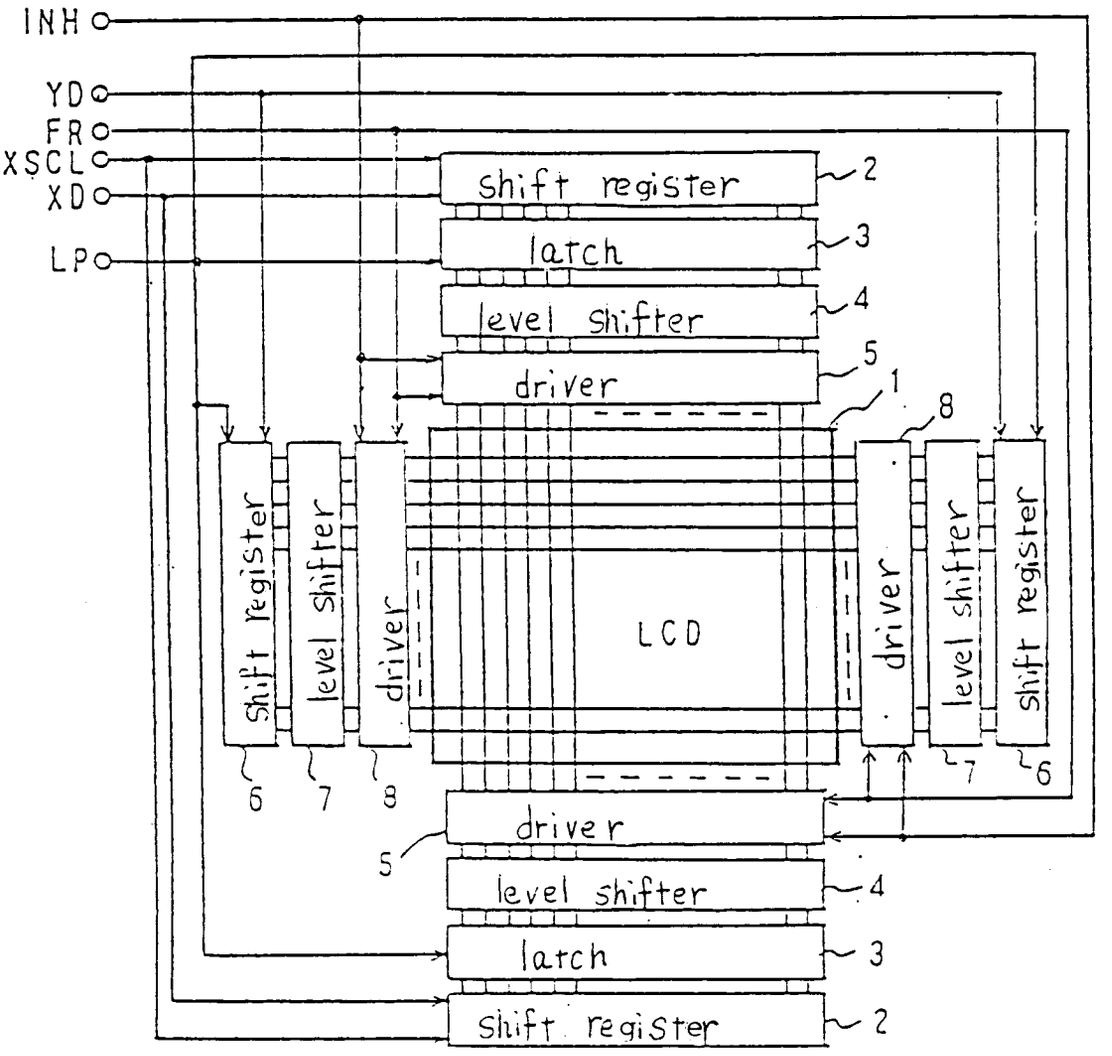
INH
YD
FR
XSCL
XD
LP
shift register
latch
level shifter
driver
LCD
Shift register
level shifter
driver
driver
level shifter
shift register
driver
level shifter
latch
shift register
1
2
3
4
5
6
7
8

Fig. 1

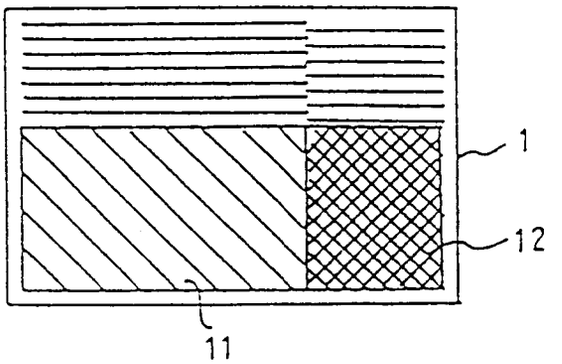

Fig. 2

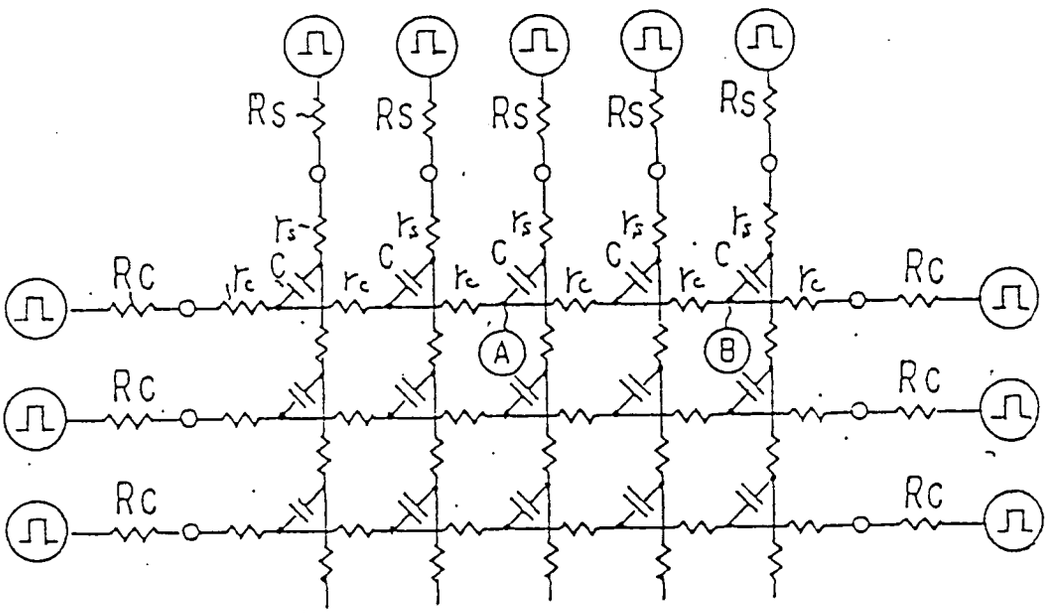

Fig. 3

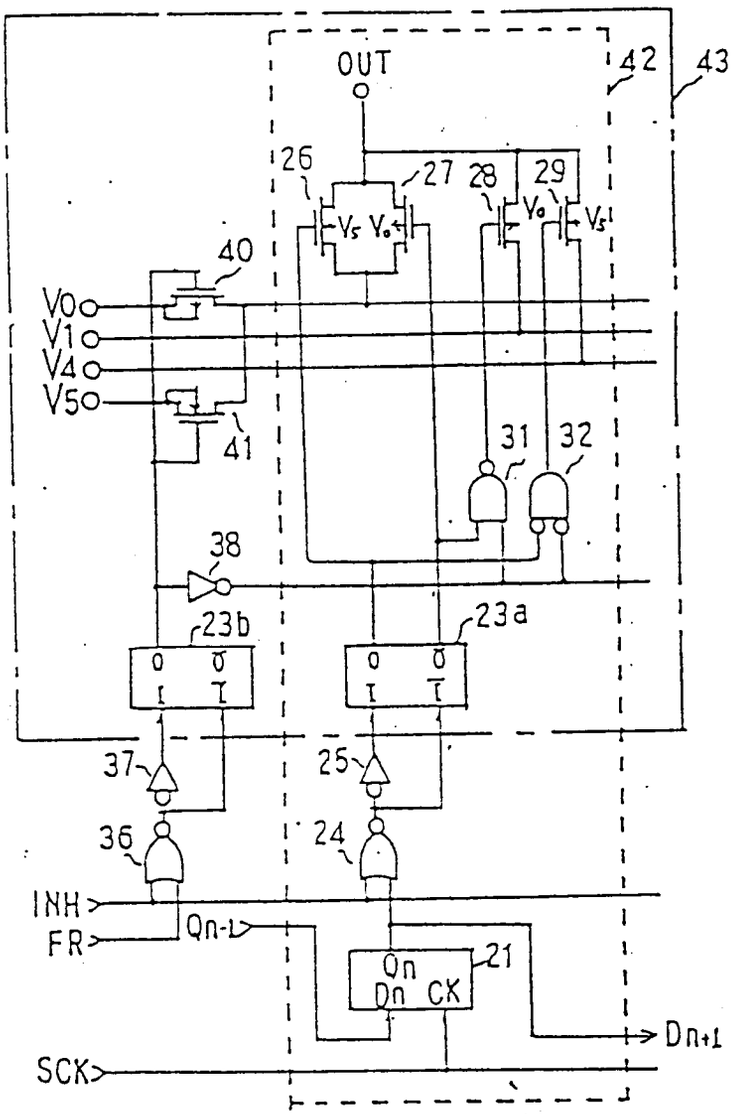
OUT
42
43
26
27
28
29
40
V0
V1
V4
V5
41
31
32
38
23b
23a
37
25
36
24
INH
FR
Qn-1
Qn
Dn
CK
21
Dn+1
SCK

Fig. 4