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(54) An IC chip for an analog electronic watch.

(57) An IC chip (20) for an analog electronic watch has a core CPU (201), a program memory (202) for storing software for actuating the core CPU, and a motor drive controlling circuit (212) for controlling a plurality of step motors according to commands of the software. An analog electronic watch having such an IC chip also has a plurality of step motors, and at least one gear train mechanism to couple each step motor to a rotatable indicator hand. Drive of the step motors can be controlled arbitrarily according to the software stored in the program memory.

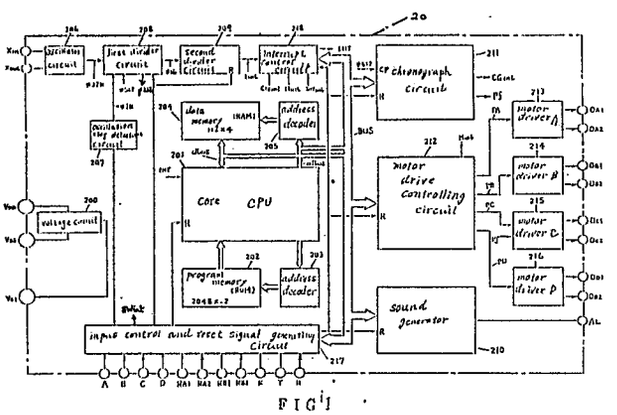

FIG 1

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Description

AN IC CHIP FOR AN ANALOG ELECTRONIC WATCH

The present invention relates to IC chips for analog electronic watches and to analog electronic watches having multi-function indicating means controlled by such IC chips.

As disclosed in Japanese Laid-Open Patent Application No. 286783/1986, Japanese Laid-Open Patent Application No. 294388/1986, Japanese Laid-Open Utility Model Application No. 26191/1986 analog electronic watches having multi-function indicating means use IC chips designed exclusively and individually therefor.

Problems therefore arise, in that:-

(1) the development time for a specialised IC chip is long, so that time is lost in catering for current market demands;

(2) such an IC chip must be modified on a large scale if additional functions are needed or specifications are changed (if the worse comes to the worst, the whole IC chip must be replaced); and

(3) a single IC chip cannot cope with function variations.

The present invention seeks to overcome the aforementioned problems, and to provide an IC chip for an analog electronic watch, which can be developed in a short period of time, is capable of catering for function addition and change of specification, and also to function variations, and thus to satisfy diverse consumers' needs.

According to the present invention, an IC chip for an analog electronic watch, comprises a core CPU, a program memory for storing software for actuating the core CPU, a plurality of motor drivers, and a motor drive controlling circuit for selectively supplying the motor drivers with predetermined driving signals according to commands of the software.

The motor drive controlling circuit may have a plurality of motor clock control circuits, each for controlling the number of driving pulses to be applied to a step motor.

The motor drive controlling circuit may have a drive reference signal forming circuit for forming a drive reference clock signal to act as a trigger for step motor drive, the drive reference signal forming circuit selecting the frequency of the drive reference clock signals according to commands of the software.

The motor drive controlling circuit may include a plurality of driving pulse forming circuits for generating different waveforms of motor driving pulse and a motor drive system controlling circuit for determining which waveform of driving pulse is to be selected for a step motor according to commands of the software.

The invention extends to an analog electronic watch comprising such an IC chip, a plurality of step motors, and at least one gear train mechanism to couple each step motor to a rotatable indicator hand.

It will be appreciated that with such a construction of the invention, the drive of each of a plurality of step motors can be controlled arbitrarily by software stored in the program memory.

The invention is described further, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a block diagram representing an IC chip for an analog electronic watch in one embodiment of the invention;

Figure 2 is a block diagram representing a chronograph circuit forming part of the circuit of Figure 1;

Figure 3 is a block diagram representing a motor drive controlling circuit forming part of the circuit of Figure 1;

Figure 4 is a block diagram representing a drive reference signal forming circuit forming part of the circuit of Figure 3;

Figures 5, 6, 7 and 8 are timing charts of motor driving pulses generated from first, second, third and fourth driving pulse shaping circuits respectively, forming part of the circuit of Figure 3;

Figure 9 is a block diagram representing one of four motor clock control circuits forming part of the circuit of Figure 3;

Figure 10 is a plan view of one embodiment of an analog electronic watch according to the invention;

Figure 11 is a sectional view of gear trains in the watch of Figure 10 for driving hands to indicate ordinary time in hours and minutes;

Figure 12 is a sectional view of a gear train in the watch of Figure 10, for driving a hand to indicate ordinary time in seconds;

Figure 13 is a sectional view of a gear train in the watch of Figure 10, for driving a stopwatch second hand;

Figure 14 is a sectional view of gear trains in the watch of Figure 10, for driving a hand to indicate a chronograph minute and a timer second;

Figure 15 is a sectional view of a gear train in the watch of Figure 10, for driving hands to indicate an alarm set time;

Figure 16 is a circuit connection diagram of the watch of Figure 10;

Figure 17 is a front view of a complete multi-function electronic watch according to one embodiment of the invention;

Figures 18 (a) and 18 (b) are flow charts of alternative steps for indicating ordinary time;

Figures 19 (a) and 19 (b) are flow charts of alternative steps of a chronograph function;

Figures 20 (a) and 20 (b) are flow charts of alternative steps of a timer function;

Figures 21 (a), 21 (b) and 21 (c) are flow charts of alternative steps of an alarm function; and

Figures 22 (a), 22 (b) and 22 (c) are flow charts of alternative steps of driving methods of the motor.

A CMOS-IC chip 20 (Figure 1) is a one chip micro-computer for an analog electronic watch with a program memory 202, a data memory 204, four motor drivers 213, 214, 215 and 216, a motor drive controlling circuit 212, a sound generator 210, an interrupt control circuit 218 and other circuits integrated on one chip around a core CPU 201.

The core CPU 201 comprises an ALU, a register for arithmetic operations, an address controlling register, a stack pointer, an instruction register, an instruction de-coder and other functional circuits, and is connected to peripheral circuits through an address bus adbus and a data bus dbus according to a memory-mapped I/O system.

The program memory 202 consists of a mask read only memory ROM of 2,048 words x 12 bits, storing software for operating the IC, and has an address de-coder 203.

The data memory 204 consists of a random access memory RAM of 112 words x 4 bits which is used for various timers, counters for storing hand position of each pointer and others, and has an address de-coder 205.

An oscillator circuit 206 oscillates at 32,768 Hz with a tuning fork crystal resonator connected to terminals Xin and Xout as an oscillation source.

A first divider circuit 208 divides the 32,768 Hz signal Ø32k generated from the oscillator circuit 206 in sequence and generates a 1 kHz signal Ø1k, a 512 Hz signal Ø512, a 256 Hz signal Ø256, and a 16 Hz signal Ø16. An oscillation stop detection circuit 207 is connected to receive the signal Ø1k and, when a stop of oscillation of the oscillator circuit 206 is detected, applies a re-set to the system.

A second divider circuit 209 divides the signal Ø16 from the first divider circuit 208 in sequence into 8 Hz, 4Hz, 2 Hz and 1 Hz signals, which can be read into the core CPU 201 by the software.

The 16 Hz signal Ø16, 8 Hz signal Ø8, and 1 Hz signal Ø1 are used as a time interrupt (Tint) for processing such as time keeping or the like. The time interrupt (Tint) is generated at the fall of each signal. Read, re-set and mask of each interrupt source are all effected by the software, and re-set and mask are read individually at every source.

The sound generator 210 can generate a buzzer driving signal to a terminal AL. Driving frequency, ON/OFF operation and sound pattern of the buzzer driving signal can be controlled by the software.

The chronograph circuit 211 (Figure 2) provides a 1/100 sec chronograph, though the drive of the 1/100 sec hand is controlled by hardware to lighten the load on the software.

The circuit 211 includes a clock forming circuit 2111 which forms 100 Hz signal Ø100 working as a reference clock for chronography from 512 Hz signal Ø512, and a clock pulse Pfc 100 Hz and 3.91 ms in pulse width for forming 1/100 sec hand driving pulse Pf. A 50-proceeding chronograph counter 2112 counts signals Ø100 passing through an AND gate 2119 and is re-set on a chronograph re-set signal Rcg generated by a control signal forming circuit 2118. A register 2113 holds the contents of the chronograph counter 2112, when a split indication command signal Sp is generated by the control signal forming circuit 2118. A 50-proceeding hand position counter 2114 stores 1/100 sec hand indication position of the 1/100 sec hand by counting 1/100 sec hand driving pulses Pf from a 1/100 sec hand drive controlling circuit 2117 and is re-set by a signal Rhnd from the control signal forming circuit 2118 to store a zero position on the 1/100 sec hand.

An identity detection circuit 2115 compares the contents of the register 2113 and of the hand position counter 2114 and generates an identity signal Dty when identity is detected. A zero position detection circuit 2116 generates a zero detection signal DtØ upon detection of zero in the hand position counter 2114.

The control signal forming circuit 2118 receives instructions over the bus BUS and forms and generates a start signal St, a chronograph re-set signal Rcg, a split signal Sp, a drive signal Drv and the zero position signal Rhnd. The start signal St is passed to AND gate 2119 and to circuit 2117 to command a measurement start or stop according to a command of the software. The split signal Sp is passed to register 2113 and circuit 2117 to command a split indication or split indication release. The chronograph re-set signal Rcg is passed to counter 2112 to command a re-set of measurement. The zero position signal Rhnd is passed to counter 2114 to store a zero position of the 1/100 sec hand. The drive signal Drv is passed to circuit 2117 to command operation or inoperation of the 1/100 sec hand. The 1/100 sec hand drive controlling circuit 2117 receives clock pulses Pfc from circuit 2111 and passes clock pulses Pfc when the contents of the chronograph counter 2112 and the hand position counter 2114 are identical in the state when the 1/100 sec hand operates and also during measuring, that is when signals Dty and Drv or St are up. The circuit 2117 also passes clock pulses Pf when the contents of the register 2113 and the hand position counter 2114 are not identical at the time of split indication and also stop of measuring, that is when signal Dty is down and signal Sp is up or signal St is down. The circuit 2117 also passes clock pulses Pf when the contents of the hand position counter 2114 is other than zero in the state when the 1/100 sec hand is not operating and also during measuring, that is when signal DtØ is down and signal Drv is down or signal St is up. The clock pulses Pf are supplied to motor driver 215 (Figure 1) so that the 1/100 sec hand is ready for driving only by a step motor C. Further, a chronograph interrupt CGint (Figure 2) is generated on a 5 Hz carry signal Ø5 coming from the chronograph counter 2112, and a measurement after 1/5 seconds is ready for processing by the software.

The motor drive controlling circuit 212 (Figure 3) generates motor driving pulses for each motor driver according to commands from the software.

The circuit 212 includes a motor drive system controlling circuit 219 which stores a drive system for each motor and according to commands from the software forms and generates control signals, namely, signal Sa for selecting a forward drive I, signal Sb for selecting a forward drive II, signal Sc for selecting a reverse drive I, signal Sd for selecting a reverse drive II, and signal Se for selecting a forward

corrective drive.

The circuit 212 also includes a drive reference signal forming circuit 220 (Figure 4) for forming and generating a drive reference clock signal Cdrv according to commands from the software over the bus BUS. The circuit 220 includes a 3-bit register 2201 which stores data supplied over the data bus dbus for deciding the frequency of the driving reference clock signal Cdrv according to the output signal of an address de-coder 2202 receiving addresses over the address bus adbus from the software. The circuit 220 also includes a 3-bit register 2203 which is loaded with the data in the register 2201 at the fall of the driving reference clock signal Cdrv generated by a programmable dividing circuit 2205. The circuit 220 also includes a de-coder 2204 generating numerals 2, 3, 4, 5, 6, 8, 10 and 16 in binary form corresponding to data stored in the register 2203. The programmable dividing circuit 2205 divides the 256 Hz signal Ø256 generated from the first divider circuit 208 by n, being the numeral generated by the de-coder 204. Accordingly, the drive reference signal forming circuit 220 is capable of selecting the frequency of the drive reference clock signal Cdrv from among eight kinds, namely, 128 Hz., 85.3 Hz, 64 Hz, 51.2 Hz, 42.7 Hz, 32 Hz, 25.6 Hz and 16 Hz. The frequency of the drive reference clock signal Cdrv is changed at the point in time when data is loaded into the register 2203, and the data is loaded into the register 2203 synchronously with the drive reference clock signal Cdrv. Therefore an interval of 1/fa will be secured when the frequency fa is switched to the next frequency fb.

The circuit 212 also includes four motor clock controlling circuits 226, 227, 228, 229 which control driving pulse numbers of step motor A, step motor B, step motor C, step motor D, respectively, according to commands from the software. As the circuits are identical, only one circuit 226 (Figure 9) will be described in detail. The circuit 226 includes a 4-bit register 2261 which stores a driving pulse number commanded by the software. A 4-bit up-counter 2262 counts drive reference clock signals Cdrv passing through AND gate 2274, and is re-set by a control signal. A control signal forming circuit 2272 receives instructions over the address bus adbus, and forms and generates a signal Sset for setting a driving pulse number on the data bus dbus in the register 2261 according to commands from the software, a signal Sread for reading data of the up-counter 2262, and a signal Sreset for re-setting the register 2261 and the up-counter 2262. The signal Sread is supplied to an inverter 2273 whose output is to the AND gate 2274, so that the driving reference clock signals Cdrv are prohibited from passing the AND gate 2274. A two-way switch 2271 is turned to ON when the signal Sread is generated, thus applying data of the up counter 2262 onto the databus dbus. In this case, the register 2261 and up-counter 2262 must be re-set after reading by the signal Sreset.

An identity detection circuit 2263 compares the contents of the register 2261 and the up-counter 2262 and generates an identity signal Dy when the contents are identical. An all-1 detection circuit 2264 generating an all-1 detection signal D15 when the contents of the register 2261 are all 1s. A motor driving pulse forming trigger signal generation circuit 2265 comprises inverters 2266 and 2267, a 3-input AND gate 2268, a 2-input AND gate 2269 and a 2-input OR gate 2270.

The circuit 2265 receives clock signals Cdrv supplied as inputs to AND gates 2268 and 2269, the identity signal Dy as input to inverter 2266 whose output is one input of AND gate 2268, and the all-1 detection signal D15 as input to AND gate 2269 and as input to inverter 2267 whose output is one input to AND gate 2268. The outputs of AND gates 2268 and 2269 are ORed in OR gate 2270 whose output is a motor trigger signal Tr. When a number, other than all 1s, is set in register 2261, which number differs from that in register 2262, trigger signals Tr are generated through AND gate 2268 until the numbers agree, when the identity signal Dy stops such generation. When the register 2261 is set to all 1s, the circuit 2265 generates trigger signals Tr repeatedly through AND gate 2269 even when an identity signal Dy is generated.

When the identity detection circuit 2263 detects identity or when the pulse number is set at zero, a motor control interrupt Mint is generated, which interrupt can be read by the software, and can be re-set after reading.

The circuit 212 (Figure 3) includes four trigger forming circuits 230, 231, 232 and 233, each receiving a signal Sa, Sb, Sc, Sd or Se from circuit 219 and passing a trigger signal Tr generated from the corresponding motor clock controlling circuit as trigger signals Sat, Sbt, Sct, Sdt, Set for drive pulse controlling circuits 221, 222, 223, 224 and 225 to form motor driving pulses Pa, Pb, Pc, Pd, Pe correspondingly to drive system control signals Sa, Sb, Sc, Sd, Se generated from the motor drive system controlling circuit 219.

When the forward drive I and the reverse drive are carried out continuously, the frequency of the driving reference clock Cdrv is limited to below 64 Hz. The first drive pulse forming circuit 221 forms and generates the driving pulse Pa for forward drive I (Figure 5). The second drive pulse forming circuit 222 forms and generates the driving pulse Pb for forward drive II (Figure 6). The third drive pulse forming circuit 223 forms and generates the driving pulse Pc for the reverse drive I Figure 7). The fourth drive pulse forming circuit 224 forms and generates the driving pulse Pd for reverse drive II (Figure 8). The fifth drive pulse forming circuit 225 forms and generates a pulse group Pe for corrective drive, comprising ordinary driving pulse P1, correction driving pulse P2, pulse P3 at the time of AC magnetic field detection, AC magnetic field detecting pulse SP1, rotation detecting pulse SP2, as disclosed in Japanese Laid-Open Patent No. 260883/1985.

Four motor driving pulse selection circuits 234, 235, 236 and 237 (Figure 3), select and generate driving pulses PA, PB, PC and PD, respectively, necessary for a step motor from among the motor driving pulses Pa, Pb, Pc, Pd, Pe generated by the driving pulse forming circuits 221 to 225, corresponding to the drive system control signals Sa, Sb,

Sc, Sd or Se received.

The motor drivers 213, 214, 215 and 216, each drive a step motor by passing motor driving pulses PA, PB, PC and PD, respectively, coming from the motor driving pulse selection circuit 212 alternately to two output terminals of each motor driver.

An input control and re-set signal forming circuit 217 receives switched inputs at terminals A, B, C, D, RA1, RA2, RB1 and RB2, and inputs at terminals K, T and R. The circuit 217 also receives data and instructions on bus BUS and any re-set input from the oscillation stop detection circuit 207.

The interrupt control circuit 218 operates to give precedence to each switch interrupt SWint, chronograph interrupt CGint, motor control interrupt Mint, storage before reading, and re-set R after reading, by issuing a signal INT. A constant voltage circuit 200 provides a low constant voltage of about 1.2 V at terminal VS1 from a battery voltage of about 1.58 V impressed across terminals VDD and VSS. If there is a switched input at any one of the terminals A, B, C, D, RA1, RA2, RB1 or RB2, a switch interrupt signal SWint is generated. In this case, read and re-set of the interrupt source are carried out by the software. Then, each input terminal is pulled down to the level of terminal VSS representing data 0, where data 1 is represented by the level of terminal VDD.

The terminal K is that for switching specifications, and two kinds of specifications can be selected according to the data on terminal K. Then, the data on the terminal K is read by the software.

The terminal R is that for system re-setting, and when the terminal R is at the level of terminal VDD, the core CPU 201, the divider circuits 208 and 209 and other peripheral circuits are initialised by the hardware.

The terminal T is that for converting the test modes, and by inputting a clock pulse to the terminal T with the terminal RA2 at the level of terminal VDD, sixteen test modes for testing peripheral circuits can be changed. The main test mode comes in a forward drive I ensuring mode, a forward drive II ensuring mode, a reverse drive I ensuring mode, a reverse drive II ensuring mode, a corrective drive ensuring mode, a chronograph 1/100 sec ensuring mode and others, and in these ensuring modes, the motor driving pulse is generated automatically to each motor driving pulse output terminal.

The system can be re-set by connecting the terminal R to the level of terminal VDD and also by closing the switches concurrently otherwise. In the IC, the system will be re-set forcibly by hardware when A or C, and B and RA2 are closed concurrently, and also when one of A, B and C, and RA2 and RB2 are closed concurrently.

Then, functions to re-set the divider circuit and other peripheral circuits are available by the software, and when the peripheral circuits are re-set, the divider circuits will also be re-set.

Thus, the CMOS-IC 20 has the following features for the drive of step motors, and is extremely effective as IC chip for multi-hand type multi-functional analog electronic watches:-

1. the motor drivers 213, 214, 215 and 216, so that the four step motors can be driven concurrently;

2. the motor drive system controlling circuit 219, the drive pulse forming circuits 221 to 225 and the motor drive pulse selection circuits 234 to 237, so that three kinds of forward drive and two kinds of reverse drive on each of the four step motors can be effected by the software;

3. the drive reference signal forming circuit 220, so that the drive speed of each step motor can be arbitrarily changed by the software; and

4. the motor clock controlling circuits 226 to 229 each corresponding to a step motor, so that a driving pulse number can be set arbitrarily for each step motor.

An embodiment of a multi-functional analog electronic watch (Figure 10) according to the invention incorporates a CMOS-IC 20 as hereinbefore described. The watch includes a base plate 1 formed of a plastics resin material, and a silver oxide battery 2 (SR927W). There are four step motors A, B, C, and D, referenced in Figure 10 as 3, 15, 27 and 32. The step motor 3 for indicating ordinary time, comprises a magnetic core 3a of high permeability material, a coil block 3b consisting of a coil wound on the magnetic core 3a, a coil lead substrate having the opposite ends processed to be conductive and a coil frame, a stator 3c formed of high permeability material, and a rotor 4 consisting of a rotor magnet and a pinion 4a (Figure 11).

A fifth wheel 5 has a gear 5a engaged with the pinion 4a, and a pinion 5b engaged by a gear 6a of a fourth wheel 6. The wheel 6 has a pinion 6b engaged by a gear 7a of a third wheel 7 which also has a pinion 7b engaged by a gear 8a of a minute wheel 8. The wheel 8 has a pinion 8b engaged by a gear 9a of an intermediate wheel 9 having a pinion 9b engaged by a gear 10a of an hour wheel 10. The minute wheel 8 and hour wheel 10 have their axes disposed centrally of the watch face and have noses projecting therethrough carrying minute and hour hands 11 and 12, respectively. The various pinions, wheels and gears of the gear train are mounted on bearings in the base plate 1 and a spaced plate 53 (Figures 11 to 15). The plate 53 (Figure 15) is recessed to receive a circuit substrate 54 held in place by a plate 52.

The reduction ratio between the rotor pinion 4b and the minute wheel gear 8a is 1/1800, so that the minute wheel 8 and hand 11 rotate once for every 1800 rotations of the rotor 4. If the rotor 4 rotates once in two seconds, that produces a single revolution of the wheel 8 per 3600 seconds or 60 minutes or one hour. The reduction ratio between the minute pinion 8b and the hour wheel gear 10a is 1/12, so that with the rotor 4 rotating once in two seconds, the hour wheel rotates once in twelve hours.

The pinion 5b of the fifth wheel 5 (Figure 12) is also engaged by a gear 13a of a small second wheel 13 whose axis of rotation is disposed eccentrically of the watch face and along the position of the hour hand at 9 o'clock (Figure 17). The wheel 13 has a nose projecting through the watch face 41 (Figure 12) and carrying a small second hand 14. The reduction gear ratio between the rotor pinion 4a and the small second gear 13a is 1/30, and thus the small

second wheel 13 turns once per 60 seconds when the rotor 4 rotates once per two seconds, thereby indicating seconds of ordinary time.

The step motor 15 (Figure 10) for chronograph second hand indication, comprises a magnetic core 15a of high permeability material, a coil block 15b consisting of a coil wound on the magnetic core 15a, a coil lead substrate with the opposite ends processed to be conductive and a coil frame, a stator 15c consisting of high permeability material, and a rotor 16 consisting of a rotor magnet and a rotor pinion 16a (Figure 13).

The rotor pinion 16a is engaged by a gear 17a of a chronograph first intermediate wheel 17 having a pinion 17b engaged by a gear 18a of a chronograph second intermediate wheel 18. The wheel 18 has a pinion 18b engaged by a gear 19a of a chronograph wheel 19. The chronograph wheel 19 is disposed centrally of the watch and has a nose projecting through the noses of the minute and hour wheels 8 and 10, and carries a hand 21. The wheel 19 is urged into engagement with the wheel 8 by a spring 65 (Figures 11 to 15) pressing on a bearing portion projecting through the plate 53. The reduction gear ratio between the rotor pinion 16a and the chronograph gear 19a is 1/150. The rotor 16 rotates two and a half times or 900° per second on electrical signals from CMOS-IC 20, so that the chronograph wheel 19 rotates 6° per second, or five steps of 1.2°, thereby indicating 60 chronograph seconds per revolution. The hand 21 functions as a timer set hand for timer setting at the same time in a timer operation described hereinafter.

The step motor 27 (Figure 10) for minute indication of the chronograph and second indication of an elapsed time of the timer, comprises a magnetic core 27a of high permeability material, a coil block 27b consisting of a coil wound on the magnetic core 27a, a coil lead substrate with the opposite ends processed to be conductive and a coil frame, a stator 27c consisting of high permeability material, and a rotor 28 consisting of a rotor magnet and a rotor pinion 28a (Figure 14). The rotor pinion 28a is engaged by a gear 29a of a chronograph minute intermediate wheel 29 having a pinion 29b engaged by a gear 30a of a chronograph minute wheel 30. The chronograph minute wheel 30 is disposed to rotate on an axis eccentric to the watch face and along the position of the hour hand at 12 o'clock. A minute indication of the chronograph and a second indication of an elapsed time of the timer are made on that axis. The reduction gear ratio between the rotor pinion 28a and the chronograph minute gear 30a is 1/30. In the chronograph mode, the rotor 28 rotates once per minute on electrical signals from CMOS-IC 20. Accordingly, the chronograph minute wheel 30 rotates 12° per minute, or once every half hour, thus realising a chronograph minute indication of 30 minutes. The wheel 30 has a nose projecting through the watch face 41 and carrying a chronograph minute hand 31 for chronograph minute indication. By combining the indications of the chronograph hands 21 and 31, a chronograph indication is realised with 1/5 seconds as minimum reading unit and 30 minutes as maximum.

In the timer mode, the rotor 28 rotates counter to that of chronograph mode once every two seconds on electrical signals from CMOS-IC 20. Thus the chronograph minute hand 31 rotates once counter-clockwise every 60 seconds in steps of one second, thus indicating seconds of an elapsed time of the timer in a 60 seconds rotation. At the same time, the rotor 16 rotates two and a half times per minute counter to that of chronograph mode on electrical signals from the CMOS-IC 20. Accordingly, the central chronograph hand 21 turns counter clockwise at 6° per minute, thus indicating minutes of elapsed time of the timer. The CG minute hand 31 driven by the step motor 27 acts as the 1/100 second hand referred to in connection with Figure 2, when controlled by software.

The watch has first and second manually operable stems 22 and 23 (Figure 17) and three switch operating buttons 24, 25 and 26. In setting the timer, the second stem 23 is placed in a first state and the rotor 16 rotates through 180° in five steps whenever a button 25 is pushed once to close the switch connected to terminal B, so that the chronograph hand 31 turns 6° representing one minute. Thus a timer set time as long as 60 minutes can be shown.

The step motor 32 (Figure 10) comprises a magnetic core 32a of high permeability material, a coil block 32b consisting of a coil wound on the magnetic core 32a, a coil lead substrate with the opposite ends processed to be conductive and a coil frame, a stator 32c consisting of high permeability material, and a rotor 33 consisting of a rotor magnet and a rotor pinion 33a (Figure 15). The rotor pinion 33a is engaged by a gear 34a of an alarm intermediate wheel 34 having a pinion 34b engaged by a gear 35a of an alarm minute wheel 35. The wheel 35 has a pinion 35b engaged by a gear 36a of a third alarm wheel 36 having a pinion 36b engaged by an alarm hour wheel 37. The reduction ratio between the rotor pinion 33a and the alarm minute gear 35a is 1/30, and the reduction ratio between the alarm minute pinion 35b and the alarm hour wheel 37 is 1/12. The wheels 35 and 37 rotate about a common axis disposed eccentrically of the watch face along the position of the hour hand at 6 o'clock. The wheel 35 carries an alarm minute hand 38 and the wheel 37 carries an alarm hand 39.

When the second stem 23 is in the first state to select a timer set or alarm mode, the rotor 33 is rotated through 180° on an electrical signal from the CMOS-IC 20 by pushing the button 26 once to close the switch connected to terminal C. The alarm minute hand 38 turns through 6° representing 1 minute, and the alarm hour hand 39 turns through 0.5°. Thus the alarm time can be set at minute intervals up to 12 hours. For this, if the button 26 is pressed continuously, the alarm minute hand 38 and the alarm hour hand 39 rotate rapidly, thus setting the alarm time in a short time. When the set alarm time and the ordinary time coincide, an alarm rings.

When the second stem 23 is placed in the zero state, an alarm off mode is selected, and the alarm minute hand 38 and the alarm hour hand 39 indicate ordinary time. In this case, the rotor 33 is rotated in steps of 180° at every minute on an electrical signal

from CMOS-IC 20.

The CMOS-IC 20 is connected with other electric elements as shown in the circuit diagram of Figure 16. These other elements include buzzer driving elements consisting of a boosting coil 55, a mini-mold, or small sized surface coupling, transistor 56 with protective diode and a piezo-electric buzzer 64 applied to a back cover of the watch case. A 1uF chip capacitor 57 suppresses voltage fluctuations of the constant voltage circuit 200. A micro tuning fork type crystal oscillator 58 is the source for the oscillator circuit 206 through terminals Xin and Xout. A three position switch 46a can be closed on terminal RA1 or on terminal RA2 or be open. A similar three position switch 59a can be closed on terminal RB1 or on terminal RB2 or be open.

The buttons 24, 25 and 26 are spring-biased and can only close their switches when pushed. The switch 46a is on a yoke 46 engaged with the first stem 22, so as to close with terminal RA1 in a first state of the first stem 22, to close with terminal RA2 in a second state and to open normally. Likewise, the switch 59a is on a lever 59 engaged with the second stem 23, so as to close with terminal RB1 in a first state of the second stem 23, to close with terminal RB2 in a second state, and to open normally.

The watch (Figure 17) has a case 40. On the watch face 41 are indicia 42 for ordinary second time, indicia 43 for a chronograph minute and timer elapsed time second indication, and indicia 44 for an alarm set time indication.

Ordinary time is indicated by the small second hand 14 stepping at every second, whilst the minute hand 11 and the hour hand 12 rotate more slowly. For correcting the time, the first stem 22 is pulled out to the second state. The first stem 22 engages a lever 45 and yoke 46 to move a setting lever 47 which engages and stops the fourth wheel 6. The first stem 22 is then rotated and through a clutch wheel 48 rotates a setting pinion 50 in either direction. The pinion 50 (Figure 11) is engaged with the gear 9a of the intermediate wheel 9. Rotation of the wheel 9 is transferred to the minute wheel 8 and the hour wheel 10. The gear 8a of the minute wheel 8 is coupled to the wheel 8 and pinion 8b with constant sliding torque, so that relative rotation can occur under the torque applied manually through the stem 22 because the stopping of the fourth wheel 6 also stops the third wheel 7 and gear 8a. The rotor 4 also stops and the second wheel 13 (Figure 12) also stops. When the minute and hour hands 11 and 12 have been set to the desired time, the stem 22 is returned from its second state to its normal position and the rotor 4 re-starts rotation to drive the hands 11, 12 and 13.

If a 1 Hz interrupt (Figure 18 (a)) is input, it is first determined whether or not the switch 46a is connected to terminal RA2. If not, then a forward correction drive of the step motor A is set on the motor drive system controlling circuit 219 (Figure 3) and a drive number 1 is set on a motor clock controlling circuit 226. If the switch 46a is connected to the terminal RA2, a time corrected state (Figure 18 (a)), the motor drive is stopped, and divider circuits 208 and 209 are re-set instantaneously so as to drive the motor one second later at the point in time when the switch 46a is turned off.

In the flow chart of the chronograph function (Figures 19 (a) and 19 (b)), CG is used as an abbreviation for chronograph. When a switch input to the circuit 217 occurs, it is first determined whether the second stem 23 is not in the first or second state, so that the switch 59a is not on the terminal RB1 or RB2. If the switch 59a is not on either terminal, then it is determined whether the switch input comes from pushing the button 24 to connect to terminal A. If so, the data memory is read to determine if CGreset or CGstoP is stored therein. If so, then the GC circuit is started and CGstart is written into the memory in place of CGreset or CGstoP. CGstart causes the CG second hand 21 to be driven five steps per second from the zero position from which it starts. The number of seconds is counted in both the counter 2113 and the counter 2114 and after 60 seconds, a carry causes the CG minute hand 31 to be stepped to indicate the passage of one minute of time.

This continues until another switch input occurs and is found to be from the terminal A due to a push on the button 24. It is first determined whether CG start has occurred and because CGstart is written in the memory, the CG circuit is stopped and CGstoP is written into the memory in place of CGstart. Thus the CG second hand 21 and the CG minute hand 31 are both stopped and the elapsed time can be read off the watch face. If, whilst CGstart is in the memory, a switch input is found not to be from terminal A, it is determined whether it is from terminal B. If so, then it arises from a push on the button 25 and CG split is started and CGsplit is written into the memory in place of CGstart. This stops the rotation of the CG second hand 21 and the CG minute hand 31, but continues the counting of the seconds passing in counter 2113. Thus a split time can be read from the hands 21 and 31 off the watch face.

If a further push on button 25 occurs thereafter, and it is determined that CGsplit is in the memory, then a calculation occurs as to the difference between the CG hand position as it is recorded in counter 2114 and the CG hand position as it ought to be as recorded in counter 2113. The difference in circuit 2115 causes the CG hands to be driven quickly until it is eliminated when they continue to rotate at normal forward speed. At the same time, CGstart is re-written into the memory in place of CGsplit.

If, after the button 24 has been pushed to stop the chronograph indication and CGstop has been written into the memory, the button 25 is pushed, then after a determination that CGstart and CGsplit are not in the memory and that CGstop is in the memory, the difference between the hand position and the zero hand position is calculated and the hands rapidly returned to the zero position as indicated in the circuit 2116, whilst CGreset is written into the memory in place of CGstop.

If, after the button 25 has been pushed and CGsplit written into the memory, the button 24 is pushed to close the switch upon terminal A, then the

hand is already stopped at the split time. The counting of seconds is stopped and the accumulated value is retained in memory. If the button 25 is again pushed to close the switch upon terminal A, counting is re-started, but the hand remains stopped.

If the second stem 23 is moved to the first state, the switch 59a engages the terminal RB1 and the flow chart of Figures 20 (a) and 20 (b) indicates the resultant steps in the timer set mode. If a switch input to circuit 217 is detected, it is first determined whether the terminal RB1 is connected. If so, it is determined whether the terminal A is connected due to the button 24 being pushed. If so, it is determined whether timerset or timerstop is written in the memory. There is no need to write timerset into memory, if it is determined that neither timerstart nor timerstop is written in memory, it is assumed that timerset is so written. If so, the timer is started as described in relation to Figure 20 (b) and timerstart is written into the memory. If in the previous determination, it is found that timerstart is written in the memory, then the timer is stopped and timerstop written in the memory. A further push on button 24 re-starts the timer.

If in the initial determination, it is found that the button 25 has been pushed so that the terminal B is connected, it is determined whether timerset is written in the memory. If so, then this indicates that neither timerstart nor timerstop is written in the memory and that a timer operation is not in progress. Accordingly, the timer set time is increased by one minute and this is indicated by clockwise stepping of the CG second hand 21 by five steps representing 6° on the watch face 41. Repeated pushing of the button 25 causes repeated increases and stepping until the CG second hand 21 indicates the desired timer set time. The maximum time that can be set is 60 minutes. When the timer is started by pushing the button 24, the 1 Hz interrupt signal with timerstart written in the memory causes a decrease of one second in the time set each second and the CG minute hand 31 is driven counter clockwise. Every minute, the CG minute hand completes a full circle and the CG second hand 21 is stepped five steps counter clockwise until only one minute remains. Then the CG minute hand 31 stops and the CG second hand 21 is stepped five steps for each second. At each decrease of timer time by one second, it is determined (Figure 20 (b)) whether the time remaining is one to three seconds. If not, then it is determined whether no time remains. If not, then it is determined whether the time remaining is one minute or more. If so, the CG minute hand 31 is stepped by one second counter clockwise and it is determined if the timer second = 0. If so, then the CG second hand 21 is stepped counter clockwise by five steps. If the remaining time is found to be one to three seconds, a command is issued to the sound generator to output a notice sound. If the remaining time is zero, a command is issued to the sound generator to output a time-is-up sound. If the remaining time is less than one minute, the CG second hand 21 is stepped counter clockwise by five steps. If a time of one minute only is set, the elapse of time is only indicated by counter clockwise movement of the CG second hand 21. Otherwise, time elapsed is shown by both hands 21 and 31 until only one minute remains. It will be appreciated that when the remaining time is zero, the CG minute hand 31 is already in a zero position and the CG second hand 21 is stepped through five steps back to the zero position.

A flow chart of the alarm function is illustrated in Figures 21 (a), 21 (b) and 21 (c). When a switch output is received in circuit 217, it is first determined whether the switch 59a is on terminal RB1 due to the second stem 23 being in the first state. If so, it is determined whether the button 25 has been pushed to close on the terminal C. If so, the alarm minute hand 38 is stepped forward by one minute and the alarm hour hand 39 by a corresponding amount. This can be repeated until the desired alarm time is set or the button can be kept pushed in, in which case both hands 38 and 39 are rotated quickly to enable the alarm time to be set in a short time. At the same time, the alarm set time is written into the memory. When a 1 Hz interrupt is received, and the second stem has not been moved into the second state, the alarm current time is increased by one second. It is then determined if the time has increased by one minute, as represented by "figure up?". If so, and it is found that the second stem is still in the first state, the alarm current time and the alarm set time are compared. If identity is found, then a command is issued to the sound generator to output the notice sound. If the second stem is not in the first state, it must be in the zero or normal position and the alarm minute hand is advanced by one step to keep pace with current time. Thereafter, the alarm minute and hour hands 38 and 39 will display the current time. However, if there is a need to correct the position of the hands, the second stem is moved to the second state and rotated to move the hands through the clutch wheel 49 and setting wheel 51 (Figure 15).

If a switch output is detected (Figure 21 (c)), it is determined whether the second stem has been moved from the second state to release the terminal RB2 in operation 2301. If not, the condition of the mode switch in relation to terminal RB1 is checked. In operation 2302, it is determined whether the terminal RB1 has been engaged. If so, the alarm function is changed to indicate the alarm set time. This is effected by calculating the difference between the alarm set time and the alarm current time in operation 2303. A quick driving traverse of the alarm minute and hour hands is effected in operation 2304 until the displayed time coincides with the calculated value and thus the alarm set time. If not, it is determined whether the terminal RB1 has been released in operation 2305. If so, the alarm function is changed to indicate current time. This is effected in operation 2306 by calculating the difference between the alarm current time and the alarm set time. A quick driving traverse of the alarm minute and hour hands is effected in operation 2304 until the displayed time coincides with the calculated value and thus the alarm current time.

Various motor driving methods are illustrated in Figures 22 (a), 22 (b) and 22 (c). When motor

movement is called for (Figure 22 (a)), it is first determined if the pulses required are for reverse I or forward I drives. If so, then the reference clock is set to 64 Hz, whereas if not, it is set to 128 Hz. The selection of the correct motor to drive the hands requiring movement is then made and the number of pulses set in the motor pulse register 2261 (Figure 9). If the drive called for is reverse I or forward I, then the necessary pulses are issued to the selected motor until the contents of the up counter 2262 counting incoming pulses is found to be equal to the contents of the register 2261 by the circuit 2263. The clock signals Cdrv arrive at 64 Hz.

If a quick traverse drive is called for, then the reference clock having been set on 128 Hz, the motor pulse register 2261 is set at 15, if there are 15 or more pulses to be issued, and forward II drive is set, 15 is then deducted from the number of output pulses.

If a control interrupt occurs, it is first determined if it is an interrupt of a quick traverse motor. If so, then it is determined whether the number of output pulses is less than 14. If so, then that number of pulses is set into register 2261 by the switch 2271. If not, then 15 is deducted from the number of output pulses.

As described in detail above, according to the present invention an IC chip for an analog electronic watch can enable a variety of functions to be realised according to the software loaded in a program memory. Further, the software can be developed within one third to one half of the period in which a random logic IC chip for realising the same function can be developed, thus shortening considerably the period in which the IC chip is developed. Then, if there arise changes in specifications, additions of function and other changes during development, the software can easily be modified accordingly, thus realising an IC chip for an analog electronic watch which is capable of satisfying diverse consumers' needs.

Claims

1. An IC chip for an analog electronic watch, comprising a core CPU (201), a program memory (202) for storing software for actuating the core CPU, a plurality of motor drivers (213, 214, 215, 216), and a motor drive controlling circuit (212) for selectively supplying the motor drivers with predetermined driving signals according to commands of the software.

2. An IC chip as claimed in claim 1, in which the motor drive controlling circuit (212) has a plurality of motor clock controlling circuits (226, 227, 228, 229) each for controlling the number of driving pulses to be applied to a step motor (A, B, C, D).

3. An IC chip as claimed in claim 1 or 2, wherein the motor drive controlling circuit (212) has a drive reference signal forming circuit (220) for forming a drive reference clock signal (Cdrv) to act as a trigger for step motor drive, the drive reference signal forming circuit (220) selecting the frequency of the drive reference clock signals according to commands of the software.

4. An IC chip as claimed in claim 1, 2 or 3, in which the motor drive controlling circuit (212) includes a plurality of drive pulse forming circuits (221, 222, 223, 224, 225) for generating different waveforms of motor driving pulse and a motor drive system controlling circuit (219) for determining which waveform of driving pulse is to be selected for a step motor according to commands of the software.

5. An IC chip as claimed in claim 4, including a plurality of motor drive selection circuits (234, 235, 236, 237) responsive to the outputs of the drive pulse forming circuits (221, 222, 223, 224, 225) and of the motor drive system controlling circuit (219) to supply pulses (PA, PB, PC, PD) to the respective motor drivers (213, 214, 215, 216).

6. An analog electronic watch comprising an IC chip (20) as claimed in claim 1 or 2 or 3 or 4 or 5, a plurality of step motors (A, B, C, D) and at least one gear train mechanism to couple each step motor to a rotatable indicator hand.

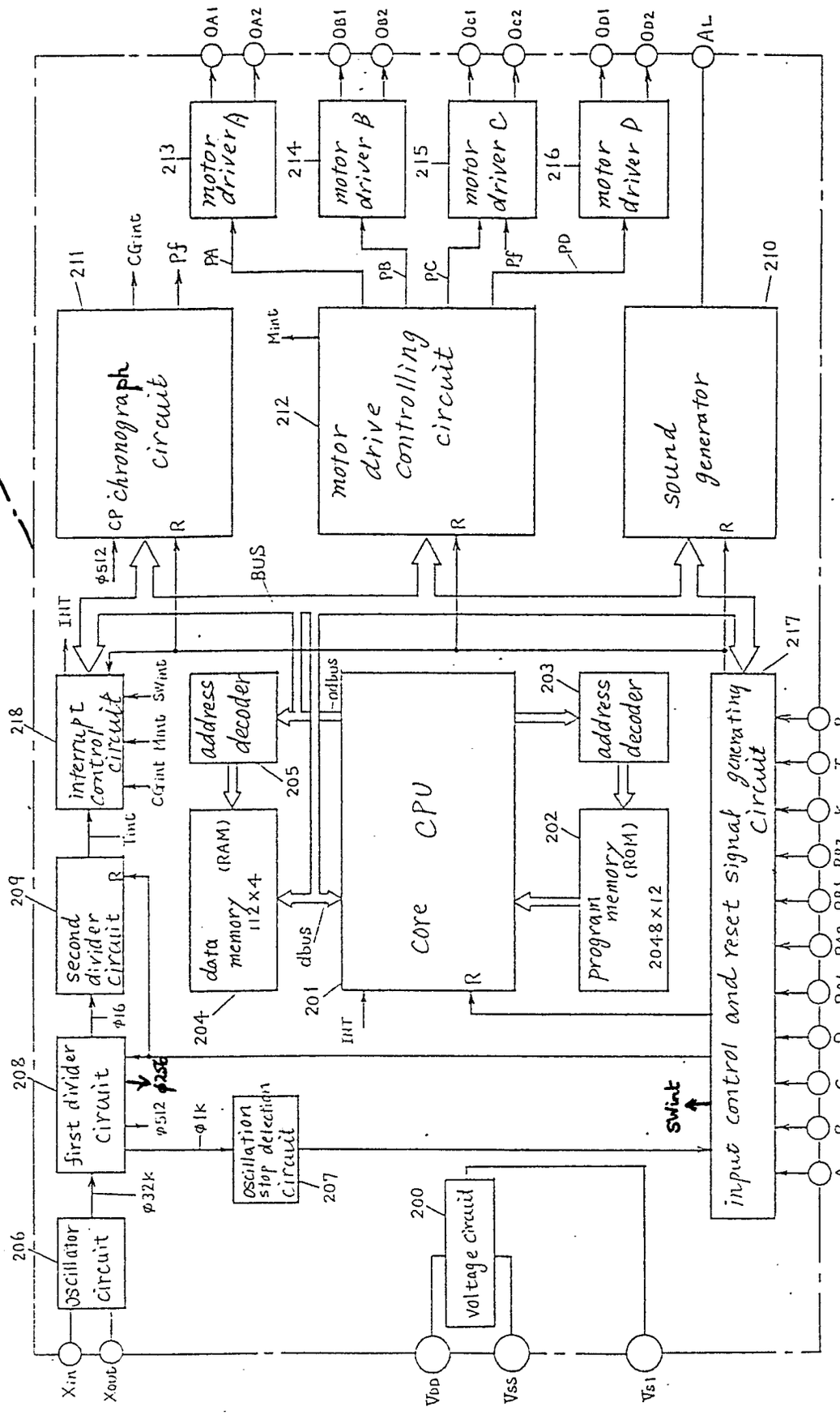

20
OA1
OA2
OB1
OB2
OC1
OC2
OD1
OD2
AL
motor driver A
motor driver B
motor driver C
motor driver D
213
214
215
216
211
CGint
PF
PA
PB
PC
PD
Mint
212
210
CP chronograph circuit
motor drive controlling circuit
sound generator
R
φ512
BUS
INT
218
interrupt control circuit
CGint Mint Swint
Tint
209
second divider circuit
φ16
208
first divider circuit
φ32K
φ512
φ1K
φ256
oscillation stop detection circuit
207
206
oscillator circuit
Xin
Xout
200
voltage circuit
VDD
VSS
VSI
address decoder
205
data memory (RAM) 112×4
204
dbus
-dbus
core CPU
201
INT
203
address decoder
202
program memory (ROM) 2048×12
217
input control and reset signal generating circuit
Swint
A
B
C
D
RA1
RA2
RB1
RB2
K
T
R

FIG 1

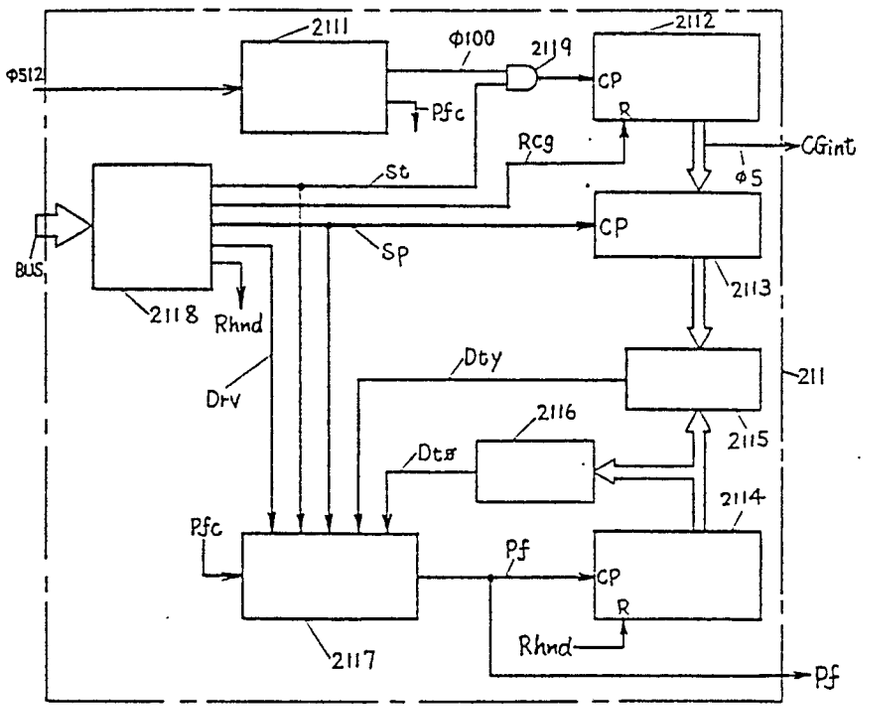

2111
φ100
2119
2112
φ512
CP
R
Pfc
Rcg
CGint
St
φ5
CP
BUS
Sp
2113
2118
Rhnd
Dty
211
Drv
2116
2115
Dtx
2114
Pfc
Pf
CP
R
Rhnd
2117
Pf

FIG2

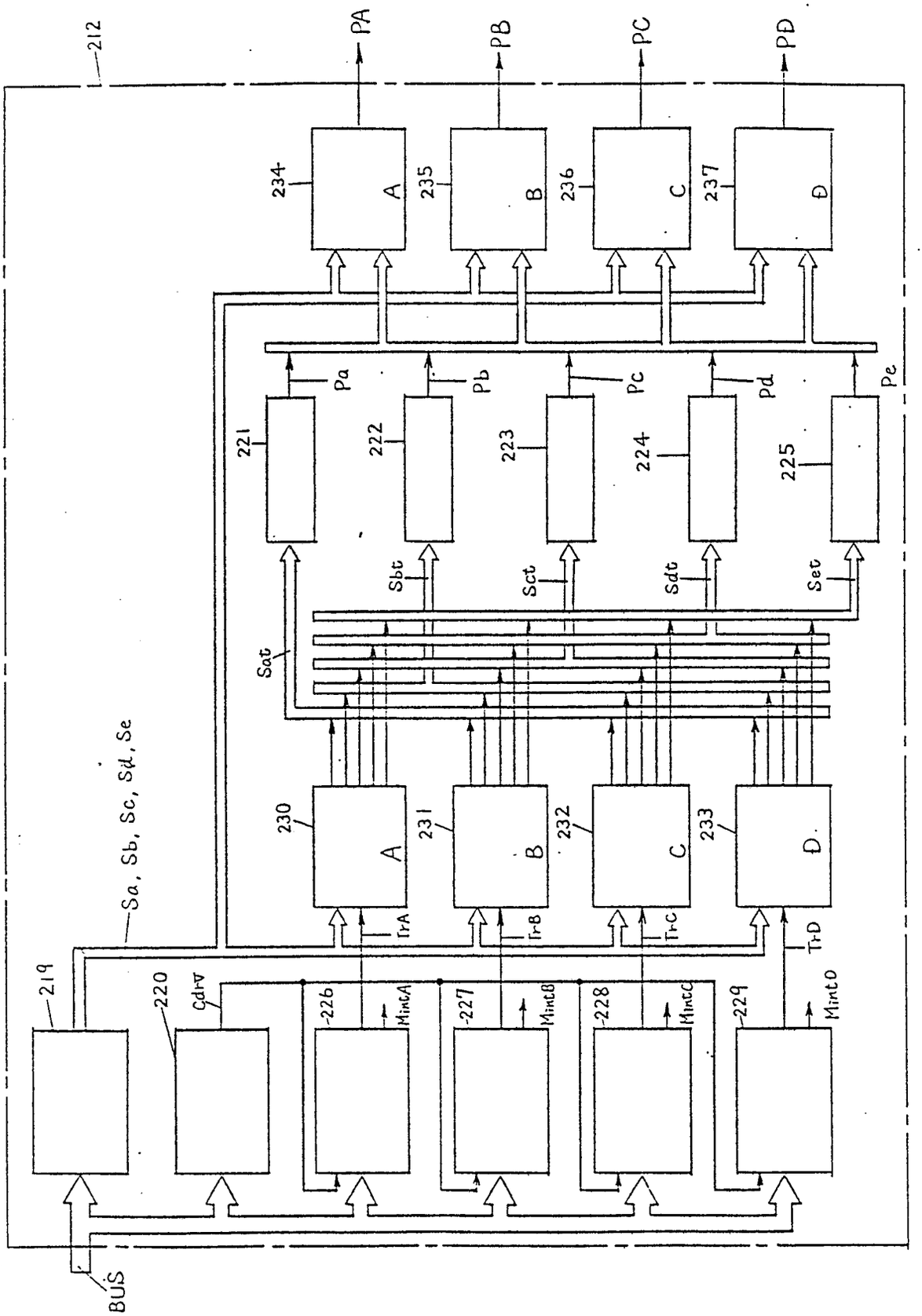

212
PA
PB
PC
PD
234
235
236
237
A
B
C
D
Pa
Pb
Pc
Pd
Pe
221
222
223
224
225
Sbt
Sct
Sdt
Set
Sat
Sa, Sb, Sc, Sd, Se
230
231
232
233
TrA
TrB
TrC
TrD
219
220
CdrV
226
227
228
229
MintA
MintB
MintC
MintD
BUS

FIG 3

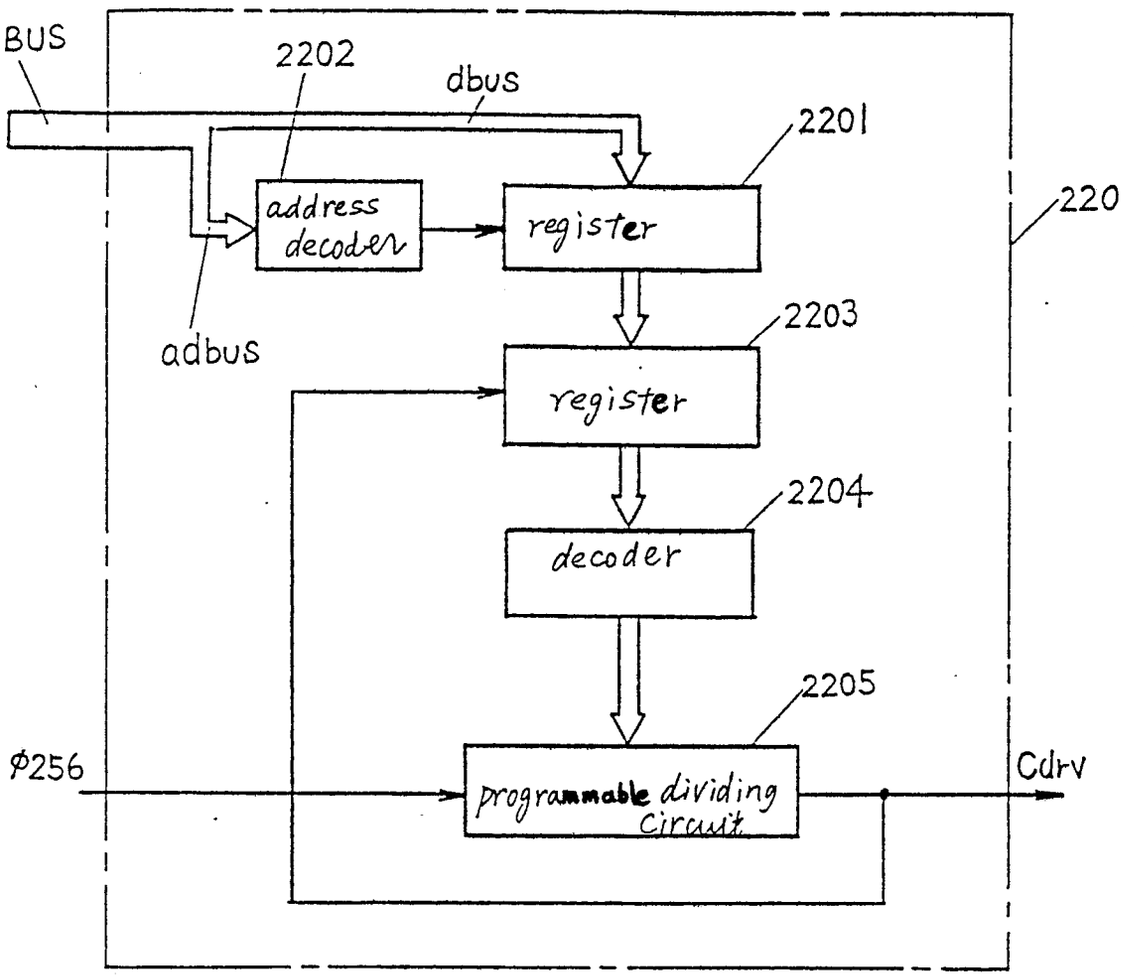

BUS
2202
dbus
2201
220
address decoder
register
adbus
2203
register
2204
decoder
2205
φ256
programmable dividing circuit
Cdrv

FIG4

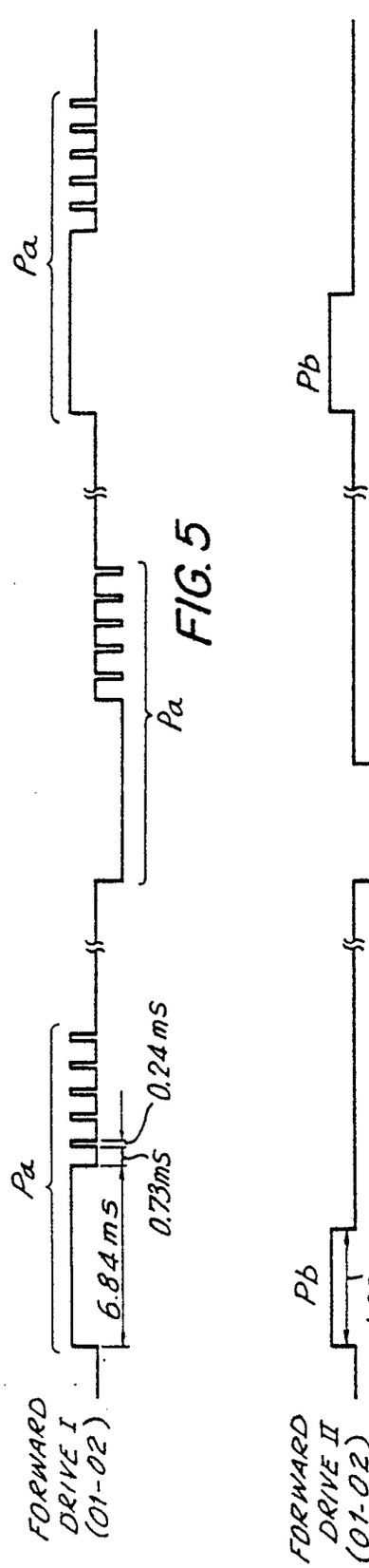


FIG. 5

FIG. 6

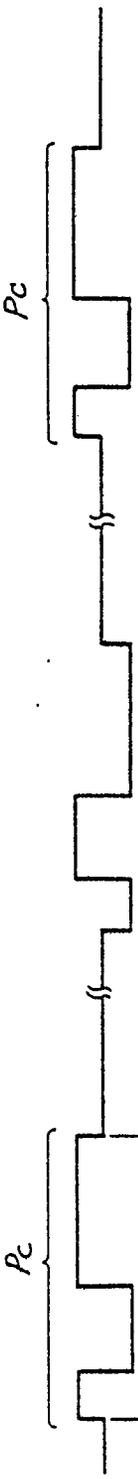


FIG. 7

FIG. 8

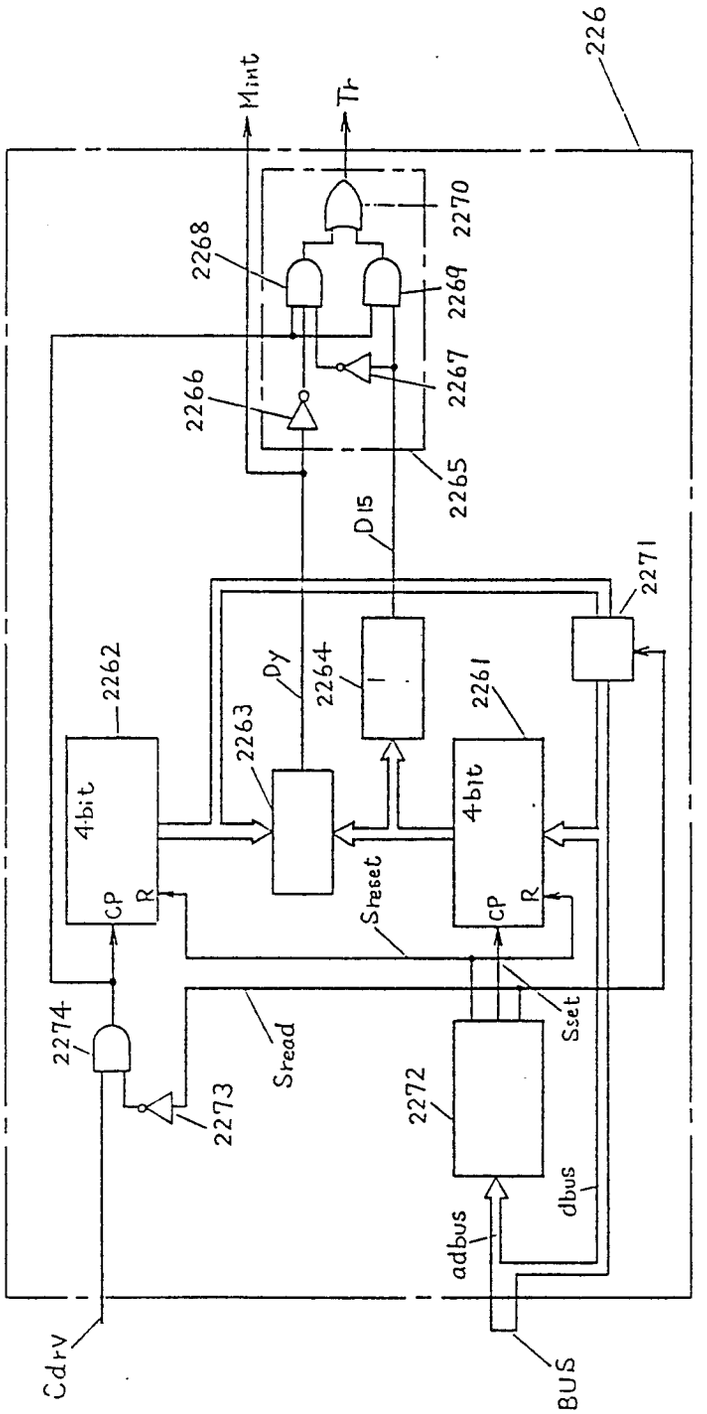

226
Mint
Tr
2270
2268
2269
2267
2266
2265
DIS
2271
2262
Dy
2264
2263
2261
4bit
CP
R
Sreset
Sread
Sset
2274
2273
2272
dbus
adbus
Cdrv
BUS

FIG 9

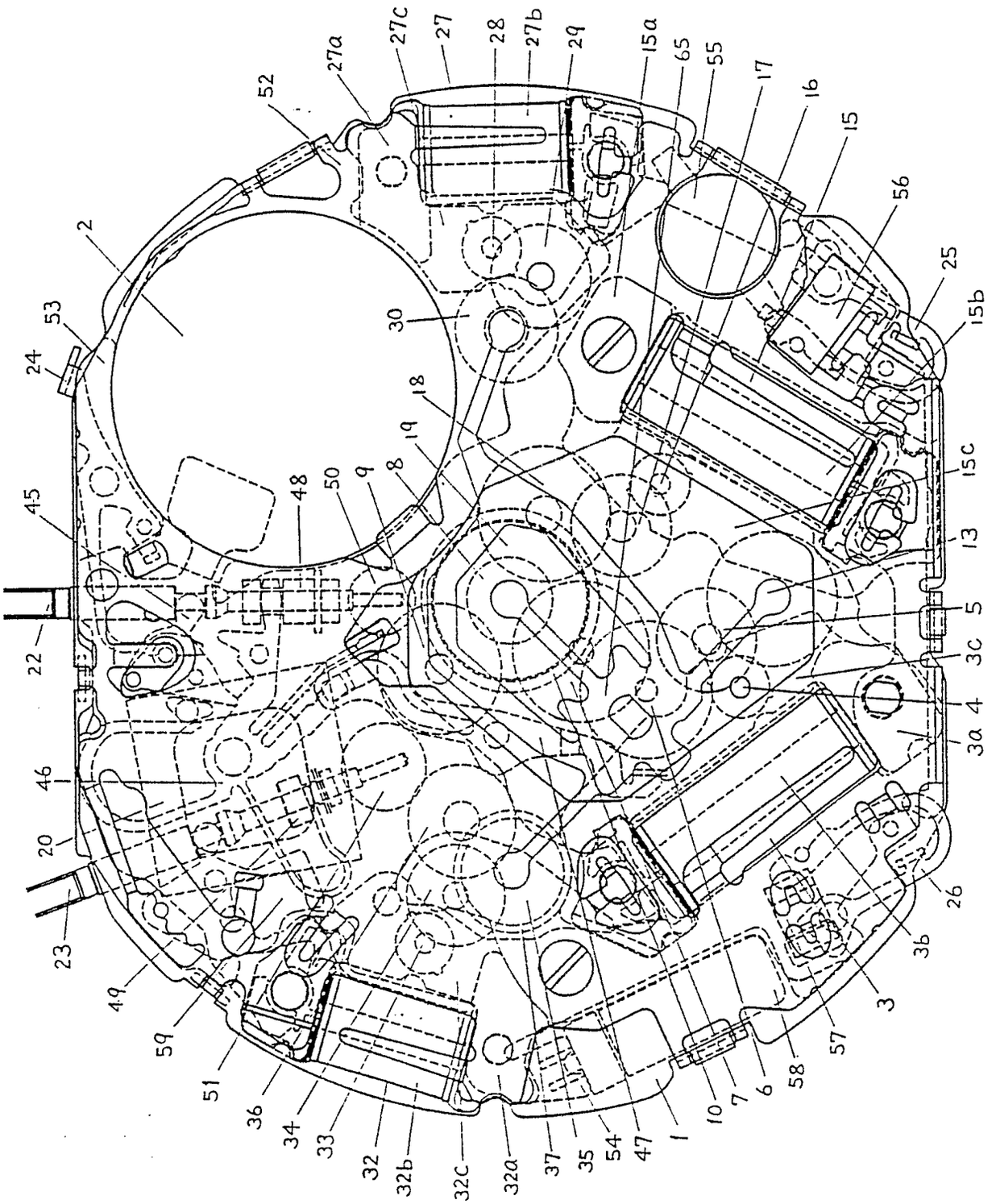

52
27a
27c
27
28
27b
29
15a
65
55
17
16
15
56
25
15b
2
53
24
30
18
19
9
8
48
50
45
15c
13
5
3c
4
3a
22
46
20
23
49
59
51
36
34
33
32
32b
32c
32a
37
35
54
47
1
10
7
6
58
57
3
36
26

FIG 10

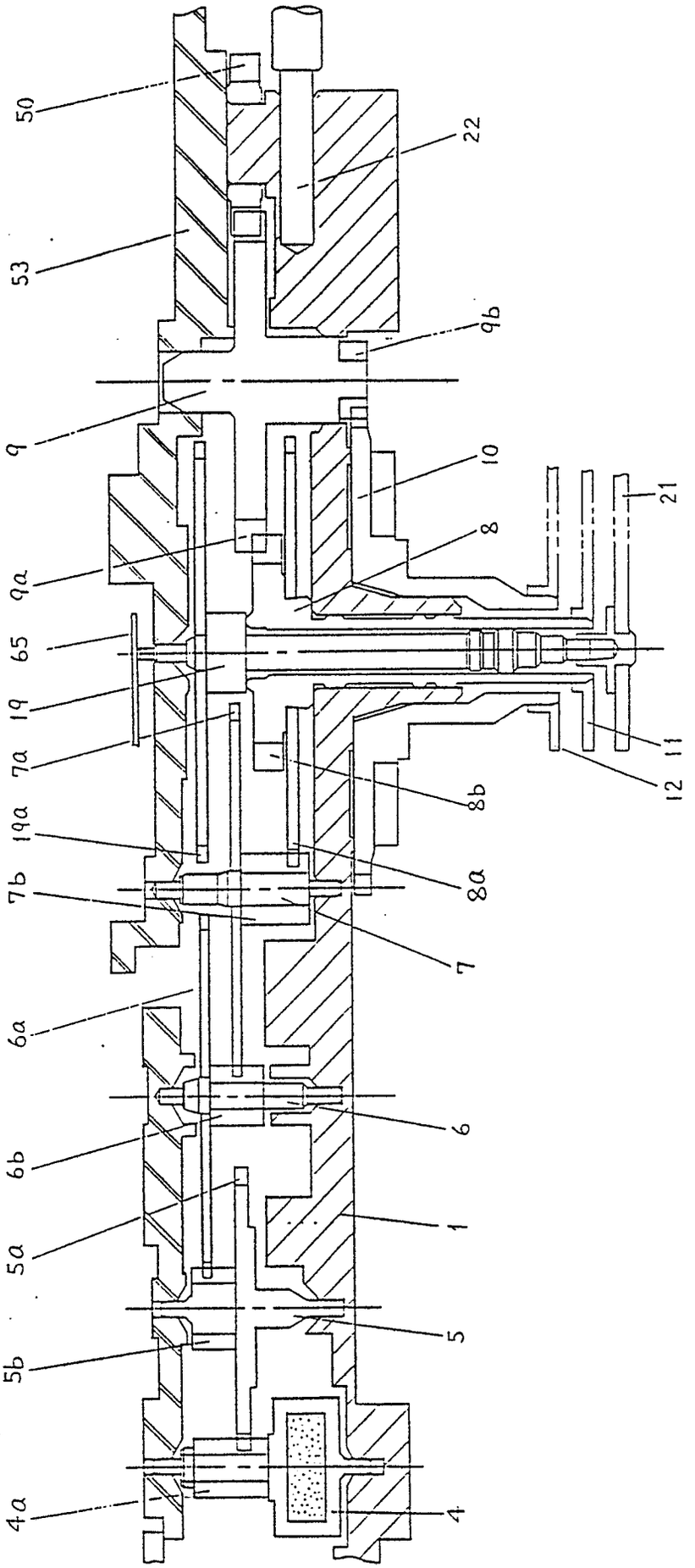

50
22
53
9b
9
10
21
8
9a
65
19
7a
11
12
8b
19a
8a
7b
7
6a
6
6b
1
5a
5
5b
4a
4

FIG 11

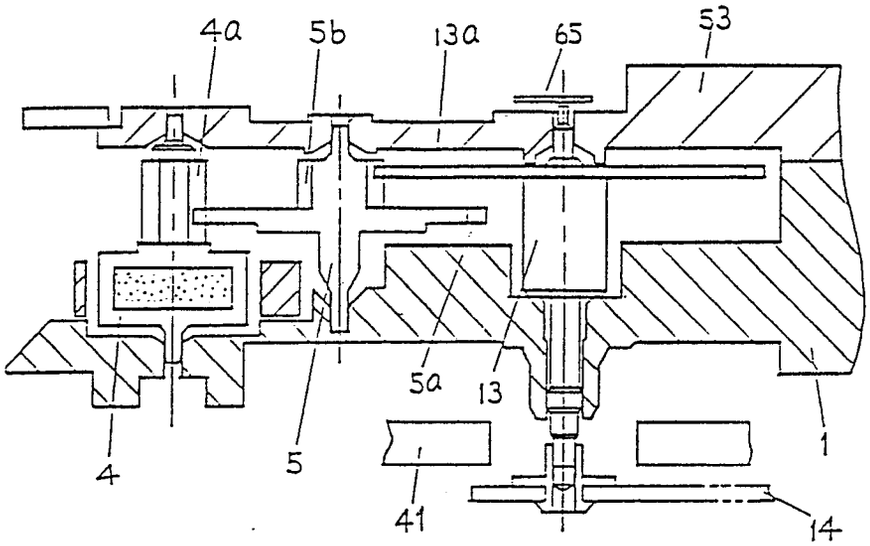

4a
5b
13a
65
53
5a
13
4
5
41
1
14

FIG12

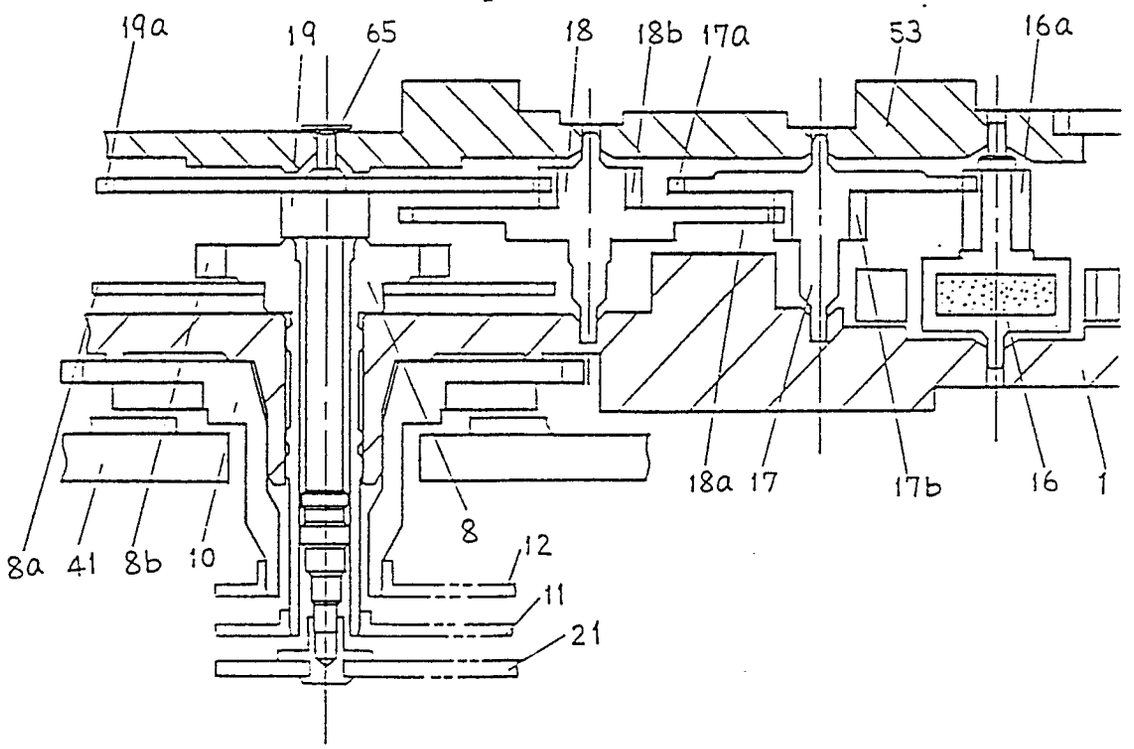
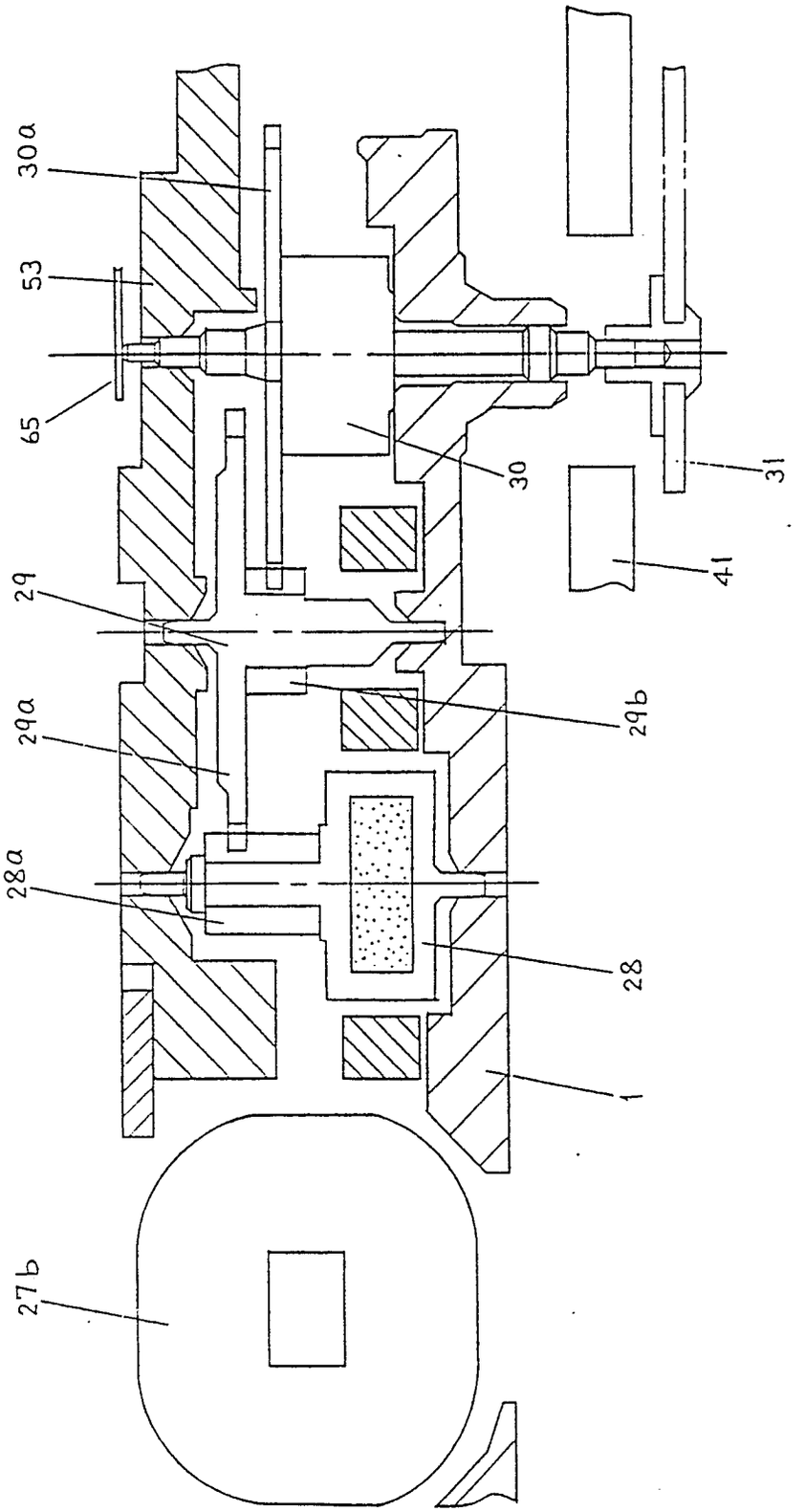

19a
19
65
18
18b
17a
53
16a
18a
17
17b
16
1
8a
41
8b
10
8
12
11
21

FIG13


30a
53
65
30
31
41
29
29b
29a
28a
28
1
27b

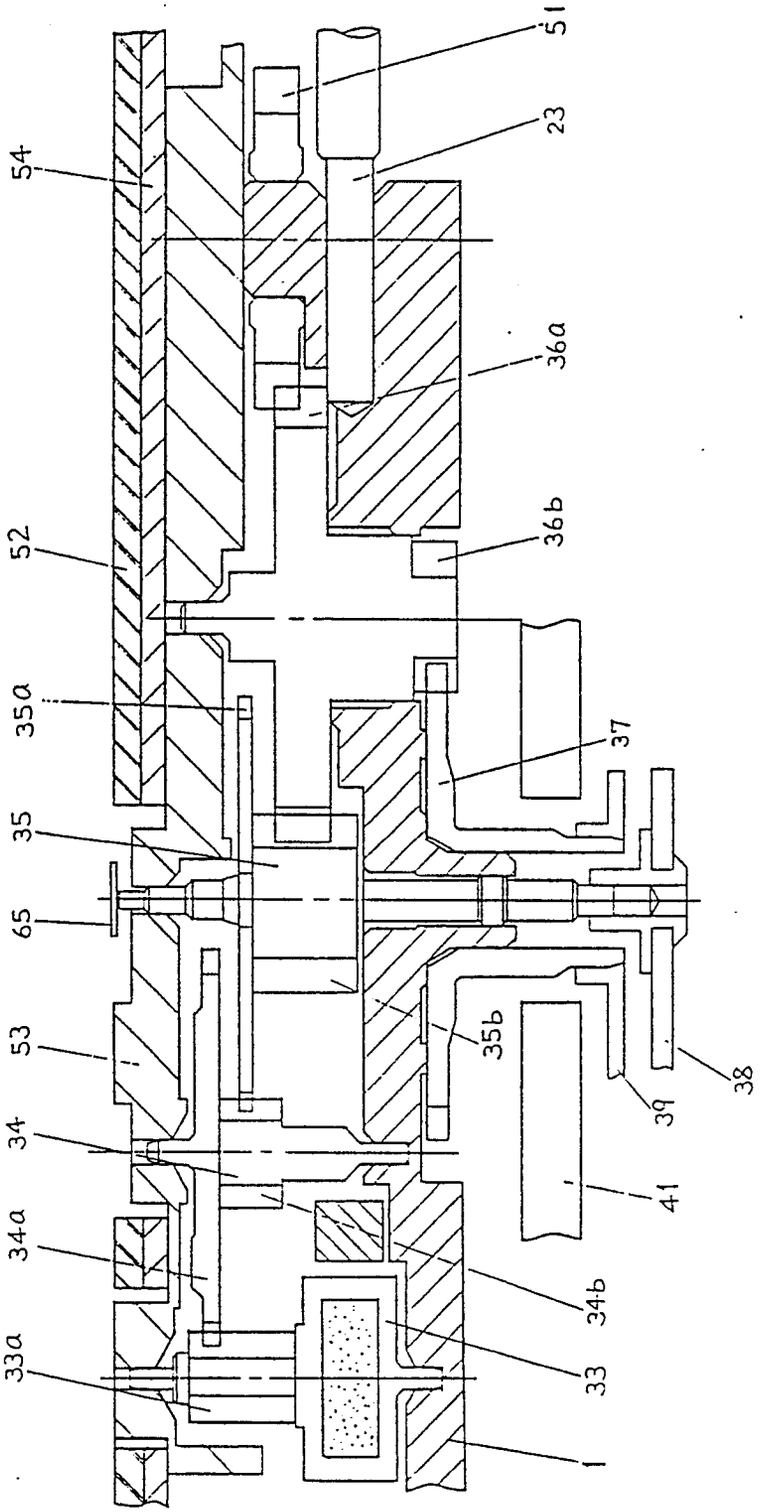


FIG 15

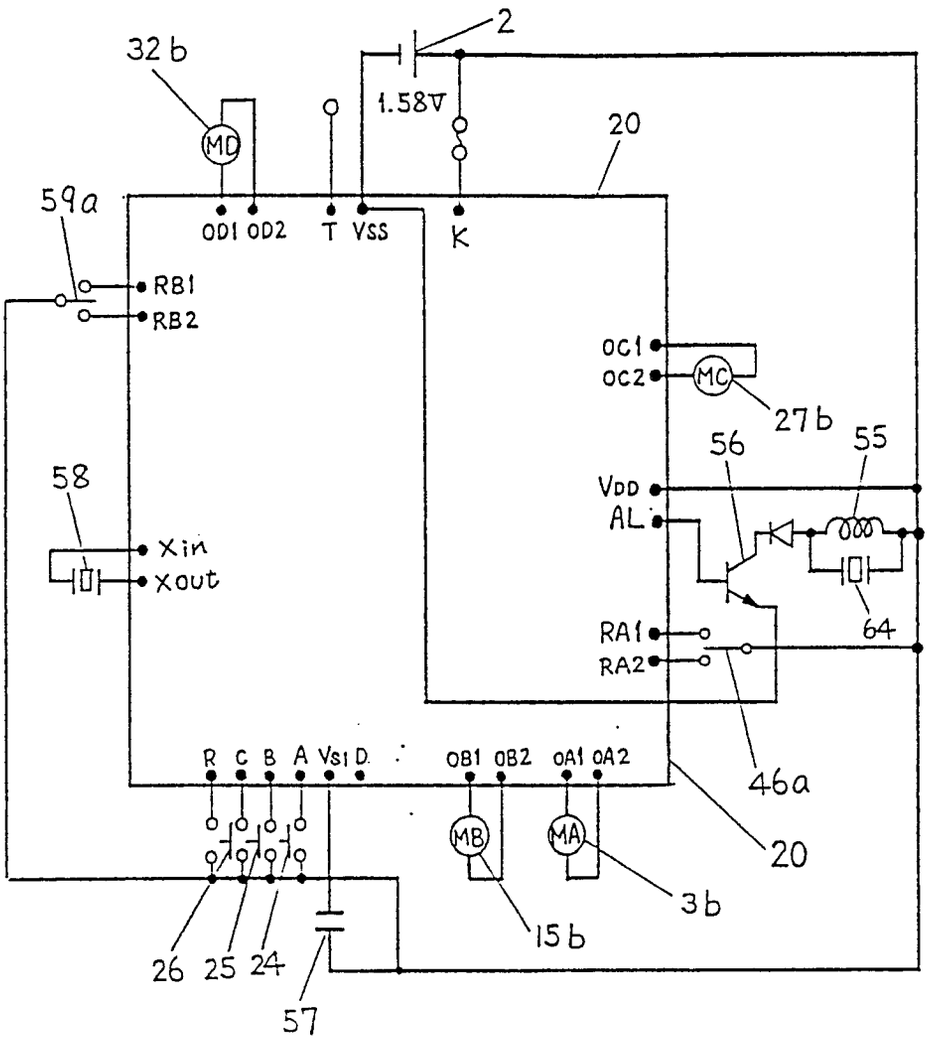

32b
2
1.58V
20
MD
59a
OD1 OD2
T
VSS
K
RB1
RB2
OC1
OC2
MC
27b
56
55
58
VDD
AL
Xin
Xout
64
RA1
RA2
R C B A Vs1 D
OB1 OB2 OA1 OA2
46a
20
MB
MA
3b
15b
26 25 24
57

FIG 16

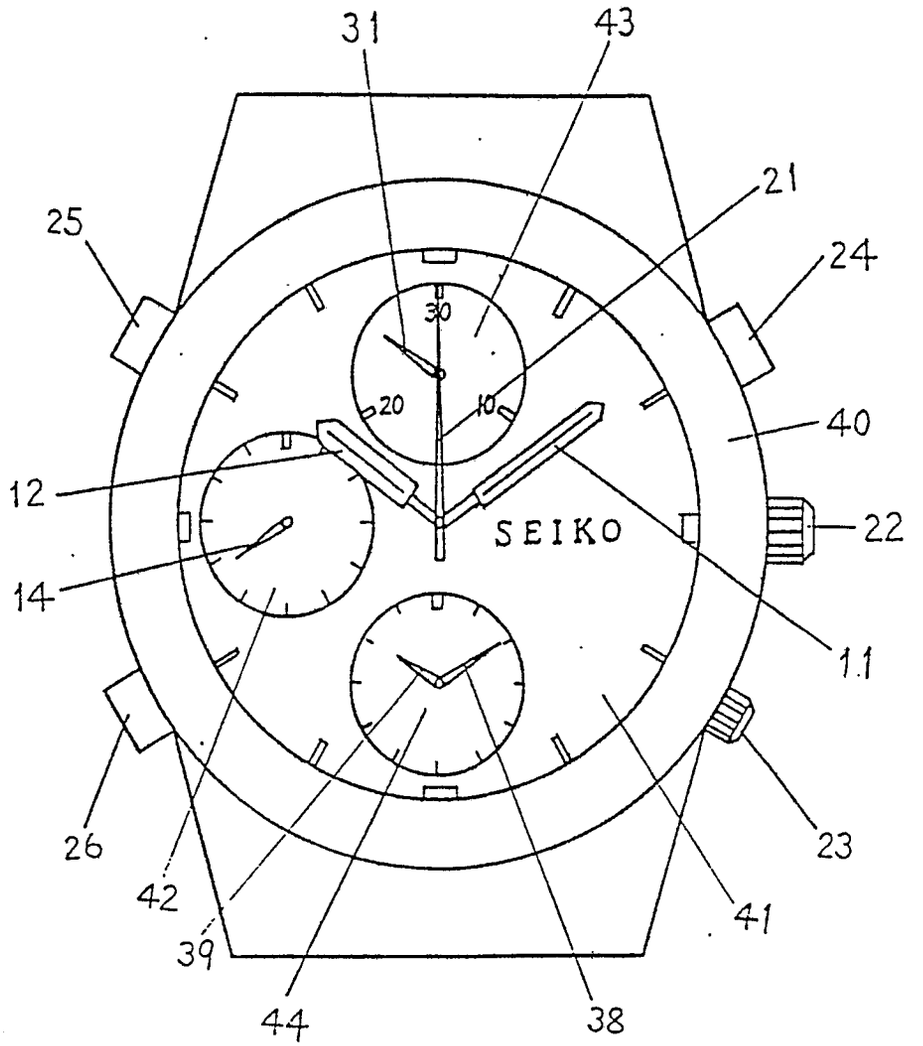


FIG 17

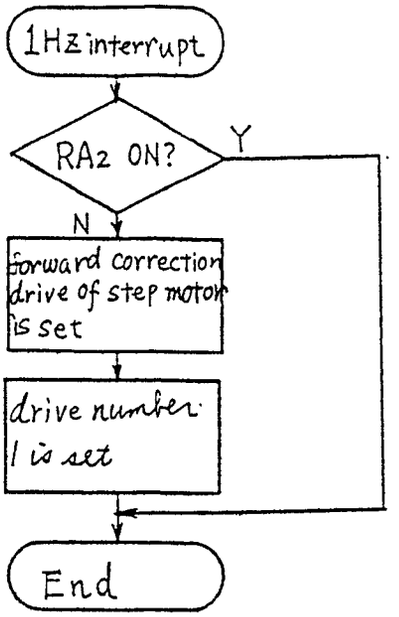


FIG 18 (b)

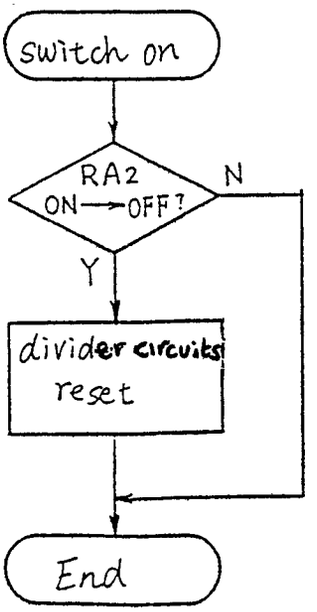
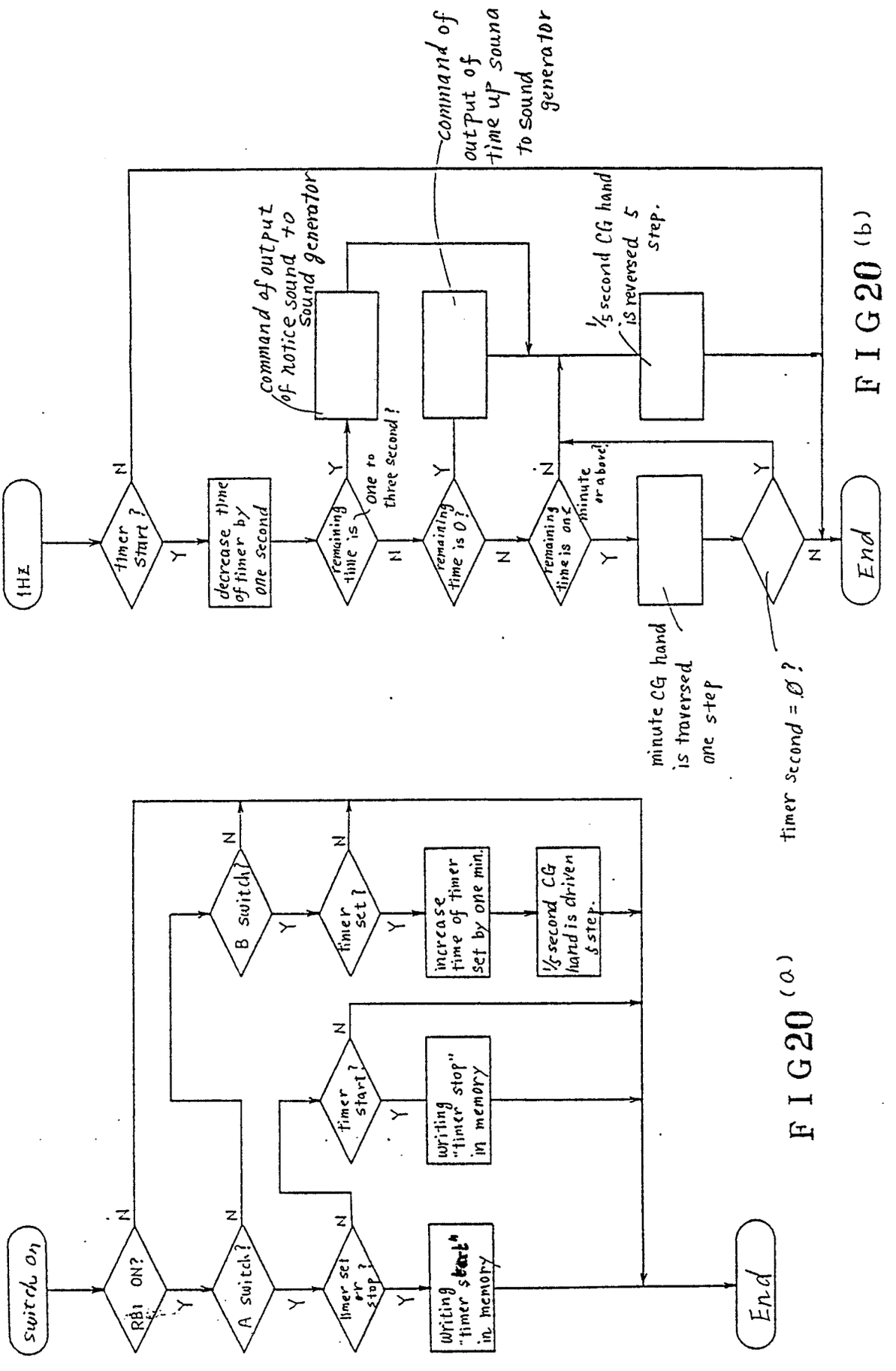


FIG 18 (a)


Switch on
RB1 ON?
A switch?
timer set or stop?
Writing "timer start" in memory
End
B switch?
timer set?
increase time of timer set by one min.
1/5 second CG hand is driven 1 step.
timer start?
writing "timer stop" in memory
FIG 20 (a)
1HZ
timer start?
decrease time of timer by one second
remaining time is one to three second?
command of notice sound to Sound generator
remaining time is 0?
command of output of time up sound to sound generator
remaining time is one minute or above?
1/5 second CG hand is reversed 5 step.
minute CG hand is traversed one step
timer second = 0?
End
FIG 20 (b)

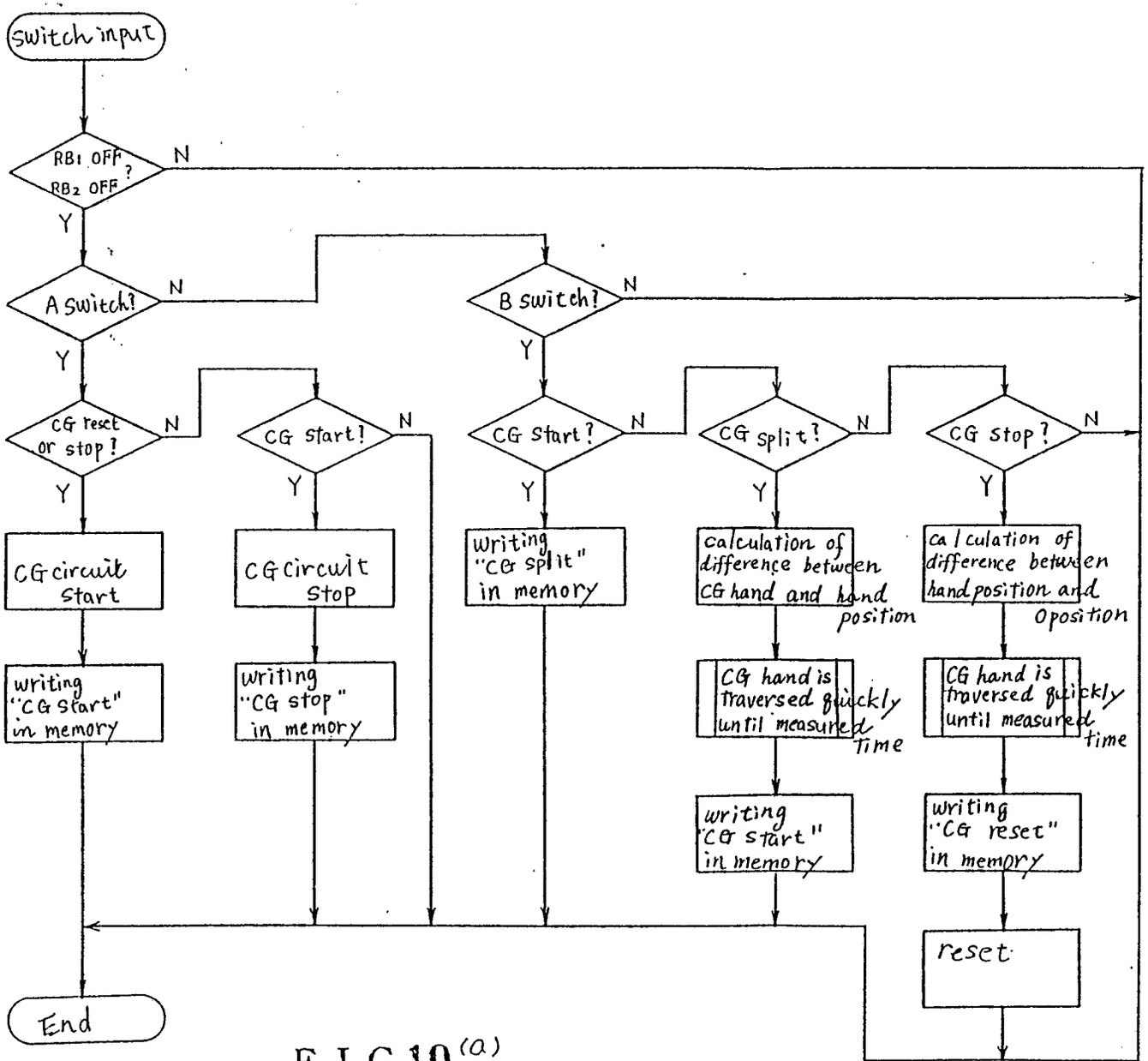


FIG19(a)

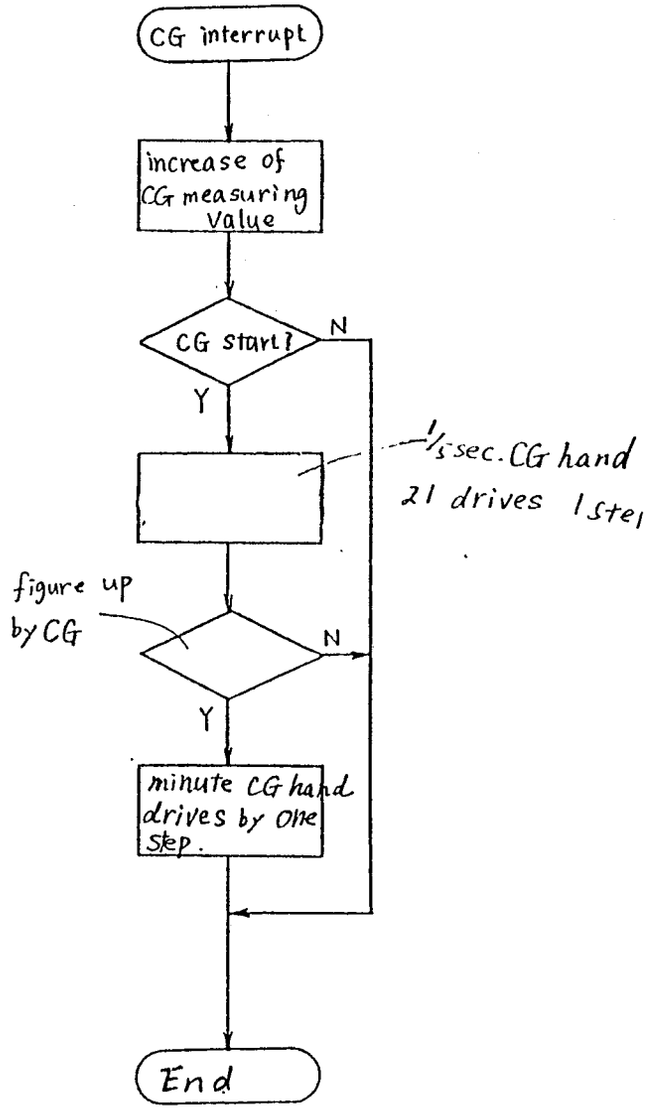


FIG19(b)

EP 0 347 249 A2

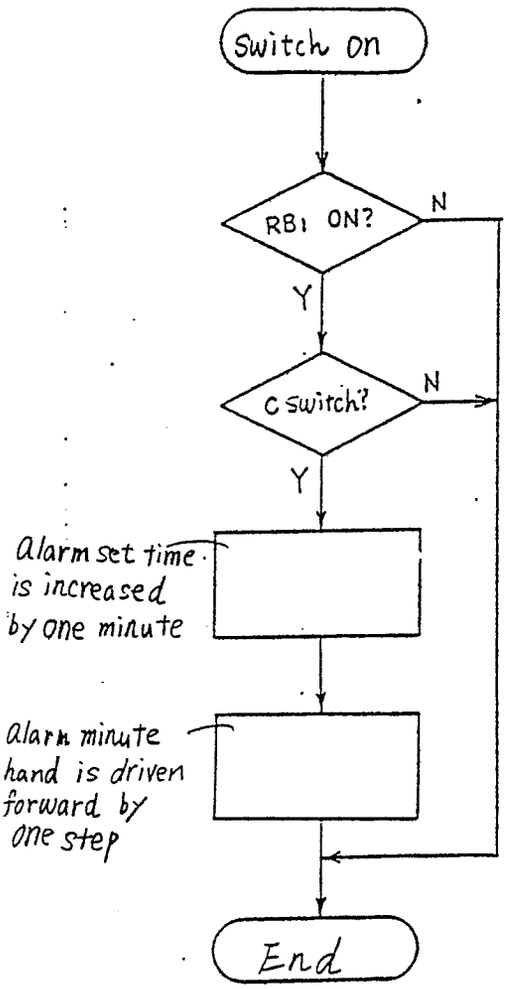


Fig. 21 (a)

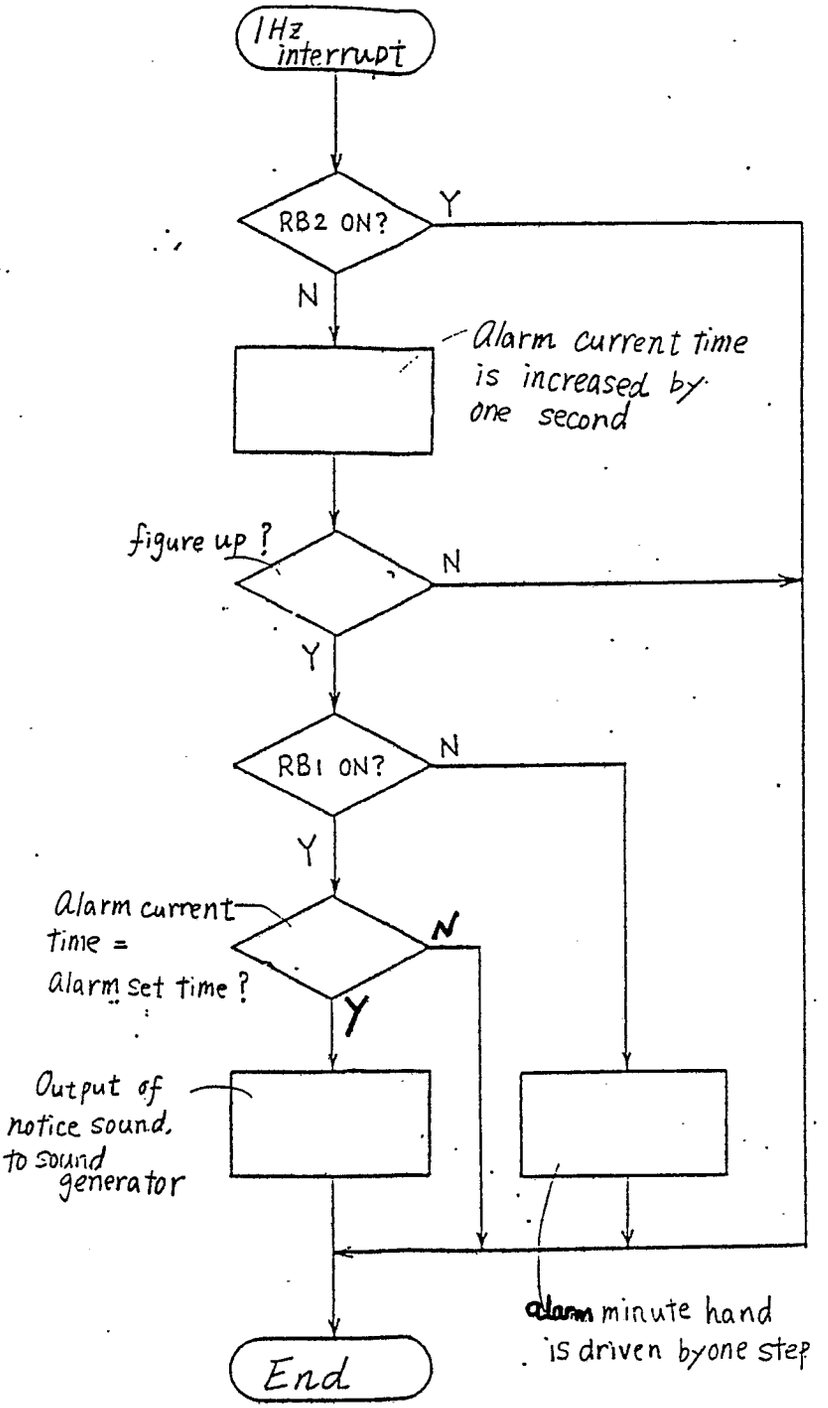


Fig. 21 (b)

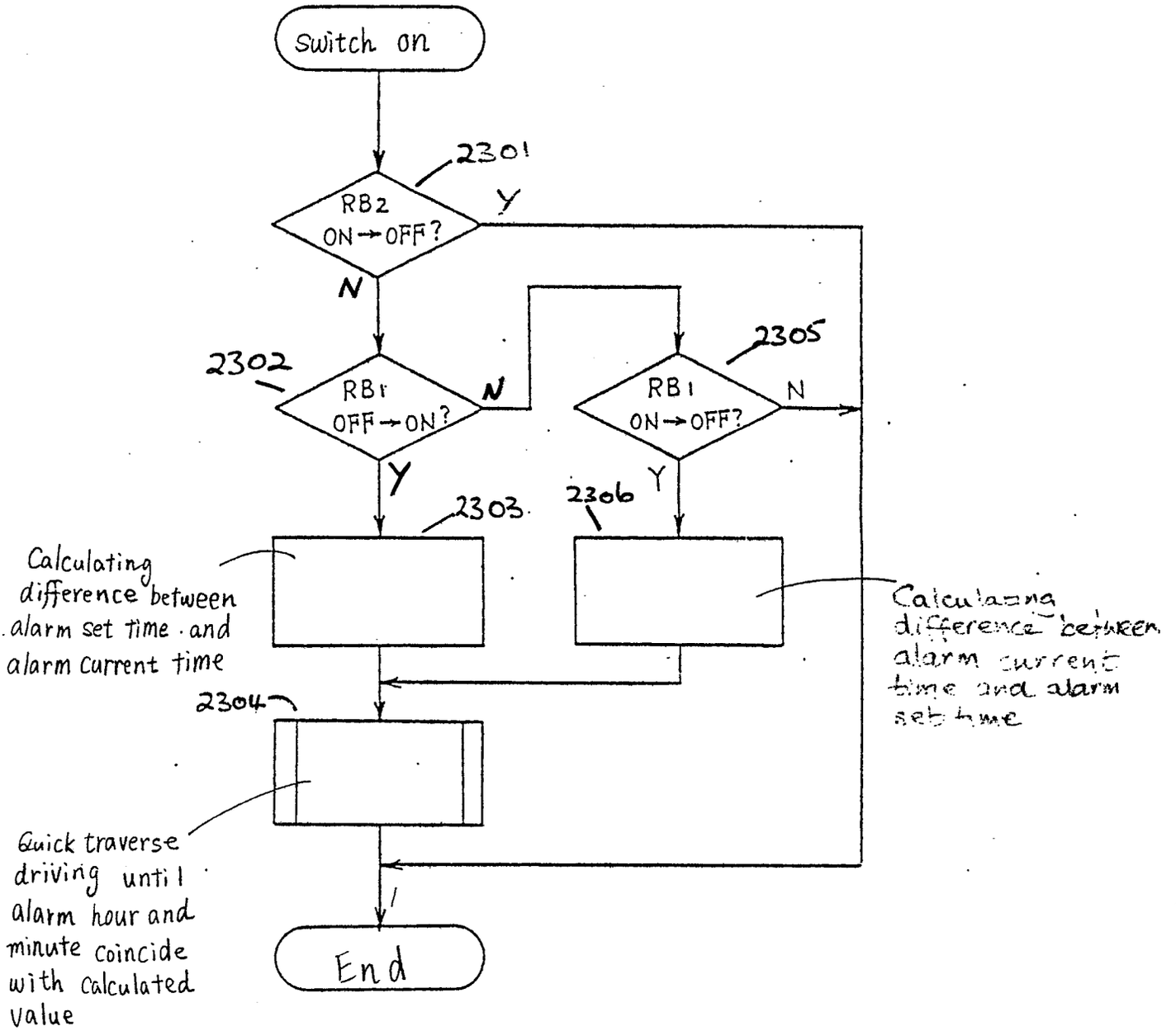

Switch on
2301
RB2 ON→OFF?
Y
N
2302
RB1 OFF→ON?
N
Y
2305
RB1 ON→OFF?
N
Y
2303
2306
Calculating difference between alarm set time and alarm current time
Calculating difference between alarm current time and alarm set time
2304
Quick traverse driving until alarm hour and minute coincide with calculated value
End

Fig. 21 (C)

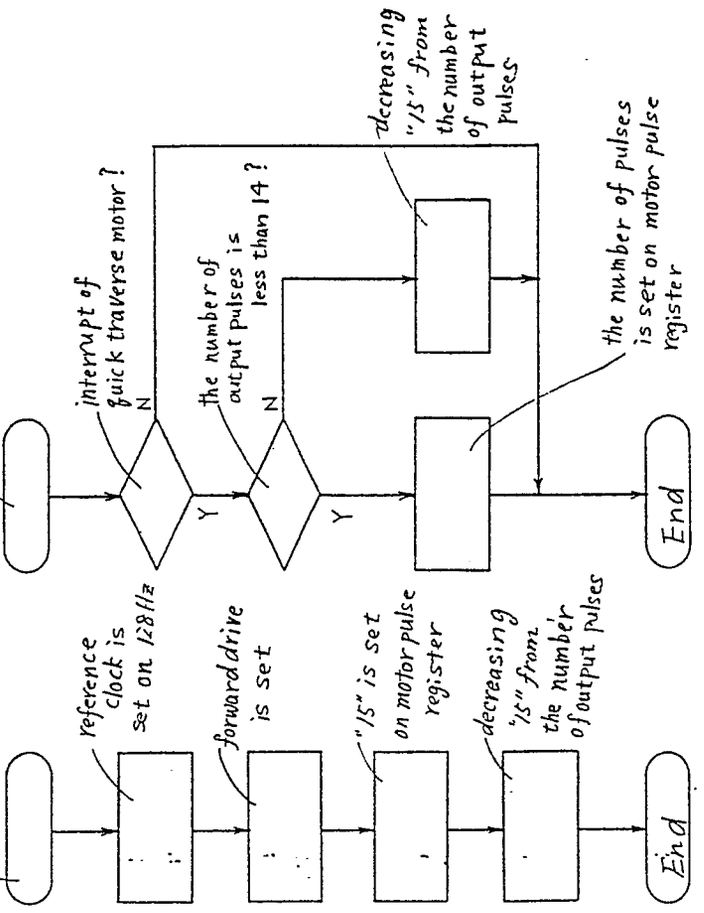


FIG22(b)

FIG22(c)

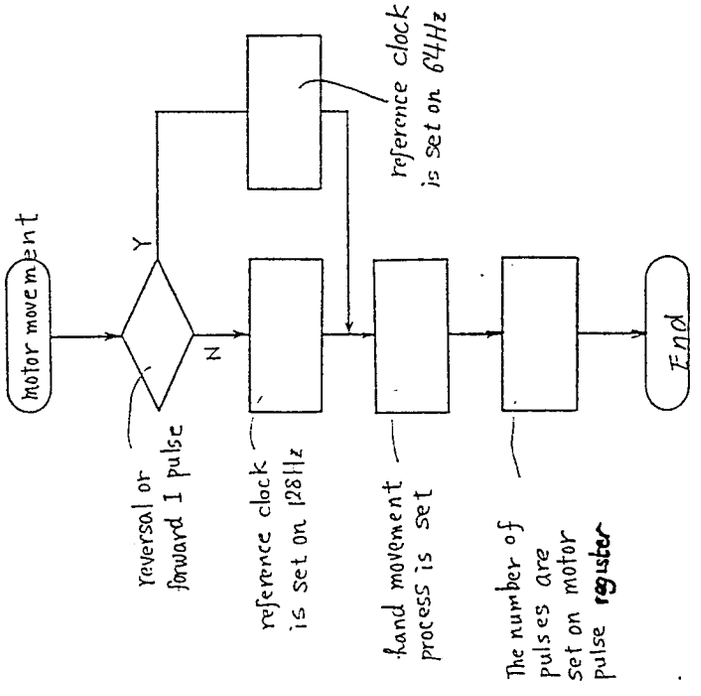


FIG22(a)