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Description

This invention relates to semiconductor memories and to methods of manufacturing such memories.

A dynamic random access memory (DRAM) comprising storage cells each comprising a combination of a data storage capacitor and an access transistor is very suitable for use in integrated circuits, and is employed in various forms of electronic apparatus.

As is described in "Trend of 4M and 16M DRAMs; Multilayer Capacitor and Trench Capacitor", Monthly Semiconductor World, Feb. 1988, pages 31 to 36, DRAMs are classified broadly into those of a multilayer capacitor type employing multilayer capacitors formed on a semiconductor substrate, and those of a trench capacitor type employing trench capacitors formed on a semiconductor substrate. Most suitable at present for high-density integration is a static RAM of a trench capacitor type comprising trench capacitors formed in trenches in a semiconductor substrate, and access transistors formed directly above the trench capacitors. The construction of such a static RAM is illustrated in a sectional view on page 36 of the foregoing Monthly Semiconductor World.

Efforts have been made to develop a method of fabricating a very large scale integrated circuit (VLSI) incorporating the foregoing semiconductor memories, by using a so-called silicon-on-insulator (SOI) substrate formed by forming a thin single crystal silicon film over an insulating body. A SOI substrate can have good crystallinity and other characteristics.

In fabricating a SOI substrate using a process shown in Figures 16A, 16B and 16C, it is required to lap a silicon wafer 101, after applying a silicon wafer 105 to the silicon wafer 101, so as to finish the surfaces of insular silicon layers 106 formed in recesses defined by a SiO₂ film, flat and flush with the surfaces 103a of the SiO₂ film 103 surrounding the insular silicon layers 106, and without damage. Various lapping methods have been proposed for such a purpose.

Figure 17 shows a lapping apparatus for such selective lapping. A laminated wafer 108 formed by laminating the silicon wafers 101 and 105 as shown in Figure 16B is attached to a wafer holder 109, for example, with a wax. An abrasive disc 112 is formed by applying an abrasive pad 111 to the surface of a lapping disc 110. The abrasive disc 112 is rotated, and a lapping liquid 114 is supplied to the surface of the abrasive pad 111, with the surface of the laminated wafer 108 to be lapped in contact with the abrasive pad 111. The lapping liquid 114 is an alkaline solution or an alkaline solution containing abrasive grains, which reacts on silicon and does not react on SiO₂. The abrasive pad 111 is a very hard disc 116 as shown in Figure 18, such as a ceramic disc or a carbide disc, or a suede-finished soft urethane form cloth 117 as shown in Figure 19.

JP provisional patent publication (Kokai) no 62/259769 discloses a lapping method for finishing the surface of a silicon wafer to a high flatness, which employs a polyurethane abrasive cloth and an amine solution as a lapping liquid for lapping. There is, however, no reference to selective lapping for finishing a flat surface including both an insulating material and silicon.

In a static RAM of a trench capacitor type comprising storage cells each comprising a trench capacitor and an access transistor formed directly above the trench capacitor, the n type source-drain region (a region on the side of the capacitor) of a metal-insulator-semiconductor (MIS) access transistor is formed in a p⁺-type layer formed on a p⁺-type semiconductor substrate by epitaxial growth. Therefore, it is possible that a depletion layer extending from an n type region into a p type epitaxial layer of a storage cell encounters a depletion layer extending from the n type source-drain region (a region on the same side as the capacitor) of the adjacent storage cell when such storage cells are formed at a high density. Accordingly, this static RAM has an electrical disadvantage that current leakage increases, even although the static RAM can be made very small, and hence it is impossible to arrange the storage cells with a sufficiently high density.

Furthermore, since most semiconductor memories are of a bulk silicon metal-oxide-semiconductor (MOS) type, it is difficult to reduce the parasitic capacitance across the bit line and the substrate. Accordingly, the open-bit construction, although excellent in integration capability, is inferior in noise resistance, and hence the open-bit construction is subject to limitation in the density of integration. The semiconductor memory of a trench capacitor type is inevitably susceptible to soft errors, and has a disadvantage that an optional bias voltage, for example, 0.5V_{cc}, cannot be applied to the plate.

Patent application EP-A-0 220 410 discloses a semiconductor memory comprising a semiconductor substrate, an insulating layer formed on the substrate and having an aperture therethrough, a semiconductor region formed in each aperture and providing a source-drain region of a respective transistor, a further insulating layer formed beneath each transistor, and a capacitor for each transistor, each capacitor comprising a first electrode formed in a respective recess in the substrate beneath the further insulating layer for the respective transistor and connected electrically to the transistor through a respective contact hole formed in the further insulating layer, and a dielectric layer separating the first electrode from the substrate whereby the substrate forms the second electrode of the capacitor.

EP-A-0 220 410 also discloses a method of making such a memory, in which: trenches are formed in a substrate; dielectric layers are deposited on the walls of the trenches; the first electrodes are deposited in the trenches; the second insulating layers are grown at the top of the first electrodes; a silicon layer is grown; the contact holes are formed through the silicon layer and second insulating layer and filled with polysilicon; the first insulating layer is formed around the site for each transistor; and the transistors are formed in the silicon layer.

In accordance with one aspect of the present invention there is provided a semiconductor memory comprising: a semiconductor substrate; a polycrystalline silicon layer formed on the substrate; an insulating layer formed on the polycrystalline layer opposite the substrate, the surface of the insulating layer opposite the polycrystalline layer being formed with a plurality of recesses; a semiconductor region formed in each of the recesses and providing a source-drain region of a respective MIS transistor; and at least one capacitor being provided for each MIS transistor, each capacitor comprising: a first electrode formed in a respective recess in the polycrystalline layer beneath the respective MIS transistor and connected electrically thereto through a respective contact hole formed in the insulating layer; and a dielectric layer separating the first electrode from the polycrystalline layer whereby the substrate and polycrystalline layer form the second electrode of the capacitor.

Accordingly, the same silicon layer serves to form in part the MIS transistors, to separate the MIS transistors from each other; to reduce current leakage between the storage cells; and to reduce the capacitance across the bit lines formed on the side of the MIS transistors and the semiconductor substrate. Accordingly, the semiconductor memory is resistant to noise and hence can be formed in an open bit construction having excellent integrating characteristics. Thus, a semiconductor memory can be formed with a high degree of integration.

The insulating layer formed over the surface of the semiconductor substrate on which the capacitors are formed intercepts alpha rays, and hence the semiconductor memory is highly resistant to soft errors.

Furthermore, since the semiconductor substrate is independent and is connected electrically to none of the rest of the components of the semiconductor memory, the semiconductor substrate can be set at an optional bias potential, for example, half V_{cc} , which permits reduction of the voltage applied to the dielectric film.

Still further, a semiconductor memory can be formed with a high degree of integration, because the capacitors are formed under the access MIS transistors.

According to another aspect of the present invention there is provided a method of manufacturing a semiconductor memory, the method comprising the steps of: selectively removing portions of the surface of a first semiconductor substrate to form recesses and semiconductor lands on which MIS transistors are to be formed; forming an insulating layer over the surface of the first semiconductor substrate; forming respective contact holes through the insulating layer so as to reach the surfaces of the lands of the first semiconductor substrate; forming respective electrode layers on the insulating layer and in the contact holes so as to connect with the surfaces of the lands of the first semiconductor substrate through the contact holes; coating the electrode layers with respective dielectric layers; forming a semiconductor layer over the insulating layer so as to cover the electrode layers coated with the dielectric layers and so that the electrode layers, dielectric layers and semiconductor layer form a plurality of capacitors; attaching a second semiconductor substrate to the semiconductor layer after flattening the contact surface of the semiconductor layer; removing the first semiconductor substrate leaving the lands thereof surrounded by the insulating layer as semiconductor regions; and forming the MIS transistors on the lands of the first semiconductor substrate remaining as the semiconductor regions so that the MIS transistors are electrically connected to the capacitors through the contact holes.

Preferably, the first semiconductor substrate is removed leaving the lands thereof surrounded by the insulating layer as semiconductor regions by a lapping process which employs an alkaline liquid as a lapping liquid, and the ratio of lapping rate for lapping portions of the first semiconductor substrate other than those forming the lands to the lapping rate for lapping the portions of the first semiconductor substrate forming the lands is not less than twenty.

In lapping the semiconductor layer, the alkaline solution and the semiconductor layer interact to form a film of a reaction product for reactive lapping. The film of reaction product is wiped off mechanically by the hard pad. The formation of a film of the reaction product and its removal are repeated alternately to lap the semiconductor layer. The alkaline solution does not react with the insulating layer. Since the lapping rate ratio is preferably not less than twenty, and the insulating layer is not lapped by reactive lapping, only the portions of the semiconductor layer remaining on the portions of the insulating layer other than those forming the recesses are lapped positively in the final stage of the lapping process, so that insular semiconductor layers having surfaces flush with the surface of the insulating layer are formed in the recesses.

Furthermore, since only the alkaline solution is used as a lapping liquid and the hard pad of a hardness in the range of 75 to 95 is used for lapping, the insular semiconductor layers are finished flush with the surface

of the insulating layer without being damaged.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

- Figure 1 is a sectional view of a semiconductor memory in a preferred embodiment of the present invention;
- 5 Figures 2A to 2K are sectional views sequentially showing the steps of a method of manufacturing a semiconductor memory embodying the present invention;
- Figure 3 is an illustration for explaining a lapping process;
- Figures 4A and 4B are illustrations for explaining a selective lapping process;
- Figure 5 is a graph showing the variation of lapping rate with lapping pressure;
- 10 Figure 6 is a graph showing the variation of lapping rate with lapping liquid supply rate;
- Figure 7 is a schematic front elevation of a lapping machine;
- Figures 8 and 9 are schematic side elevations of laminating jigs, respectively, for laminating wafers;
- Figure 10 is a plan view of a further laminating jig;
- Figure 11 is contour map for explaining the state of laminated wafers;
- 15 Figure 12 is an illustration for explaining a grinding operation;
- Figure 13 is a graph showing the relation between surface roughness and bubble forming percentage;
- Figure 14 is a sectional view for explaining a gettering process;
- Figure 15 is sectional view of a SOI substrate employed in manufacturing a semiconductor memory in another embodiment according to the present invention;
- 20 Figures 16A to 16C are sectional views for explaining a previously proposed process of fabricating a SOI substrate;
- Figure 17 is a schematic front elevation of a previously proposed lapping machine for selective lapping;
- Figure 18 is a sectional view of a previously proposed lapping disc in lapping operation;
- Figure 19 is a sectional view of another previously proposed lapping disc; and
- 25 Figure 20 is a sectional view for explaining the lapping action of the lapping disc of Figure 19.

A semiconductor memory in a preferred embodiment of the present invention will now be described with reference to Figures 1 and 2A to 2k.

- Referring to Figure 1, there are shown a semiconductor substrate (silicon substrate) 1, a polycrystalline silicon layer 2 formed on the substrate 1, an insulating layer (SiO₂ layer) 3 formed over the surface of the polycrystalline silicon layer 2, recesses 4 (only one of them is shown) formed in the surface of the insulating layer 3 in a predetermined pattern by selectively removing portions of the insulating layer 3, and semiconductor regions (silicon regions) 5 (only one of them is shown) formed in the recesses 4. The substrate 1, the polycrystalline silicon layer 2, the insulating layer 3 and the semiconductor regions 5 form a SOI structure.
- 30 Access MIS transistors having source-drain regions 6 and 7 are formed in each semiconductor region 5. The source-drain region 6 is connected to a bit line, and the source-drain regions 7 are connected to capacitors. Contact holes 8 are formed through the insulating layer 3 and filled with polycrystalline silicon layers 9. Polycrystalline silicon layers 10 are formed under the source-drain regions 7 formed in the surface of the polycrystalline silicon layer 2, and are respectively connected through the polycrystalline silicon layers 9 to the source-drain regions 7.

- Dielectric films 11, such as SiO₂ films, are formed between the polycrystalline silicon layers 10 and the polycrystalline silicon layer 2. Each dielectric film 11 may be a SiO₂/SiN/SiO₂ structure (ONO structure). The substrate 1, the polycrystalline silicon layer 2, the dielectric films 11 and the polycrystalline silicon layers 10 form capacitors for information storage. The substrate 1 and the polycrystalline silicon layer 2 serve as first electrodes of the semiconductor memory, and the polycrystalline silicon layers 10 serve as second electrodes thereof. The polycrystalline silicon layers 10 serving as the second electrodes are connected electrically through the polycrystalline silicon layers 9 filling the contact holes 8, to the source-drain regions 7 of the MIS transistors.
- 40 Also shown in Figure 1 are oxide films 12 for the gates of the MIS transistors, gate electrodes 13 formed, for example, of polycrystalline silicon or polycide, a layer insulating film 14, a contact hole 15 for a bit line formed in the layer insulating film 14, and a bit line 16 formed of aluminium or polycide, and connected through the contact hole 15 to the source-drain region 6.
- 50 Since the storage cells of the semiconductor memory thus constructed are separated by the insulating layer 3, current leakage between the storage cells, which occurs in the previously proposed DRAMs of trench capacitor type, does not occur.

- The SOI structure substantially reduces the capacitance between the bit line 16 and the substrate 1, which enhances the noise resistance, and enables the employment of the open bit construction which enables the construction of a semiconductor memory with a high degree of integration.
- 55 Furthermore, forming the capacitors on the side of the semiconductor substrate of SOI construction, and

shielding the capacitors from alpha rays by the insulating layer, enhances the resistance to soft errors.

Still further, since the substrate 1 and the polycrystalline silicon layer 2 of the semiconductor memory are isolated electrically from the rest of the components, an optional bias voltage can be applied to the substrate 1 and to the polycrystalline silicon layer 2. Accordingly, the voltage applied to the dielectric films 11 is reduced by half to improve the signal-to-noise (S/N) ration, and the reliability of the dielectric films 11, by applying half of a supply voltage V_{cc} to the substrate 1 as a plate voltage.

Moreover, forming the capacitors of the semiconductor memory under the access MIS transistors enables high-density integration of the storage cells, and hence the present invention has the potential of forming 16M-bit or 64M-bit static RAMs.

A method of manufacturing a semiconductor memory embodying the present invention will now be described with reference to Figures 2A to 2K.

Step A: The surface of a first semiconductor substrate (silicon substrate) 17 is etched selectively to a depth of, for example, 0.1 mm to form lands 18 as shown in Figure 2A. The first semiconductor substrate 17 and the semiconductor substrate 1 shown in Figure 1 are separate semiconductor substrates. In the final stage of the semiconductor memory manufacturing process, portions of the first semiconductor substrate 17 other than those forming the lands 18 are removed, leaving only the lands 18 as semiconductor regions (Figure 1) in which MIS transistors are formed.

Step B: As shown in Figure 2B, an insulating layer 3, namely, a SiO_2 film, is formed over the surface of the first semiconductor substrate 17.

Step C: As shown in Figure 2C, the insulating layer 3 is etched selectively to form contact holes 8 reaching the surfaces of the lands 18 corresponding to the backs of the semiconductor regions 5, at positions in portions in which source-drain regions 7 are to be formed.

Step D: As shown in Figure 2D, the contact holes 8 are filled with polycrystalline silicon layers 9 respectively. In forming the polycrystalline silicon layers 9, polycrystalline silicon is deposited in the contact holes 8 by a chemical vapour deposition (CVD) process, and then the surface of the deposited polycrystalline silicon is etched to finish the surface of the polycrystalline silicon layers 9 flush with the surface of the insulating layer 3.

Step E: As shown in Figure 2E, polycrystalline silicon layers 10 for the second electrodes of capacitors are formed on the insulating layer 3 at positions corresponding to the surfaces of the polycrystalline silicon layers 9. The polycrystalline layers 10 are formed by photoetching a polycrystalline silicon film of several micrometres in thickness formed over the insulating layer 3.

Step F: As shown in Figure 2F, the surfaces of the polycrystalline silicon layers 10 are subjected to thermal oxidation to form dielectric films 11, namely, SiO_2 films. The dielectric films 11 may be three-layer $\text{SiO}_2/\text{SiN}/\text{SiO}_2$ films, which naturally must be formed by a CVD process.

Step G: A polycrystalline silicon layer 2 of a thickness sufficiently greater than that of the polycrystalline silicon layers 10, for example, a thickness in the range of 5 to 10 millimetres, is formed over the insulating layer 3, and then the surface 19 of the polycrystalline silicon layer 2 is finished with a flat surface by lapping as shown in Figure 2G.

Step H: As shown in Figure 2H, a second semiconductor substrate (silicon substrate) 1 is applied to the surface 19 of the polycrystalline silicon layer 2. Indicated at 20 is the back of the semiconductor substrate 17.

Step I: As shown in Figure 2I, the assembly of the semiconductor substrates 1 and 17 is turned over.

Step J: The back 20 of the first semiconductor substrate 17 is lapped until the surface of the insulating layer 3 is exposed to leave only the portions of the semiconductor substrate 17 forming the lands 18 as shown in Figure 2J. The lands 18 serve as the semiconductor regions 5.

Step K: Finally, as shown in Figure 2K, access MIS transistors are formed in the semiconductor regions 5 by a known process of forming a SOI transistor to complete a semiconductor memory as shown in Figure 1.

Step I will be described further with reference to Figures 4 to 12.

The respective surfaces of wafers 121 and 126 to be joined together are cleaned by a mixed cleaning liquid of ammonia and hydrogen peroxide, and the wafers 121 and 126 are then dried by a dryer. Then, the wafers 121 and 126 are made to adhere spontaneously to each other by hydrogen bonding, principally by the agency of hydroxyl groups in a clean atmosphere. The combination of the wafers 121 and 126 is heated in an oxygen or nitrogen atmosphere at 1100°C for two hours to increase the bonding strength of the interface 128 between the wafers 121 and 126 to a level corresponding to that of the bulk. An assembling jig 145 shown in Figure 8, or an assembling jig 149 shown in Figure 9, is used to affix the wafers 121 and 126 to each other. In affixing the wafers 121 and 126 to each other, the wafers 121 and 126 are placed in contact with each other, and then the wafers 121 and 126 are pressed at the respective corresponding central points towards each other. The assembling jig 145 shown in Figure 8 comprises a block having a V-shaped groove defined by inclined surfaces 141 and 142, and pressing rods 143 and 144 supported on the block for lateral sliding movement to press the

corresponding wafers 121 and 126 at the centres thereof. In affixing the wafers 121 and 126 to each other on the assembling jig 145, the wafers 121 and 126 are placed in the V-shaped groove so as to rest on the inclined surfaces 141 and 142, respectively, with the respective orientation flats thereof in contact with the bottom of the V-shaped groove, and then the wafers 121 and 126 are pressed towards each other with the presser rods 143 and 144. As the wafers 121 and 126 are pressed firmly to each other with the presser rods 143 and 144, the wafers 121 and 126 start joining from the central portions thereof and the joined area expands towards the peripheries thereof to form a laminated wafer 127.

The assembling jig 149 shown in Figure 9 comprises a block having an inclined surface 147 provided with a protrusion 146, and a bottom surface 148 extending perpendicularly to the inclined surface 147, a positioning pin 140 for positioning the wafers 121 and 126 relative to the protrusion 146, and a presser rod 150. In affixing the wafers 121 and 126 to each other to obtain a laminated wafer 127 by using the assembling jig 149, the wafers 121 and 126 are set against the inclined surface 147 as shown in Figure 9, and then the wafers 121 and 126 are pressed against the protrusion 146 with the presser rod 150 extended opposite to the protrusion 148. The assembling jig 149 is disposed slightly obliquely as shown in Figure 10 in affixing the wafers 121 and 126 to each other, so that the wafers 121 and 126 rest on both the bottom surface 148 and the positioning pin 140 for positioning relative to the protrusion 146. The assembling jig 145 of Figure 8 may be provided with such a positioning pin.

Then, the edges 121a and 126a of the laminated wafer 127 are ground. First, the edge 121a of the wafer 121 is deeply ground as shown in Figure 12 with a rough grinding stone, while a portion of the boundary surface of the wafer 126 near the edge 126a thereof is ground slightly. Then, the laminated wafer 127 is subjected to an etching process to remove the surface layer damaged by grinding from the ground surfaces and to remove strain. In grinding the wafer 121, the free major surface of the wafer 121 is ground in a circular arc. Ordinarily, the peripheral portion of the wafer has a cross section of the shape of a circular arc, the edge 121a of the wafer 121 separates from the other wafer 126 when the wafer 121 is deeply ground near to the boundary surface corresponding to the interface 128, and the very thin remaining portion 151 of the wafer 21 is liable to be broken. If the remaining portion 151 is broken, fragments of the remaining portion 151, that is, dust, reduces the yield of the semiconductor memory manufacturing process.

The foregoing grinding of the laminated wafer 127 eliminates the above problem.

Then, the thickness of the wafer 121 is reduced to a thickness of about 10 micrometres by precision lapping using a precision lapping machine.

The selective lapping in Step J employs a lapping disc 155 as shown in Figure 3. The lapping disc 155 is formed by applying a hard lapping pad 154, such as a polyester non-woven fabric impregnated with polyurethane, or a porous polyurethane sheet of a rubber hardness in the range of 75 to 95, to a rigid disc 110. Only an alkaline solution, such as an aqueous ethylenediamine solution or an aqueous potassium hydroxide solution, is used as a lapping liquid 156. In the lapping operation, the lapping disc 155 is pressed against the surface of the wafer 121 to be lapped at a pressure in the range of 50 to 250 g/cm², the lapping disc 155 is rotated at a circumferential speed in the range of 20 to 80 m/min, the lapping liquid 156 is supplied at a supply rate in the range of 5 to 180 cm³/min, and the wafer holder is rotated or reciprocated. Thus, a SOI substrate 153 having thin insular silicon layers 152 having a uniform thickness is obtained.

A selective lapping process shown in Figures 4A and 4B effects the lapping operation in conformity to the above lapping conditions by using the lapping disc 155 provided with the hard pad 154. Accordingly, the lapping rate ratio, namely, the ratio of lapping rate for lapping portions of the semiconductor layer corresponding to portions of the insulating layer 123 (SiO₂ layer) other than those forming the recesses, to lapping rate for lapping portions of the semiconductor layers corresponding to portions of the insulating layer 123 forming the recesses, is not less than fifty (Figure 4B), and hence, after a portion of the insulating layer 123 formed on the wafer 121 has been exposed as shown in Figure 4A, the lapping rate for a semiconductor layer 121B formed in the recess in the exposed portion of the insulating layer 123 drops suddenly, and then the semiconductor layer 121A remaining over the insulating layer 123 is removed completely by lapping while the exposed semiconductor layer 121B in the recess is lapped slightly. Thus, the surfaces of insular semiconductor layers 152 formed in the recesses are finished flush with the surface of the insulating layer 123 as shown in Figure 4B.

Figure 5 is a graph showing the variation of lapping rate for lapping portions of the semiconductor layer corresponding to portions of the insulating layer 123 other than those forming the recesses with pressure applied to the lapping disc 155, and the variation of lapping rate for lapping portions of the semiconductor layer corresponding to portions of the insulating layer forming the recesses with pressure applied to the lapping disc 155. Figure 6 is a graph showing the variation of lapping rate for lapping portions of the semiconductor layer corresponding to portions of the insulating layer 123 other than those forming the recesses with lapping liquid supply rate, and the variation of lapping rate for lapping portions of the semiconductor layer corresponding to portions of the insulating layer 123 forming the recesses with lapping liquid supply rate.

As is evident from Figures 5 and 6, the lapping rate ratio is large and stable, so lapping can be achieved when the pressure applied to the lapping disc 155 is in the range of 50 to 250 g/cm², and the lapping liquid supply rate is in the range of 5 to 180 cm³/min.

The mechanism of the selective lapping in the semiconductor memory manufacturing method of the present invention will now be explained.

The lapping liquid, such as an aqueous amine solution, does not react on the SiO₂ layer (insulating layer) and reacts on the silicon layer (semiconductor layer) to form a film of a reaction product. If the film of the reaction product is not removed, the lapping action is stopped. In the selective lapping, the film of the reaction product is removed continuously by the hard pad 154 to continue lapping the silicon layer. As the lapping operation is continued, the surface of the silicon layer sinks to a level below a plane including the surface of the SiO₂ layer. Consequently, the film of the reaction product formed over the silicon layer is no longer removed, and hence the lapping of the silicon layer substantially stops when the surface of the silicon layer sinks to a level coinciding with the plane including the surface of the SiO₂ layer, and the surface of the silicon layer is finished flat and flush with that of the SiO₂ layer. Thus, in the selective lapping process, the lapping rate ratio increases sharply after the surface of the portion of the semiconductor layer corresponding to the portion of the insulating layer forming the recess has coincided with the plane including the surface of the insulating layer, so that the thin insular semiconductor layers 152 having excellent flatness are finished in a uniform thickness with their surfaces flush with the surface of the insulating layer and without any damage therein.

Since the lapping rate ratio is large, all the portions of the silicon layer corresponding to the portions of the SiO₂ layer other than those of the same forming the recesses are removed before the SiO₂ layer serving as a lapping stopper is abraded. The lapping rate for lapping the silicon wafer 121 is not less than 0.05 micrometres m/min and hence the SOI substrate 153 can be produced at a high production rate. Since the lapping liquid is inexpensive and the lapping process does not use any abrasive grains, the silicon wafer 121 can be lapped at a reduced cost.

When the wafer 121 was lapped with the lapping disc 155 provided with the hard pad 154 using an aqueous ethylenediamine solution containing abrasive grains, the insular silicon layers 121B formed in the recesses formed in the SiO₂ layer and the SiO₂ serving as a lapping stopper were abraded by the abrasive grains to deteriorate the flatness of the surface of the insular silicon layers 121B. Accordingly, it is most desirable to lap the silicon wafer 121 using only an aqueous ethylenediamine solution or an aqueous potassium hydroxide.

Table 1

	Embodiment			Prior method		
	Ceramic disc	Soft pad	Hard pad	Ceramic disc	Soft pad	Hard pad
Lapping rate	High	Low	High	High	High	High
Abrasion of SiO ₂	Abraded	No	No	Abraded	Abraded	Abraded
Damage to SiO ₂	Damaged	No	No	Damaged	No	No
Flatness	Good	Bad	Good	Good	Bad	Bad
Lapping solution	Diamine solution			Diamine solution + Abrasive		

Results of lapping operations by a lapping process according to the embodiment and those of lapping op-

erations by a previously proposed lapping process are tabulated in Table 1.

The selective lapping process is able to lap the silicon layer to form satisfactory insular silicon layers in the recesses, even if the width of the recesses is 100 micrometres or less, whereas the lapping process using a lapping pad scrapes out silicon layers formed in the recesses, and is unable to form insular silicon layers in the recesses when the width of the recesses is 10 micrometres or less.

In affixing the wafers 121 and 126 to each other in Step H as shown in Figure 2H, the assembling jig 145 or 149 is used. The same pressures are applied in opposite directions to the central portions of the wafers 121 and 126 with the presser rods 143 and 144, or with the presser rod 150 and the protrusion 146, respectively. Consequently, the wafers 121 and 126 start joining from the central portions thereof and the joined area expands towards the periphery and, finally, the wafers 121 and 126 are affixed firmly to each other to form the laminated wafer 127, which is substantially unwarped (the warp is 3.7 micrometres at the maximum) as indicated by contour lines in Figure 11. The step between the adjacent contour lines is 0.50 micrometres. No bubble attributable to a stress induced by warping in the laminated wafer 127 is formed in the interface 128 between the wafers 121 and 126. Although pressures are applied in opposite directions to the central portions of the wafers 121 and 126 in affixing the wafers 121 and 126 to each other in this embodiment, the pressures may be applied to optional portions of the wafers 121 and 126.

Reasons for mirror-finishing the contact surfaces of the wafers 1 and 17 in an average roughness of 10×10^{-10} m or below before affixing the wafers 1 and 17 to each other in Step H (Figure 2H) will now be described.

Generally, it is considered that an optimum average roughness Ra of the surfaces of silicon wafers for semiconductor devices is in the range of 15 to 20×10^{-10} m. If the average roughness Ra is 30×10^{-10} m or greater, the wafers are unable to adhere to each other or, even if the wafers could adhere to each other, large bubbles are formed in the interface between the contact surfaces of the wafers. It is known generally that bubbles are scarcely formed when the average roughness is in the range of 15 to 20×10^{-10} m.

Our experimental studies to determine the upper limit of average roughness below which no bubble is formed will now be described.

The surfaces of wafers were lapped by a mechanical and chemical process to prepare sample wafers having different average roughnesses. The surface roughnesses of the mechanically and chemically lapped sample wafers were measured by a laser surface roughness tester having a resolution of 3×10^{-10} m after cleaning it by a washing process. The sample wafers having substantially the same surface roughness were attached to each other. The surfaces of the sample wafers were cleaned by a cleaning liquid, namely, a mixture of ammonia and hydrogen peroxide, before attaching the sample wafers to each other, and then the sample wafers were attached to each other in a clean atmosphere after drying them to obtain sample laminated wafers. The sample laminated wafers were subjected to a heat treatment at 1100°C in a nitrogen atmosphere, and then the sample laminated wafers were examined to see if any bubbles had formed in the sample laminated wafers.

The results of the experimental studies are shown in Figure 13, in which the bubble forming percentage is measured on the vertical axis, and average roughness Ra is measured on the horizontal axis. Bubble forming ratio is defined by:

$$\{(\text{Area of bubbles})/(\text{Surface area of laminated wafer})\} \times 100 (\%)$$

As is evident from Figure 13, no bubble is formed when the average roughness Ra is not more than 10×10^{-10} m.

Thus, the wafers 121 and 126 can be perfectly affixed closely to each other without warping the wafers 121 and 126, and without forming any bubbles therebetween, by using the assembling jig 145 (Figure 8) or 149 (Figure 9) when the average roughnesses of the wafers 121 and 126 are not more than 10×10^{-10} m.

The process for forming the polycrystalline layer 2 over the surface of the SiO₂ layer 3 in Step G (Figure 2G) is carried out at a comparatively low growing temperature in the range of about 500 to about 950°C (in this embodiment, about 600°C). Therefore, silicon crystal grains are formed apparently uniformly over the surface of the SiO₂ layer 3 at a comparatively low growth rate, and hence a large number of silicon crystal grains are formed. Consequently, the polycrystalline silicon layer 2 is formed uniformly by minute silicon crystal grains, without entailing the abnormal local growth of acicular crystals, namely, silicon whiskers having a length several to several tens of times a desired film thickness of about 5 micrometres, which is liable to occur when the polycrystalline silicon layer 2 is formed at a high growing temperature in the range of 100 to 1150°C. Such acicular crystals fall off in the subsequent lapping process and thereby pinholes are formed in the polycrystalline silicon layer 2. Thus, the polycrystalline silicon layer 2 formed by the present method can have uniform quality and no pinholes, and hence the wafers thus formed can be attached to each other without forming any bubbles in the interface therebetween. Accordingly, the laminated wafer thus formed is not damaged by expansion of the bubbles in heat treatment processes in manufacturing semiconductor devices, and hence the contamination of a furnace for the heat treatment of the wafers by fragments of broken wafers will not occur.

A lapping machine 130 as shown in Figure 7 employing a lapping disc formed by attaching a soft pad 135

formed of a soft sheet 134 containing abrasive grains 133 to a rigid disc 132 is used in Step G (Figure 2G) to lap the polycrystalline silicon layer 2. This lapping machine may be applied to the selective lapping of the first semiconductor substrate 17 in Step J (Figure 2J), in which abrasive grains 133 having a hardness lower than that of silicon is used. Since the rigid disc 132 is rigid and the soft pad 135 consisting of the soft sheet 134 and the abrasive grains 133 is thin, the first semiconductor substrate 17 can be lapped flat by selective lapping, namely, the lapping action of the lapping disc is stopped by the surface of the insulating layer 3 (SiO₂ layer), to form the insular semiconductor regions 5 (silicon layers) in the recesses formed by the insulating layer 3 with their surfaces flat and flush with the surface of the insulating layer 3. Since the hardness of the abrasive grains 133 is lower than those of the first semiconductor layer 17 and the insulating layer 3, the surface of the SOI substrate 153, namely, the surfaces of the semiconductor regions 5 and that of the insulating layer 3, is not damaged by selective lapping. A wax may be used instead of the soft sheet 134. When a wax is used, the lapping disc can be readily prepared by applying the molten wax to the surface of the rigid disc 132, and the lapping disc can be readily reproduced by removing the wax by melting and applying the new wax again to the surface of the rigid disc 132.

Although the selective lapping operation is stopped upon the exposure of all the portions of the SiO₂ layer other than those forming the bottoms of the recesses in the selective lapping process shown in Figures 4A and 4B, the selective lapping operation may be continued further to lap the silicon layer 121 further until the surfaces of the insular silicon layers 152 sink below the surface of the SiO₂ layer 123 slightly by a depth of about 200×10^{-10} m as shown in Figure 15. Lapping the silicon layer 121 so that the surfaces of the insular silicon layers 152 sink below the surface of the SiO₂ forms all the insular silicon layers 152 in further uniform thickness, facilitates handling the SOI substrate 153 in forming semiconductor devices on the insular silicon layers 152 and reduces the possibility of damaging and contaminating the insular silicon layers 152 in handling the SOI substrate 153, and thereby the reliability of the semiconductor device is improved. When the insular silicon layers 152 are desired to be formed in an appropriate thickness, for example, about 1000×10^{-10} m, with the surfaces thereof extending slightly below the surface of the SiO₂ layer 123, for example, by a depth of about 20×10^{-10} m, the recesses may be formed in a depth of about 1200×10^{-10} m.

A gettering process for gettering the insular silicon layers 152 in fabricating a semiconductor device employing the SOI substrate 153 will now be described with reference to Figure 14.

Generally, a so-called IG process which forms a precipitated layer of oxygen within a substrate and makes the defects absorb metallic impurities or a so-called EG process which forms a damaged layer in the lower surface of a substrate by sand blasting or polycrystalline silicon layer on the lower surface of a substrate is applied practically as gettering means in directly forming semiconductor elements on a substrate to construct a semiconductor device. However, such gettering means is not applicable to a semiconductor substrate of a SOI construction, such as the SOI substrate 153, having an insulating layer (the SiO₂ layer 123) formed under insular silicon layers (the insular silicon layers 152). Accordingly, metallic impurities remain unremoved in interfaces between the source and gate electrodes and between the gate and drain electrodes exerting adverse effects, such as increase in leakage current and reduction in the life of the semiconductor device, on the characteristics of the semiconductor device.

To obviate such adverse effects of metallic impurities on the semiconductor device, a gate electrode 161 is formed on a gate oxide film 160 formed on the insular silicon layer 152, a source region 152s, a gate region 152g and a drain region 152d are formed in the insular silicon layer 152 as shown in Figure 14, the outer portions of the source region 152s and the drain region 152d are doped by ion implanting with an electrically inert impurity, such as oxygen ions, in a doping density of $1 \times 10^{16}/\text{cm}^2$ as shown in Figure 14, and then the SOI substrate 153 is heat-treated for gettering in an oxygen atmosphere at 700°C for one hour to form getter regions 162. The doping is successful only when lattice faults are formed in the crystals as a getter.

The getter regions 162 thus formed in the outer portions of the source region 152s and the drain region 152d by ion implanting absorb metallic impurities during the subsequent heat treatment in fabricating a semiconductor device, so that the current leakage in the semiconductor device is reduced and the life is extended. The ion implanting process may be carried out before forming the gate electrode 161 or before forming the source region 152s and the drain region 152d. The getter regions 162 are effective also in fabricating a semiconductor device by using a substrate formed by a method according to the present invention, a substrate formed by a separation by implanted oxygen (SIMOX) method, or a substrate formed by an epitaxial growth method, provided that the substrate is of a SOI construction. Naturally, the getter regions 162 can be effectively applied to a substrate having insular silicon layers formed flush with the surface of the insulating layer. The electrically inert impurity may be a substance other than oxygen, such as silicon, germanium, carbon, nitrogen or argon.

Claims

1. A semiconductor memory comprising:
a semiconductor substrate (1);
5 a polycrystalline silicon layer (2) formed on the substrate;
an insulating layer (3) formed on the polycrystalline layer opposite the substrate, the surface of the insulating layer opposite the polycrystalline layer being formed with a plurality of recesses (4);
a semiconductor region (5) formed in each of the recesses and providing a source-drain region of a respective MIS transistor recesses (6, 7, 12, 13); and
10 at least one capacitor (1, 2, 10, 11) being provided for each MIS transistor, each capacitor comprising:
a first electrode (9, 10) formed in a respective recess in the polycrystalline layer beneath the respective MIS transistor and connected electrically thereto through a respective contact hole (8) formed in the insulating layer; and
a dielectric layer (11) separating the first electrode from the polycrystalline layer whereby the substrate
15 and polycrystalline layer form the second electrode of the capacitor.

2. A method of manufacturing a semiconductor memory, the method comprising the steps of:
selectively removing portions of the surface of a first semiconductor substrate (17) to form recesses and semiconductor lands (18) on which MIS transistors (6, 7, 13) are to be formed;
20 forming an insulating layer (3) over the surface of the first semiconductor substrate (17);
forming respective contact holes (8) through the insulating layer (3) so as to reach the surfaces of the lands (18) of the first semiconductor substrate (17);
forming respective electrode layers (9, 10) on the insulating layer (3) and in the contact holes (8) so as to connect with the surfaces of the lands (18) of the first semiconductor substrate (17) through the contact
25 holes (8);
coating the electrode layers (10) with respective dielectric layers (11);
forming a semiconductor layer (2) over the insulating layer (3) so as to cover the electrode layers (10) coated with the dielectric layers (11) and so that the electrode layers (10), dielectric layers (11) and semiconductor layer (2) form a plurality of capacitors (2, 10, 11); attaching a second semiconductor substrate
30 (1) to the semiconductor layer (2) after flattening the contact surface of the semiconductor layer (2);
removing the first semiconductor substrate (17) leaving the lands (18) thereof surrounded by the insulating layer (3) as semiconductor regions (15); and
forming the MIS transistors (6, 7, 13) on the lands (18) of the first semiconductor substrate (17) remaining as the semiconductor regions (5) so that the MIS transistors are electrically connected to the capacitors
35 through the contact holes (8).

3. A method according to claim 2 wherein the first semiconductor substrate (17) is removed leaving the lands (18) thereof surrounded by the insulating layer (3) as semiconductor regions (5) by a lapping process which
40 employs an alkaline liquid (156) as a lapping liquid, and the ratio of lapping rate for lapping portions of the first semiconductor substrate (17) other than those forming the lands (18) to the lapping rate for lapping the portions of the first semiconductor substrate (17) forming the lands (18) is not less than twenty.

Patentansprüche

- 45 1. Halbleiterspeicher, der aufweist:
ein Halbleitersubstrat (1);
eine polykristalline Siliziumschicht (2), die auf dem Substrat gebildet ist;
eine Isolierschicht (3), die auf der polykristallinen Schicht gegenüber dem Substrat gebildet ist, wo-
50 bei die Oberfläche der Isolierschicht gegenüber der polykristallinen Schicht eine Vielzahl von Ausnehmungen (4) aufweist;
einen Halbleiterbereich (5), der in jeder Ausnehmung gebildet ist und einen Source-Drain-Bereich eines entsprechenden MIS-Transistors (6, 7, 12, 13) bereitstellt; und
zumindest einen Kondensator (1, 2, 10, 11), der für jeden MIS-Transistor vorgesehen ist, wobei je-
55 der Kondensator aufweist:
eine erste Elektrode (9, 10), die in einer entsprechenden Ausnehmung in der polykristallinen Schicht unterhalb des entsprechenden MIS-Transistors gebildet ist und elektrisch damit über ein entsprechendes Kontaktloch (8) verbunden ist, das in der Isolierschicht gebildet ist; und

eine dielektrische Schicht (11), die die erste Elektrode von der polykristallinen Schicht trennt, wodurch das Substrat und die polykristalline Schicht die zweite Elektrode des Kondensators bilden.

2. Verfahren zur Herstellung eines Halbleiterspeichers, wobei das Verfahren folgende Schritte aufweist:
 - 5 selektives Entfernen von Bereichen der Oberfläche des ersten Halbleitersubstrats (17), um Ausnehmungen und Halbleiter-Lands (18) zu bilden, auf denen MIS-Transistoren (6, 7, 13) gebildet werden sollen;
 - Bilden einer Isolationsschicht (3) über der Oberfläche des ersten Halbleitersubstrats (17);
 - 10 Bilden entsprechender Kontaktlöcher (8) durch die Isolationsschicht (3), um so die Oberflächen der Lands (18) des ersten Halbleitersubstrats (17) zu erreichen;
 - Bilden entsprechender Elektrodenschichten (9, 10) auf der Isolationsschicht (3) und in den Kontaktlöchern (8), um so die Oberflächen der Lands (18) des ersten Halbleitersubstrats (17) über die Kontaktlöcher (8) zu kontaktieren;
 - Überziehen der Elektrodenschichten (10) mit entsprechenden dielektrischen Schichten (11);
 - 15 Bilden einer Halbleiterschicht (2) über der Isolationsschicht (3), um die Elektrodenschichten zu bedecken, die mit den dielektrischen Schichten (11) überzogen sind, so daß die Elektrodenschichten (10), die dielektrischen Schichten (11) und die Halbleiterschicht (2) eine Vielzahl von Kondensatoren (2, 10, 11) bilden;
 - Befestigen eines zweiten Halbleitersubstrats (1) an der Halbleiterschicht (2), nachdem die Kontakt-
20 oberfläche der Halbleiterschicht (2) eben gemacht wurde;
 - Entfernen des ersten Halbleitersubstrats (17), wobei darauf die Lands (18) zurückgelassen werden, die von der Isolierschicht (3) als Halbleiterbereiche (15) umgeben werden; und
 - Bilden der MIS-Transistoren (6, 7, 13) auf den Lands (18) des ersten Halbleitersubstrats (17), die
25 als Halbleiterbereiche (5) verbleiben, so daß die MIS-Transistoren elektrisch mit den Kondensatoren über die Kontaktlöcher (8) verbunden werden.
3. Verfahren nach Anspruch 2, wobei das erste Halbleitersubstrat (17) entfernt wird, wobei die Lands (18) zurückgelassen werden, die von der Isolationsschicht (3) als Halbleiterbereiche (15) umgeben werden,
30 durch einen L äpp-Prozeß, wobei eine alkaline Flüssigkeit (156) als L äpp-Flüssigkeit verwendet wird, und das Verhältnis der L äpp-Rate zum L äppen der Bereiche des ersten Halbleitersubstrats (17) mit Ausnahme derjenigen, die die Lands (18) bilden, zur L äpp-Rate zum L äppen der Bereiche des ersten Halbleitersubstrats (17), die die Lands (18) bilden, nicht kleiner als zwanzig ist.

35 Revendications

1. Mémoire à semiconducteur comprenant :
 - un substrat semiconducteur (1) ;
 - une couche en silicium polycristallin (2) formée sur le substrat ;
 - 40 une couche isolante (3) formée sur la couche polycristalline de manière à faire face au substrat, la surface de la couche isolante faisant face à la couche polycristalline étant munie d'une pluralité d'évidements (4) ;
 - une région semiconductrice (5) formée dans chacun des évidements et constituant une région de source/drain d'un transistor métal-isolant-semiconducteur (MIS) (6, 7, 12, 13) ; et
 - 45 au moins une capacité (1, 2, 10, 11) étant prévue pour chaque transistor MIS, chaque capacité comprenant :
 - une première électrode (9, 10) formée dans un évidement respectif ménagé dans la couche polycristalline au-dessous du transistor MIS respectif et connectée électriquement à celui-ci par l'intermédiaire d'un trou de contact respectif (8) formé dans la couche isolante ; et
 - 50 une couche diélectrique (11) qui sépare la première électrode de la couche polycristalline et ainsi, le substrat et la couche polycristalline forment la seconde électrode de la capacité.
2. Procédé de fabrication d'une mémoire à semiconducteur, le procédé comprenant les étapes de :
 - enlèvement sélectif de parties de la surface d'un premier substrat semiconducteur (17) pour former
55 des évidements et des zones semiconductrices (18) sur lesquelles des transistors MIS (6, 7, 13) doivent être formés ;
 - formation d'une couche isolante (3) sur la surface du premier substrat semiconducteur (17) ;
 - formation de trous de contact respectifs (8) au travers de la couche isolante (3) de manière à at-

teindre les surfaces des zones (18) du premier substrat semiconducteur (17) ;

formation de couches d'électrode respectives (9, 10) sur la couche isolante (3) et dans les trous de contact (8) de manière à réaliser une connexion avec les surfaces des zones (18) du premier substrat semiconducteur (17) au travers des trous de contact (8) ;

5 revêtement des couches d'électrode (10) avec des couches diélectriques respectives (11) ;

formation d'une couche semiconductrice (2) sur la couche isolante (3) de manière à recouvrir les couches d'électrode (10) revêtues des couches diélectriques (11) et de telle sorte que les couches d'électrode (10), les couches diélectriques (11) et la couche semiconductrice (2) forment une pluralité de capacités (2, 10, 11) ;

10 fixation d'un second substrat semiconducteur (1) à la couche semiconductrice (2) après aplatissement de la surface de contact de la couche semiconductrice (2) ;

enlèvement du premier substrat semiconducteur (17) en laissant ses zones (18) entourées par la couche isolante (3) en tant que régions semiconductrices (15) ; et

15 formation des transistors MIS (6, 7, 13) sur les zones (18) du premier substrat semiconducteur (17) restantes en tant que régions semiconductrices (5) de telle sorte que les transistors MIS soient connectés électriquement aux capacités par l'intermédiaire des trous de contact (8).

3. Procédé selon la revendication 2, dans lequel le premier substrat semiconducteur (17) est ôté en laissant ses zones (18) entourées par la couche isolante (3) en tant que régions semiconductrices (5) au moyen
20 d'un processus d'érosion qui utilise un liquide alcalin (156) en tant que liquide d'érosion et le rapport de la vitesse d'érosion pour des parties d'érosion du premier substrat semiconducteur (17) autres que celles formant les zones (18) sur la vitesse d'érosion pour éroder les parties du premier substrat semiconducteur (17) formant les zones (18) n'est pas inférieur à vingt.

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FIG. 1

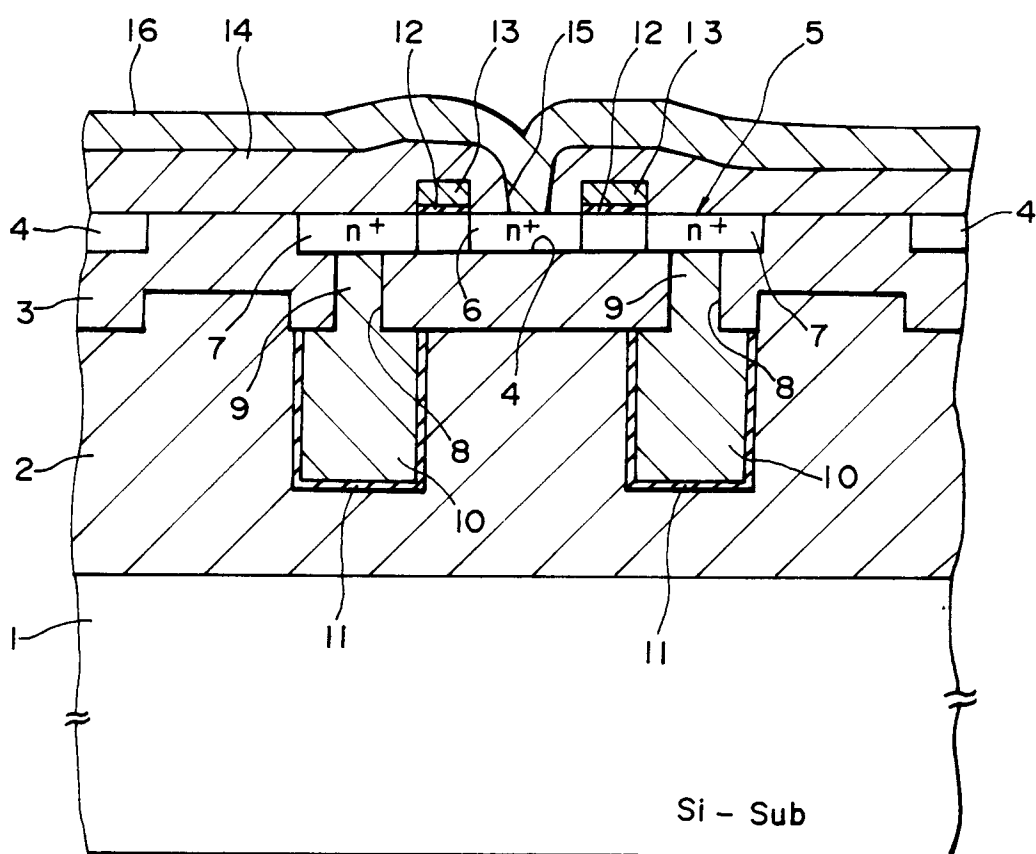


FIG. 2A

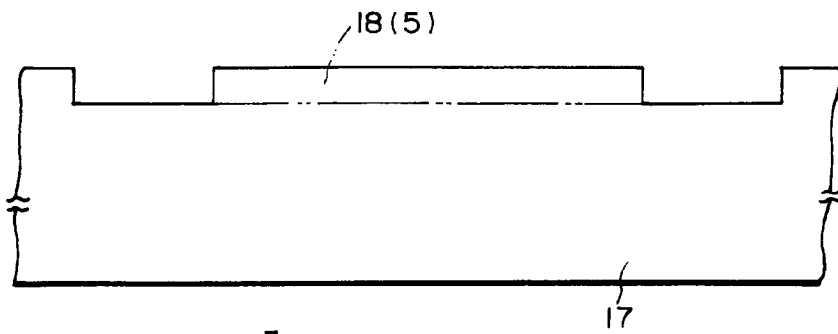


FIG. 2B

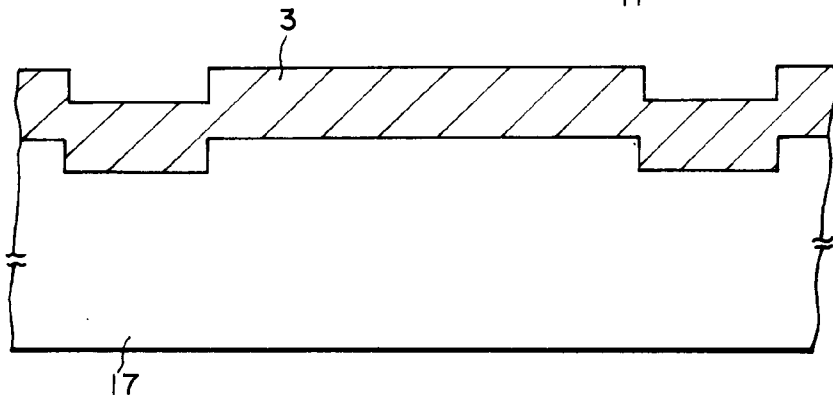


FIG. 2C

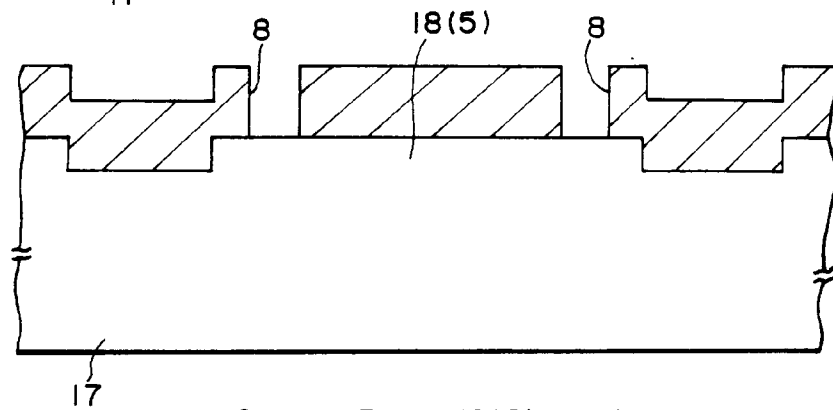


FIG. 2D

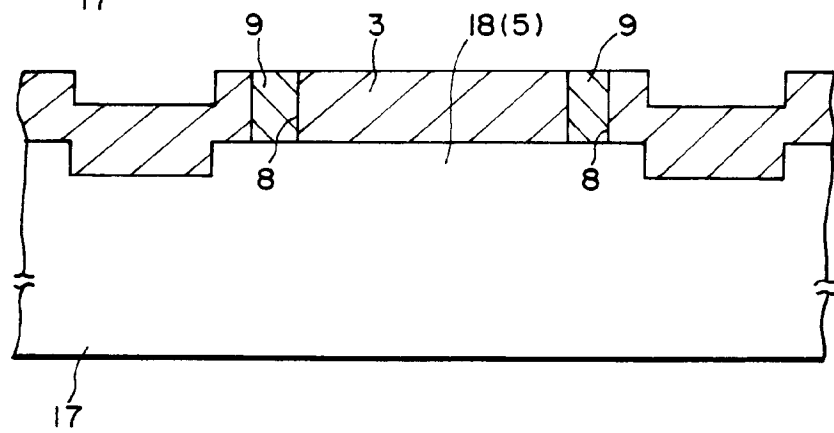


FIG.2E

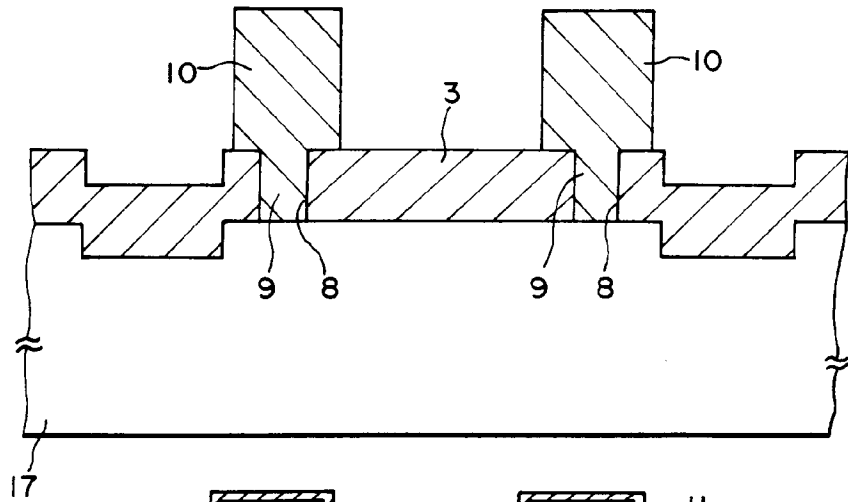


FIG.2F

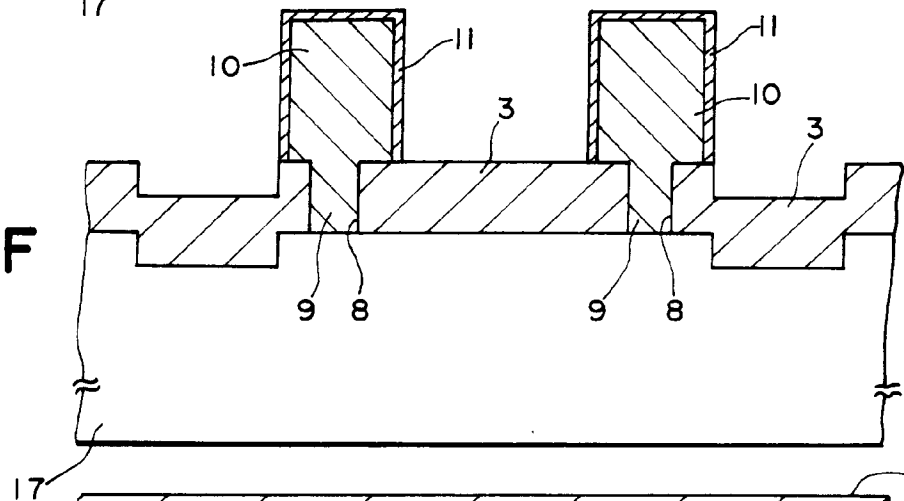


FIG.2G

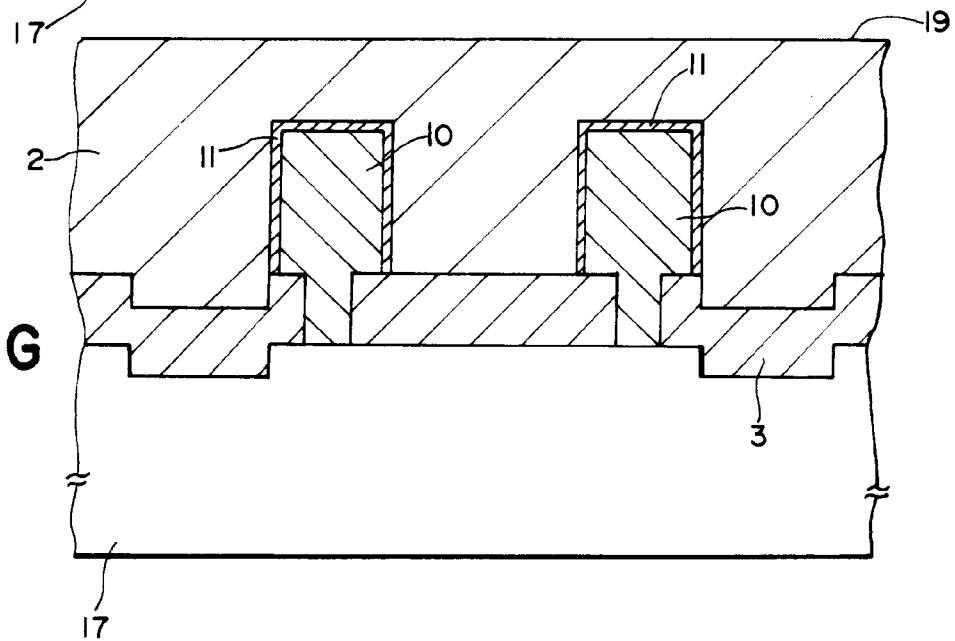


FIG. 2H

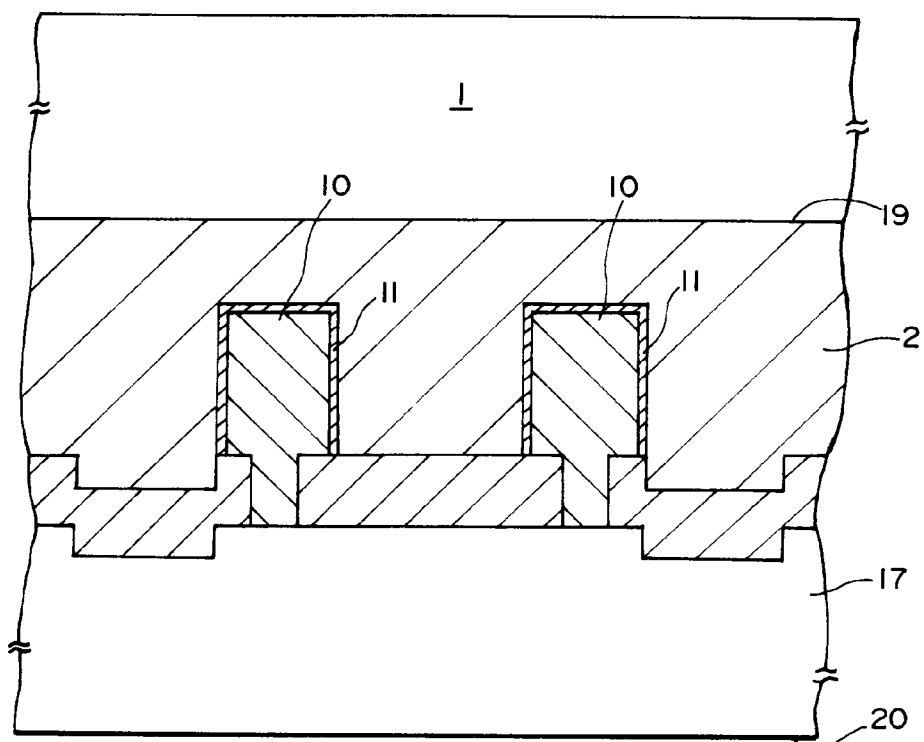


FIG. 2I

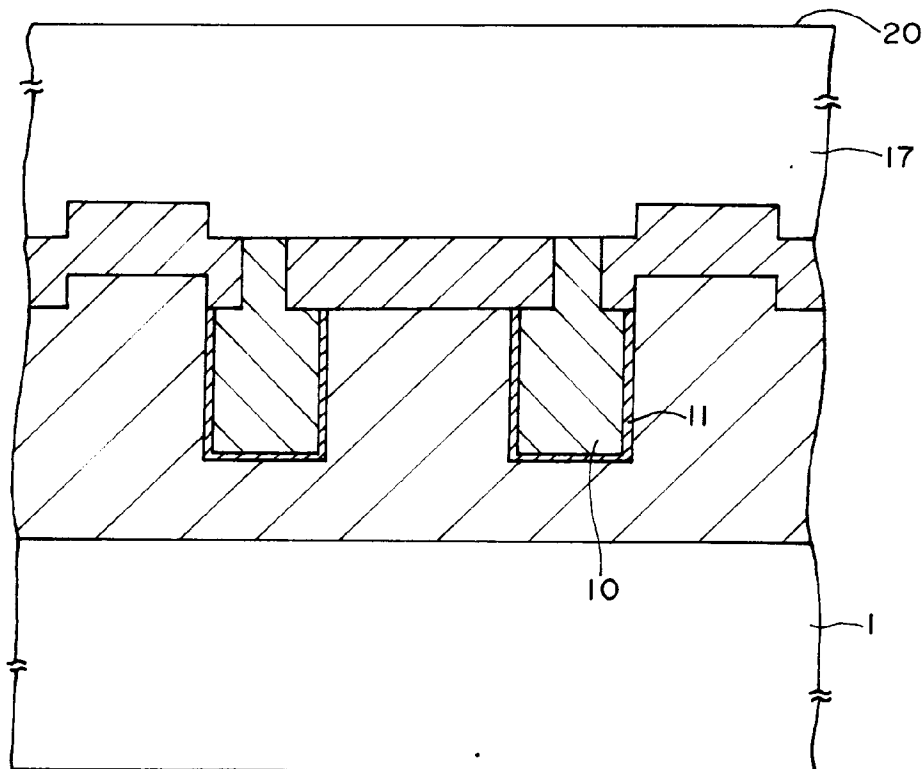


FIG. 2J

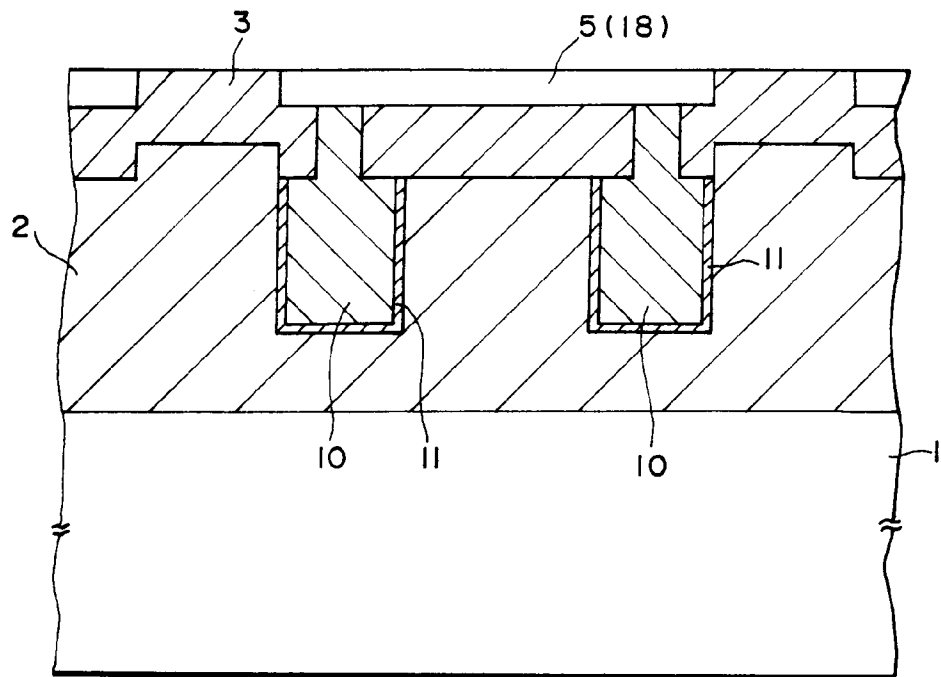


FIG. 2K

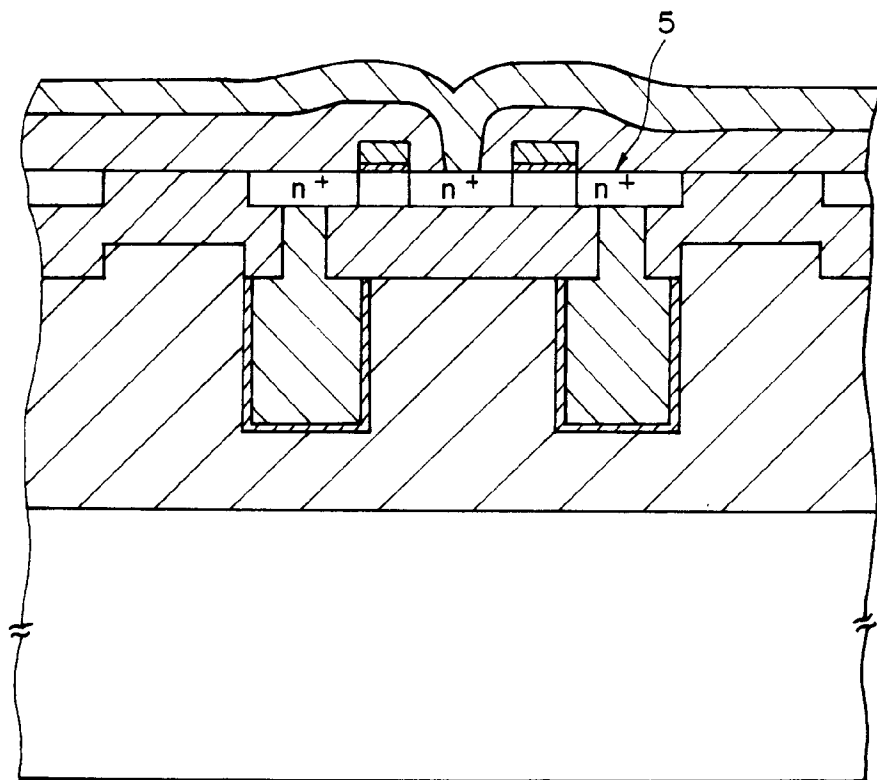


FIG. 3

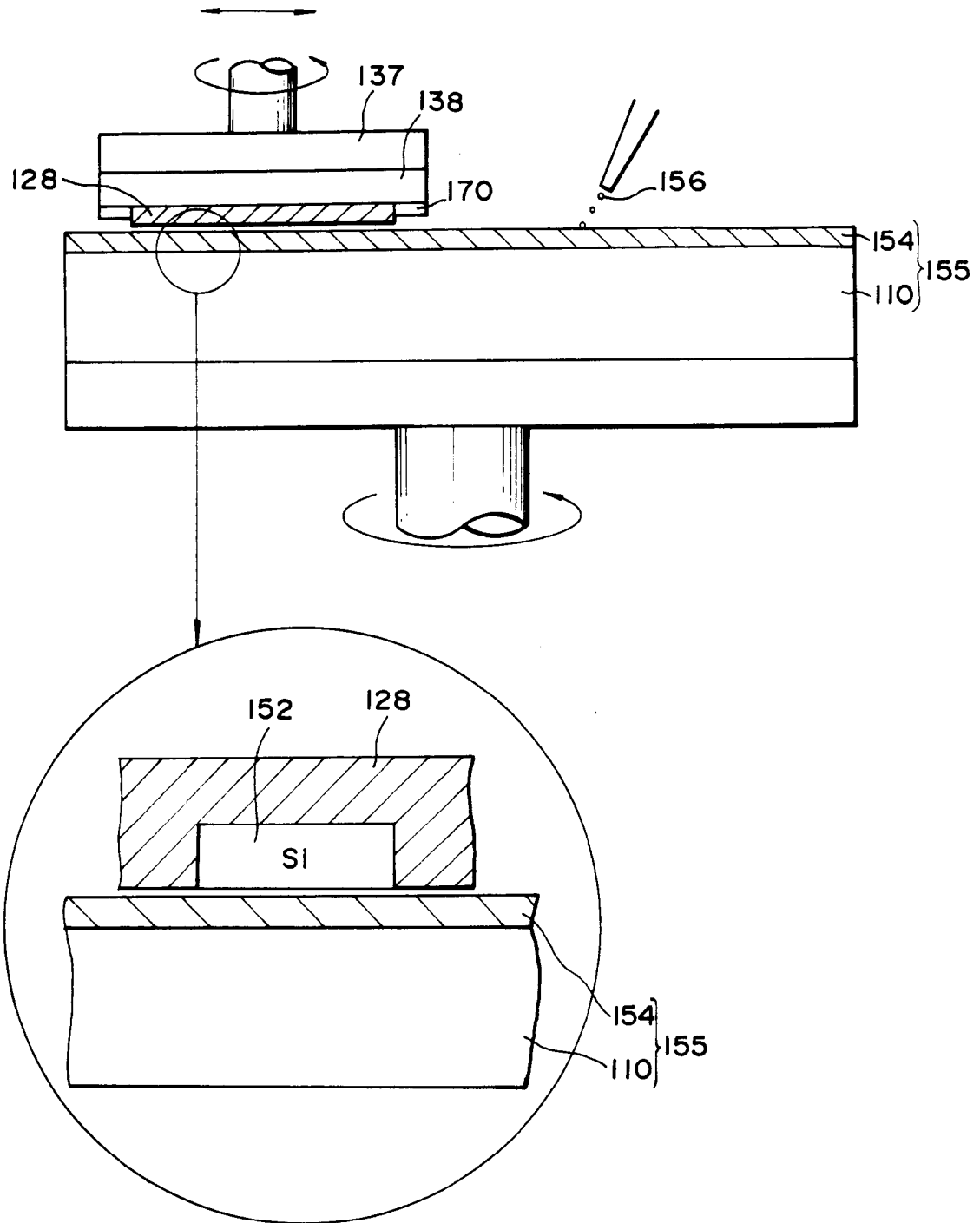


FIG. 4 A

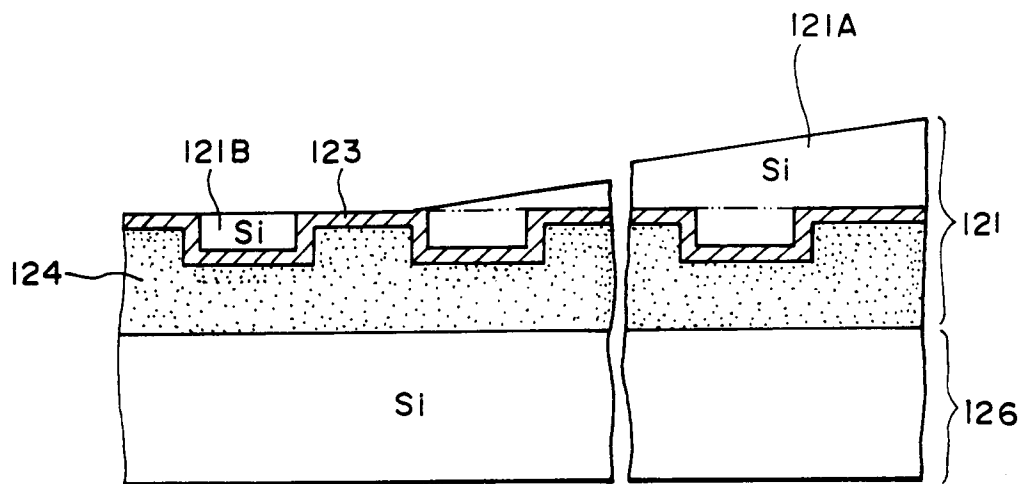


FIG. 4 B

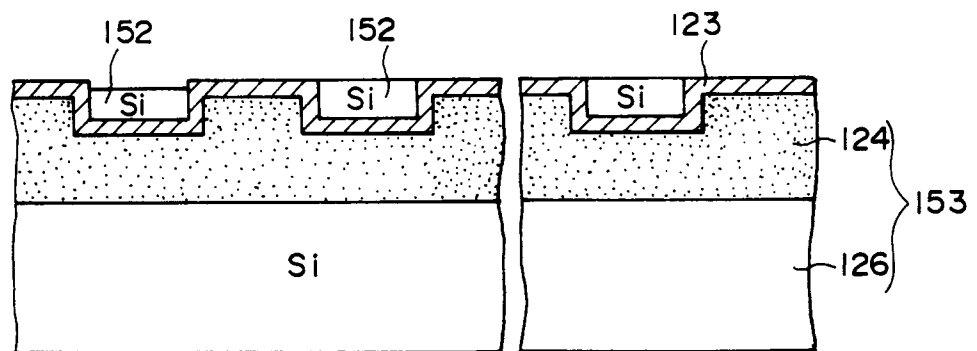


FIG.5

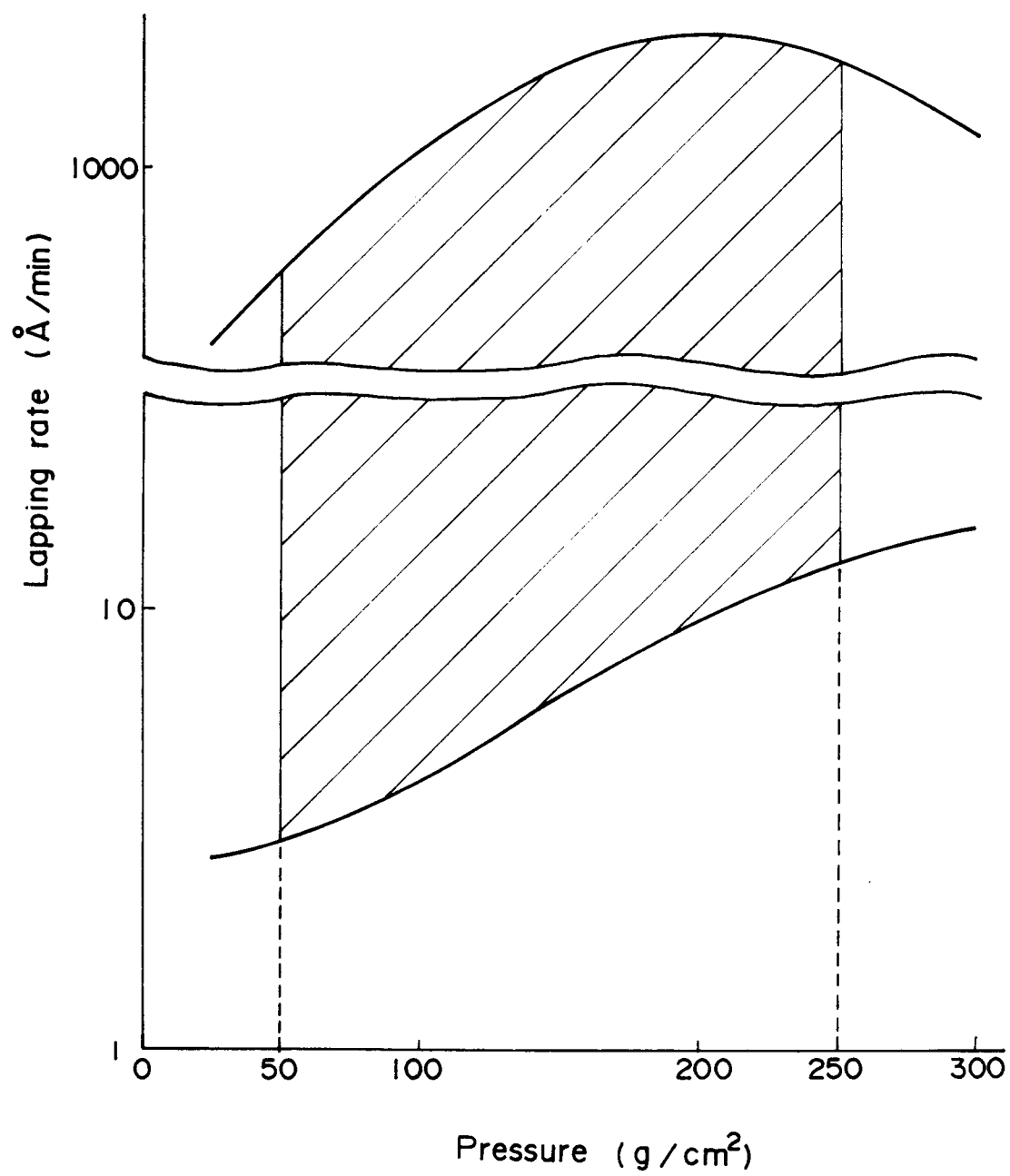


FIG. 6

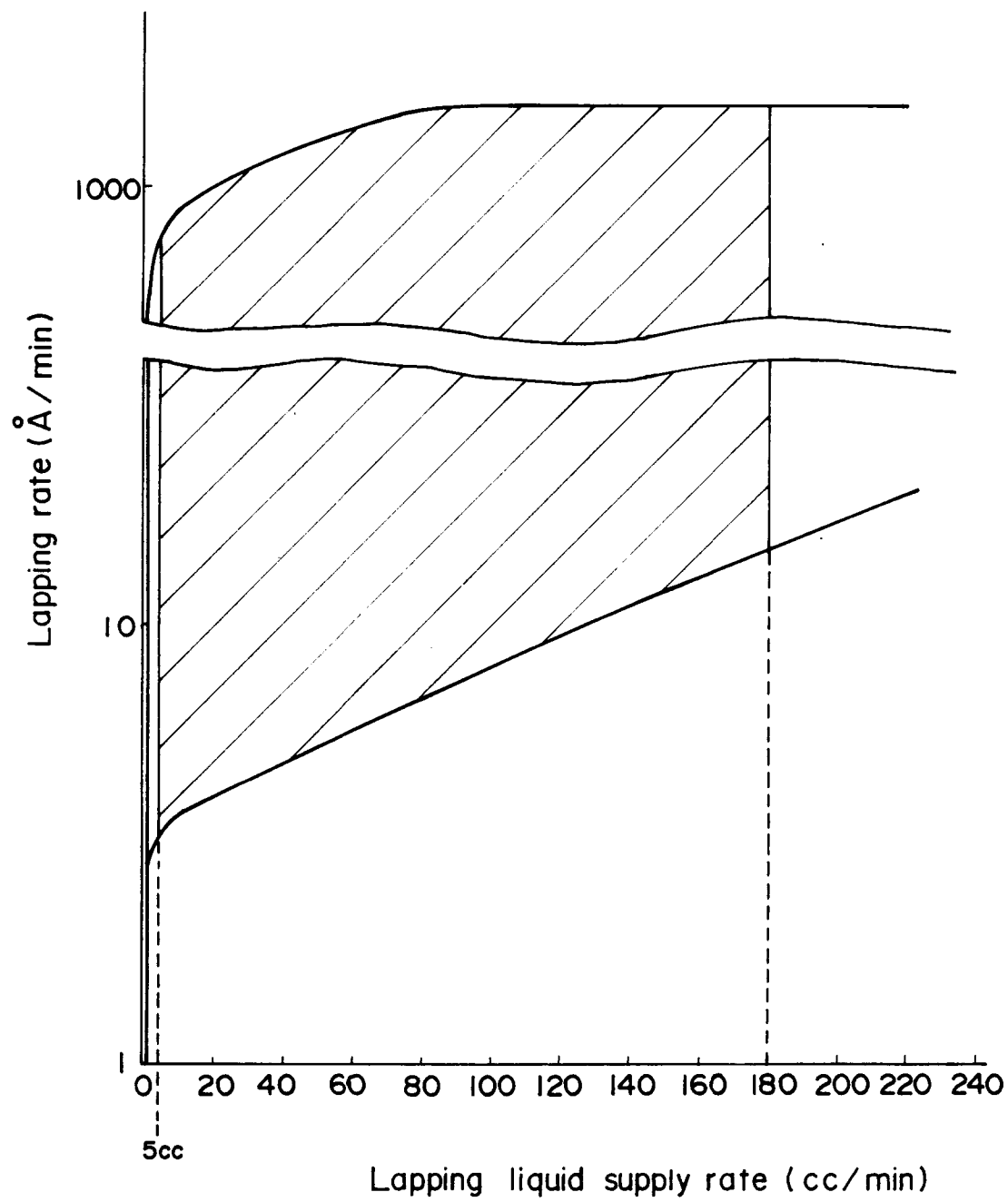


FIG. 7

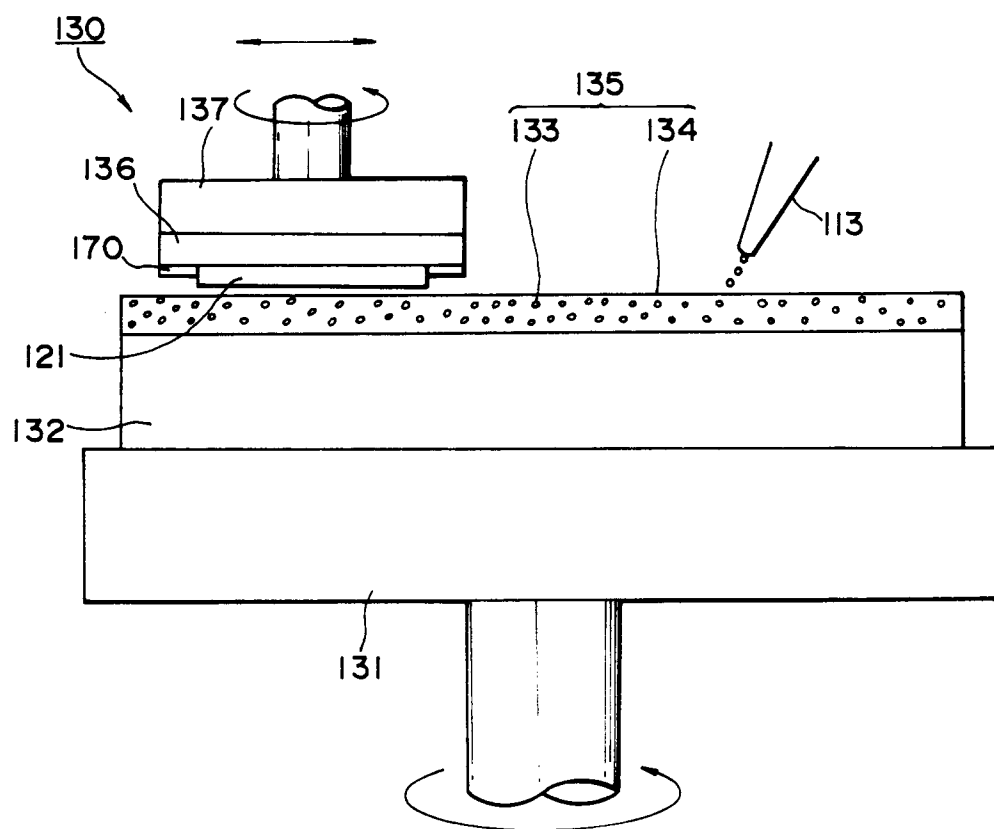


FIG. 8

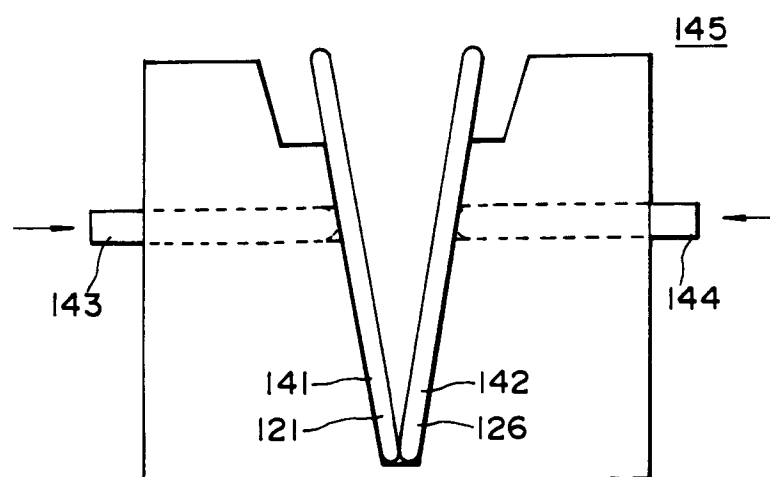


FIG. 11

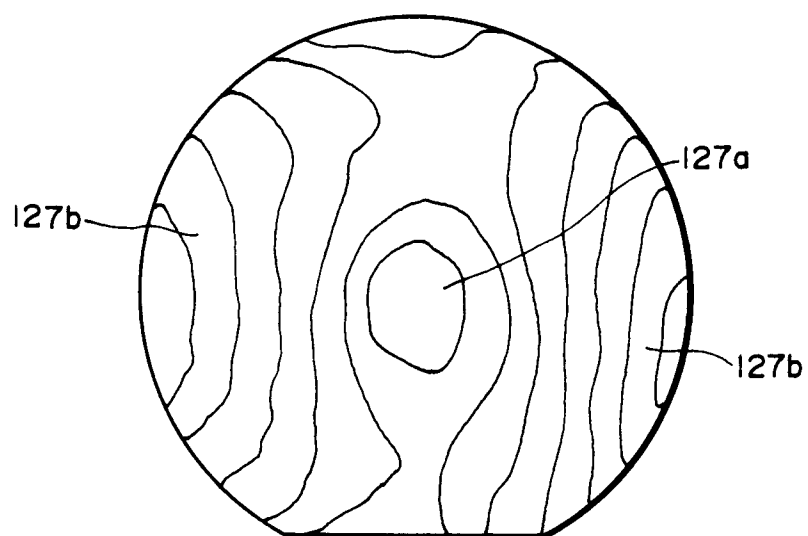


FIG. 9

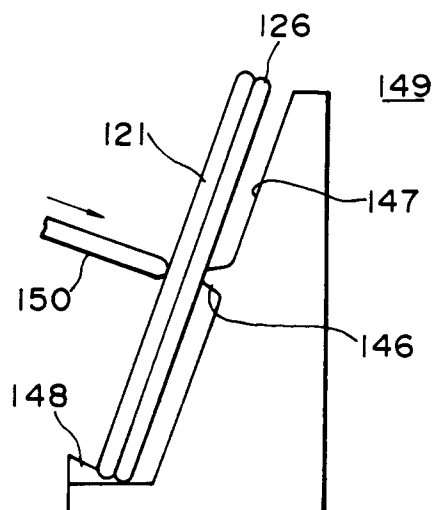


FIG. 10

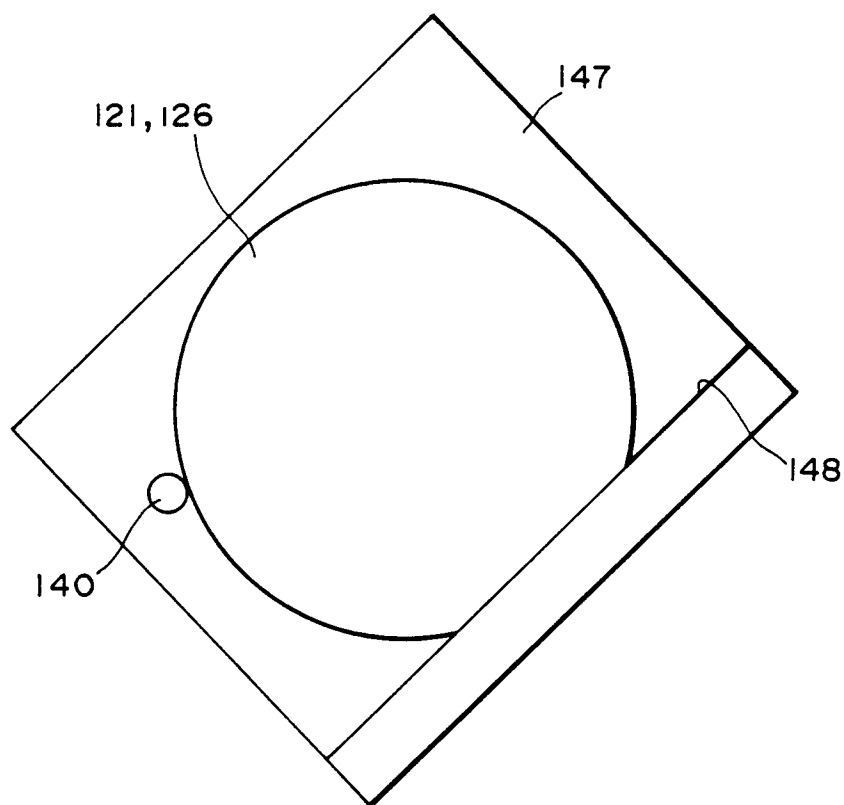


FIG. 12

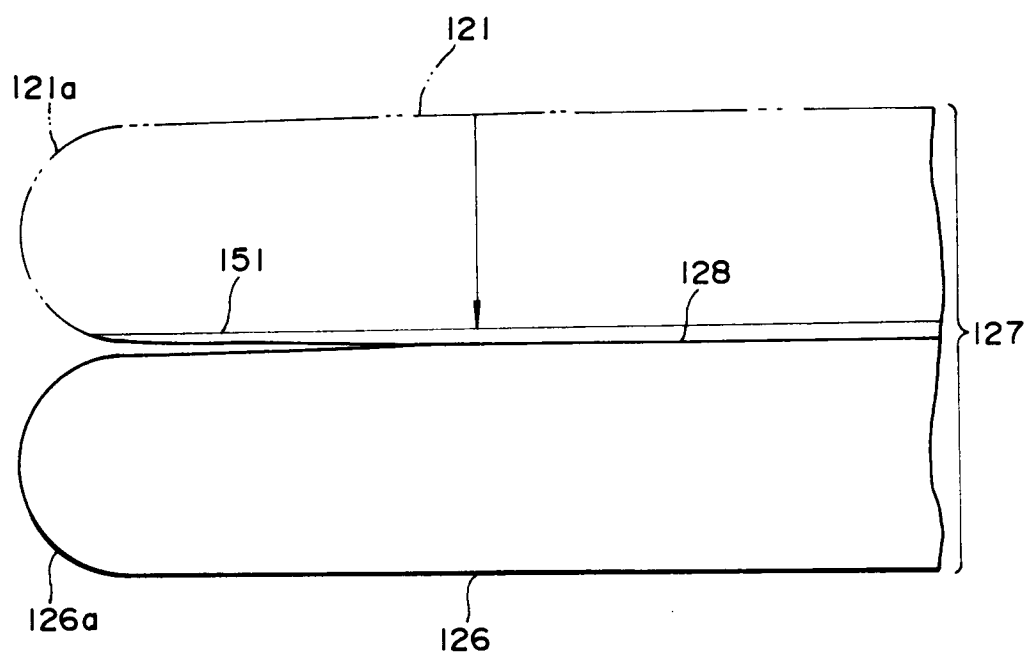


FIG. 13

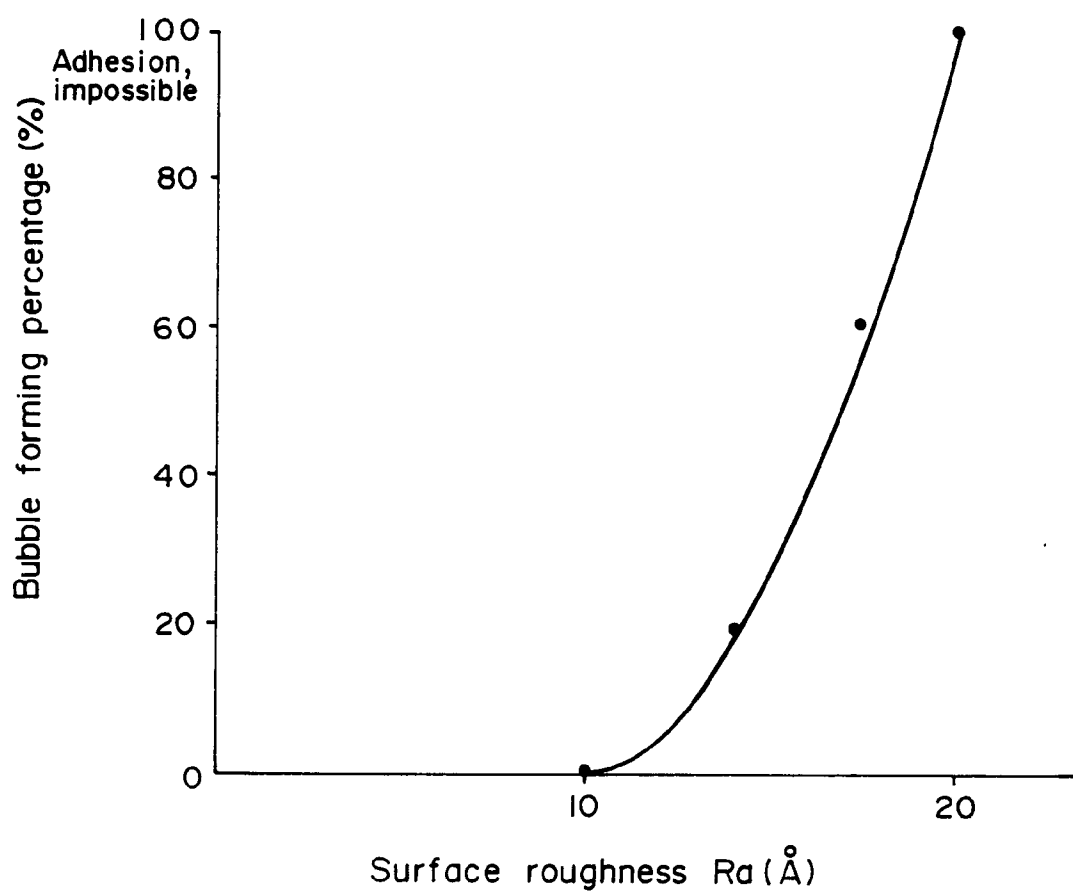


FIG. 14

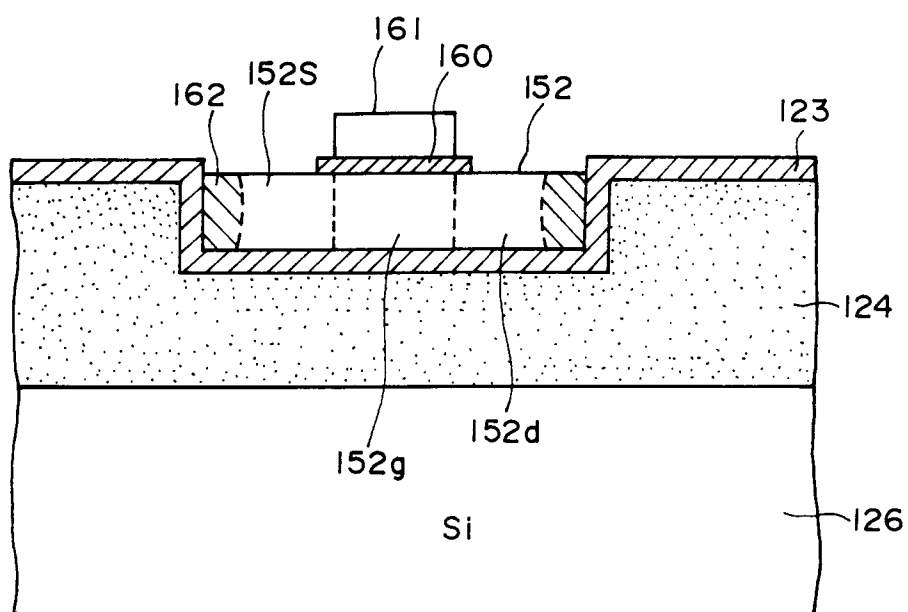


FIG. 15

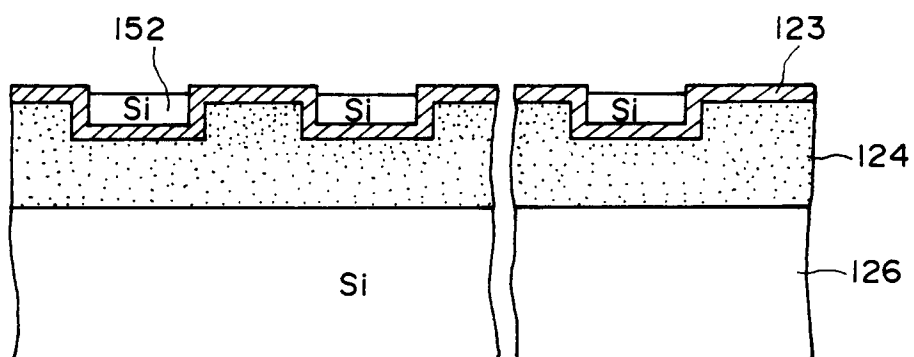


FIG.16A

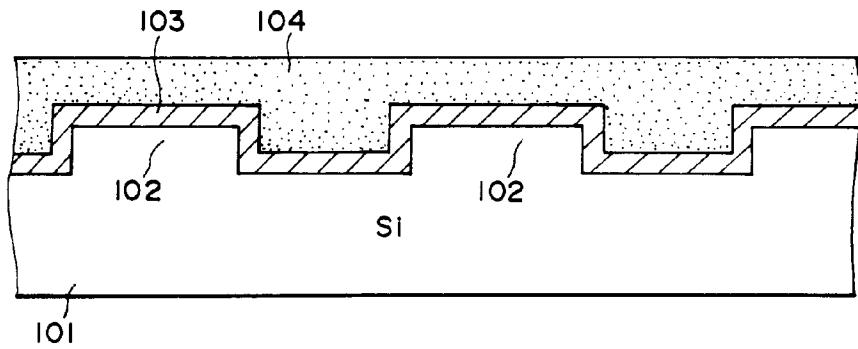


FIG.16B

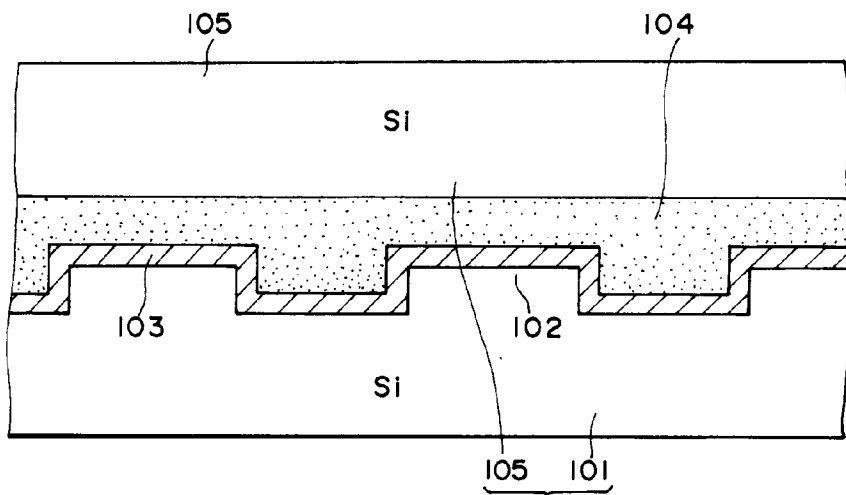


FIG.16C

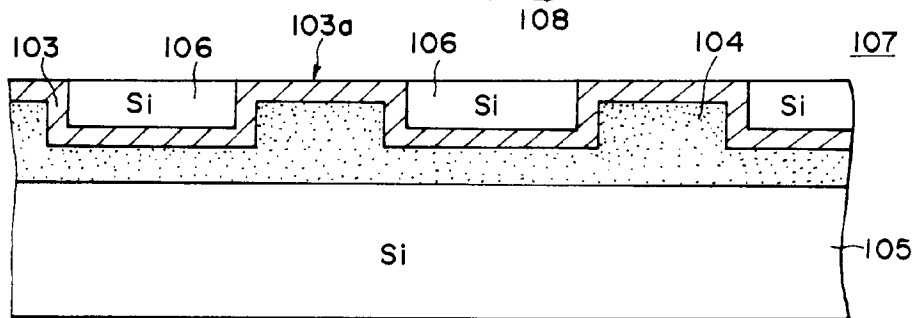


FIG. 17

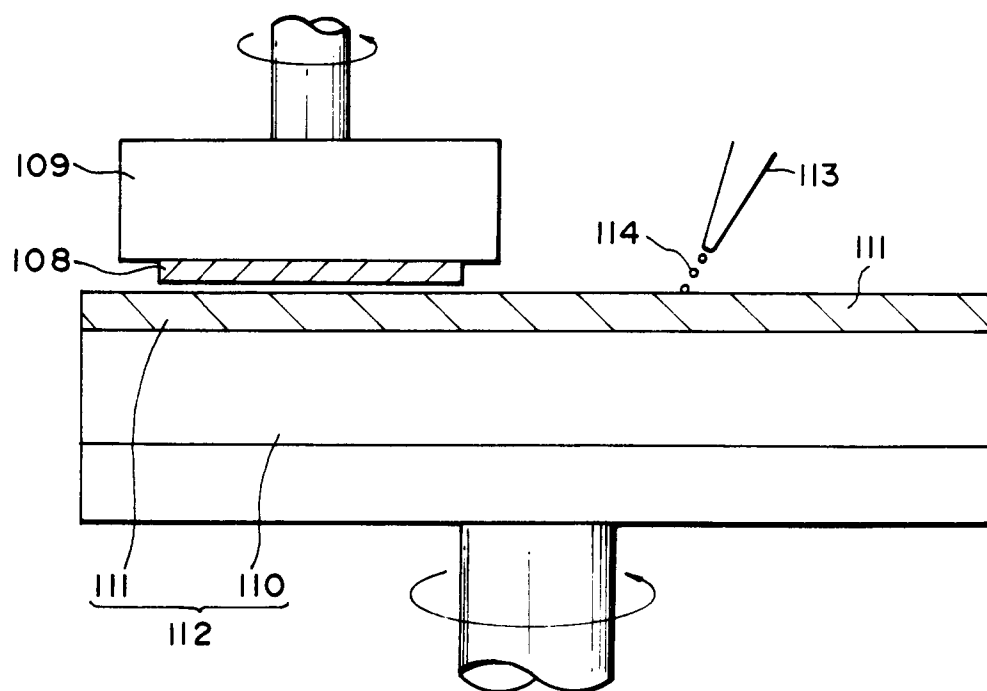


FIG. 18

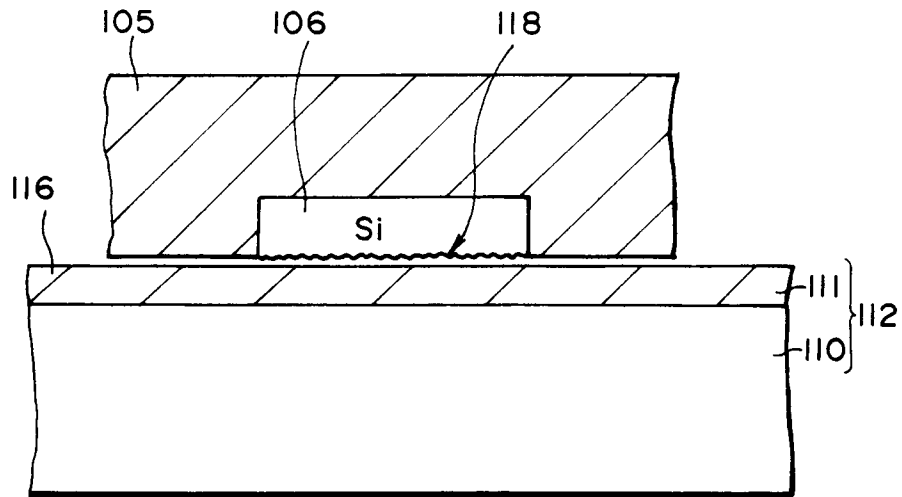


FIG. 19

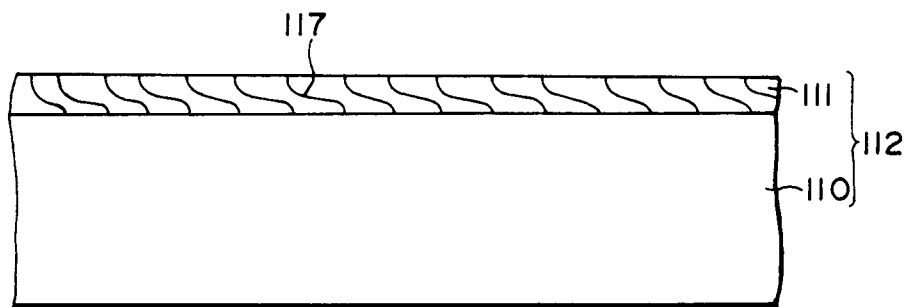


FIG. 20

