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(54) Buffer memory subsystem for peripheral controllers and method.

(37) A buffer memory subsystem for a peripheral controller. A CPU is provided for initiating data transfer. A host adapter is also provided. A memory buffer is used to store data temporarily. The peripheral controller is adapted for operating in an environment having at least two data communications buses: a CPU data communications bus connected between the CPU and the peripheral controller, and a buffer data communications bus, isolated from the CPU data communications bus, and connected to the peripheral controller, to the memory buffer and to the host adapter. In this way, a mechanism is provided to allow the CPU to access the memory buffer by means of the peripheral controller.

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## EUROPEAN SEARCH REPORT

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