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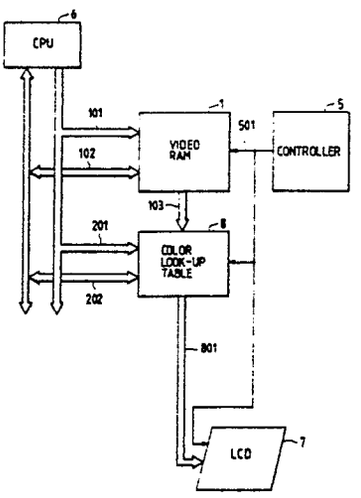
(54) Display system.

(57) A display system comprises a color look-up table for storing therein color data which specify a color or a gray scale of data to be displayed, and a display unit having a number of displayable colors or gray scales smaller than the number of colors or gray scales which can be specified by color data stored in the color look-up table. The color look-up table (8) includes a color look-up table (81) for CPU for storing therein first color data supplied from a central processing unit (CPU) (6), a color data conversion circuit (85) for converting the first color data into second color data having a number of colors or gray scales equal to the number of displayable colors or gray scales of the display unit (7), and another color look-up table (82) for display for storing therein the second color data supplied from the color data conversion circuit (85). The display unit (7) displays thereon data in a color or a gray scale specified by the second color data read out from the color look-up table (82) for display. The CPU (6) reads out first color data necessary for data processing from the color look-up table (81) for CPU.

FIG. 3



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DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to a display system having a color look-up table. and more particularly to a display system suitable to improve the efficiency in utilization of such color look-up table where a display unit is used which is limited in the number of display colors or display gray scales.

As the improvement in performance of data processing systems such as personal computers and word processors proceeds, the improvement in performance of display systems for displaying various data from such data processing systems thereon proceeds remarkably. An outstanding one of the improved performances is an increase in number of display colors, that is, augmentation of a multi-color function. One of known measures to realize the function is a technique of making use of a color look-up table to increase displayable colors without increasing the storage capacity of a video random access memory for storing display data therein. A technique of the type is disclosed, for example, in Japanese Patent Application Laid-Open No. 50-140228 or in Japanese Patent Application Laid-Open No. 60-254190. FIG. 1 diagrammatically shows an exemplary one of conventional display systems employing a color look-up table. The display system shown includes a video random access memory (hereinafter abbreviated as "video RAM") 1 for storing characters, figures and so forth as display data therein, a color look-up table 2 for converting display data into digital color signals, a digital-to-analog converter (hereinafter abbreviated as "DAC") 3 for converting digital color signals into analog color signals, a cathode-ray tube (hereinafter abbreviated as "CRT") 4 for displaying a color corresponding to levels of analog color signals thereon, and a controller 5 for establishing synchronization among the video RAM 1, color look-up table 2, DAC 3 and CRT 4, for successively reading out display data stored in the video RAM 1 and for causing the CRT 4 to display such read out data at a specified location of the CRT 4. The display system further includes a central processing unit (hereinafter abbreviated as "CPU") 6 for writing display data into the video RAM 1. The CPU 6 also executes writing and reading out operations of color data into and from the color look-up table 2.

Display data are stored over a data bus 102 into an address of the video RAM 1 designated by the CPU 6 over an address bus 101. Such display data are read out from the video RAM 1 in response to a control signal 501 from the controller 5 and outputted to a pixel data bus 103. The color look-up table 2 has color data stored in all addresses thereof in advance over an address bus 201 and a data bus 202 by the CPU 6. The display data outputted to the pixel data bus 103 are utilized as an address for referring to the color look-up table 2, and data resultantly read out from the color look-up table 2 are outputted to a red (hereinafter abbreviated as "R") display digital signal bus 210, a green (hereinafter abbreviated as "G") display digital signal bus 220 and a blue (hereinafter abbreviated as "B") display digital signal bus 230. The DAC 3 thus outputs analog values corresponding to digital R, G and B values to an R-display analog signal line 310, a G-display analog signal line 320 and a B-display analog signal line 330. The CRT 4 displays the data at a location thereof designated by the control signal 501 with intensities specified by the analog values from the R-signal line 310, G-signal line 320 and B-signal line 330, that is, in a color designated by the color data.

FIG. 2 particularly shows the color look-up table 2 and DAC 3 of the display system of FIG. 1 where the display system is constructed such that it can display 256 colors out of a total ot 262,144 colors at a time. Construction and operation of the color look-up table 2 will be described below with reference to FIG. 2.

Data transmitted over the pixel data bus 103 have an 8 bit width and are inputted as address data to designate an address of an R-memory array 211, a G-memory array 221 and a B-memory array 231 into which R-data-, G-data and B-data are to be stored, respectively. To this end, each memory array has a capacity of 256 (= 2^8) words. Each memory array further has a 6 bit width per word, and consequently, a combination of a total of 18 bits is provided for each address, which enables selection of a color out of a total of 262,144 (= $2^6 \times 2^6 \times 2^6$) different colors.

With the construction described above, simultaneous display of 256 colors out of the 262,144 colors can be realized.

It is assumed here that color data of 12 (001100B in binary number: the unit B will hereinafter denote a binary number), 21 (010101B) and 42 (101010B) are stored in advance in the 128th (80H in hexadecimal number: the unit H will hereinafter denote a hexadecimal number) addresses of the R-memory array 211, G-memory array 221 and B-memory array 231, respectively, as shown in Fig. 2 from the CPU 6 over the address buss 201 and data bus 202. In this instance, in case the display data on the pixel data bus 103 is 128 (80H), color data of 12 (001100B), 21 (010101B) and 42 (101010B) are outputted to the

R-display digital signal bus 210, G-display digital signal bus 220 and B-display digital signal bus 230, respectively. An R-DAC 311, a G-DAC 321 and a B-DAC 331 are each constructed to output an analog value corresponding to a digital value received. If it is assumed that each of the R-DAC 311, G-DAC 321 and B-DAC 331 outputs a voltage (0 to 1 volt) proportional to a digital value, then in the present case, the R-DAC 311, G-DAC 321 and B-DAC 331 will output 0.19 volts (= 12/63 volts), 0.33 volts (= 21 63 volts) and 0.67 volts (42/63 volts) to the R-display analog signal line 310, G-display analog signal line 320 and B-display analog signal line 330, respectively.

If color data all equal to 0 are written into the 128th addresses of the memory arrays 211, 221 and 231, then each of the DACs 311, 321 and 331 outputs 0 (zero) volt by the operation described above, and consequently, black is displayed on the CRT 4 described hereinabove with reference to FIG. 1. To the contrary, if color data all equal to 63 (111111B) are written into the same 128th addresses of the memory arrays 211, 221 and 231, then each of the DACs 311, 321 and 331 outputs 1 volt, and consequently, white is displayed on the CRT 4. In this manner, a color to be displayed on the CRT 4 can be changed very rapidly only by changing color data in the color look-up table 2.

The number of displayable colors can be increased remarkably only by increasing the bit width of a color look-up table as described above. IMSG171 by Inmos Limited is known as an integrated circuit device in which such a color look-up table and DACs as described hereinabove with reference to FIG. 2 are integrated, and one of known data processing systems which employ such integrated circuit device is a personal computer PS/2 by International Business Machines Corporation.

However, no particular attention is paid to the compatibility of such conventional display systems which employ a CRT as described above with a display system which employs, in place of a CRT, a display unit which is restricted in number of display colors or number of display gray scales such as a liquid crystal display device (hereinafter abbreviated as "LCD") or a plasma display panel (hereinafter abbreviated as "PDP"). Accordingly, such conventional display systems as described above have the following problems.

Of such display units listed above, description will be given, for example, of an LCD having a 16 color display function which can be anticipated to be manufactured as a product in several years. Since such LCD presents a 16 color display, a display signal to be inputted requires a data capacity of 4 bits (2^4 = 16) for each picture element. While the conventional display system described hereinabove converts color data of 18 bits of the color look-up table into three R, G and B analog signals using the DACs, where such an LCD as described above is employed as the display unit, an analog-to-digital converter (hereinafter abbreviated as "ADC") is additionally required, which makes a superfluous construction. Thus, it is also possible to employ a modification to the conventional display system wherein the DACs are removed and instead some measure for converting an output of 18 bits of the color look-up table into data of 4 bits is connected to the LCD. With the modification, a data capacity of 4 bits is basically sufficient. However, the color look-up table having an up to 18 bit width must be read out at the same speed as the displaying speed, and accordingly, it is required for the product to have a high performance.

Another modification may be employed wherein the color look-up table has a 4-bit width. The modification, however, is disadvantageous in that it cannot assure a compatibility with the function of such a conventional display system as described hereinabove that color data of 18 bits of the color look-up table can be written into and read out from the CPU.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a display system wherein a display unit having a comparatively small number of display colors or display gray scales is employed which has a sufficient compatibility with a conventional display system which employs a display unit having a comparatively large number of display colors or display gray scales.

The above object is accomplished according to the present invention by providing a display system which comprises a first memory for storing therein data to be displayed, a data source for supplying first color data which specify a color or a gray scale of the data to be displayed, a display unit having a number of displayable colors or displayable gray scales smaller than the number of colors or gray scales which can be specified by the first color data, a color data conversion circuit for converting the first color data supplied from the data source into second color data which specify one of the colors or the gray scales which can be displayed by the display unit, a second memory for storing therein the first color data supplied from the data source, and a third memory for storing therein the second color data supplied from the color data conversion circuit, the display unit displaying thereon the data read out from the first memory in the color or the gray scale specified by the second

color data read out from the third memory.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. 1 is a block diagram showing a conventional display system;

FIG. 2 is a block diagram showing a color look-up table and DACs of the display system shown in FIG. 1;

FIG. 3 is a block diagram of a display system showing an embodiment of the present invention;

FIG. 4 is a block diagram showing an exemplary color look-up table which is employed in the display system of FIG. 3;

FIG. 5 is a detailed block diagram of the color look-up table shown in FIG. 4 during a data writing operation;

FIGs. 6A and 6B are views showing an HSV color model, wherein FIG. 6A is a plan view of the HSV color model and FIG. 6B is a perspective view of the HSV color model;

FIGs. 7A , 7B, 7C and 7D are views illustrating 16 colors plotted on the HSV color model, wherein FIG. 7A is a plan view of the HSV color model, FIG. 7B is a sectional view taken along line VIIB-VIIB of FIG. 7A, FIG. 7C is a sectional view taken along line VIIC-VIIC of FIG. 7A, and FIG. 7D is a sectional view taken along line VIID-VIID of FIG. 7A;

FIGs. 8A, 8B, 8C and 8D are views illustrating an example of division of the HSV color model which is employed in the present invention, wherein FIG. 8A is a plan view of the HSV color model, FIG. 8B is a sectional view taken along line VIIIB-VIIIB of FIG. 8A, FIG. 8C is a sectional view taken along line VIIIC-VIIIC of FIG. 8A, and FIG. 8D is a sectional view taken along line VIIID-VIIID of FIG. 8A;

FIG. 9 is a detailed block diagram of the color look-up table shown in FIG. 4 during a data reading operation;

FIG. 10 is a block diagram showing part of another color look-up table which can be employed in the display system of the present invention;

FIG. 11 is a timing chart illustrating operation of the color look-up table shown in FIG. 10;

FIG. 12 is a block diagram showing part of a further color look-up table which can be employed in the display system of the present invention;

FIG. 13 is a timing chart illustrating operation of the color look-up table shown in FIG. 12; and

FIG. 14 is a block diagram of a display system showing another embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring first to FIG. 3, there is shown a display system according to an embodiment of the present invention. The display system shown includes a video RAM 1, a controller 5 and a CPU 6 which have the same functions with those of the conventional display system described hereinabove with reference to FIG. 1. The CPU 6 writes display data over a data bus 102 into an address of the video RAM 1 designated by address data received over an address bus 101. The display system further includes a color look-up table 8 which is constructed to control an LCD 7 which is capable of displaying 16 colors thereon in accordance the present invention. Color data from the CPU 6 are written over another data bus 202 into an address of the color look-up table 8 designated by address data received over another address bus 201. The color look-up table 8 of the display system shown in FIG. 3 corresponds to the color look-up table 2 of the display system shown in FIG. 1. Such corresponding relationship is attained by provision of the color look-up table 8 with an interface circuit which absorbs any possible differences between the video RAM 1 and the color look-up table 8 and/or between the CPU 6 and the color look-up table 8. Display data stored in the video RAM 1 are read out in response to a control signal 501 from the controller 5 and outputted to a pixel data bus 103. The color look-up table 8 has color data stored in advance therein as described hereinabove, and the display data outputted to the pixel data bus 103 are thus used as data of an address for referring to the color look-up table 8. Data read out from the color look-up table 8 in response to the address data are outputted to a display bus 801. The LCD 7 thus displays the received data at a location thereof designated by the control signal 501 in a color specified by the data received over the display bus 801.

FIG. 4 shows an internal structure of the color look-up table 8 according to the present invention. The color look-up table 8 shown includes a color look-up table 81 for CPU, a color look-up table 82 for display, a pair of table write circuits 83 and 84, a color data converter 85, a table readout circuit 86, and an interface circuit 87. Interfaces to the outside include the pixel data bus 103, address bus 201, data bus 202 and display bus 801, and they individually have such functions as described hereinabove. The interface circuit 87 is constructed to absorb possible differences in timings of signals, polarities or the like of the color look-up table 8 according to the present invention from the color look-up table 2 of the conventional system described hereinabove so that the color look-up table

8 may be equivalent to the table 2 of the conventional system when it is seen from the outside.

Operation of the color look-up table 8 will be described particularly below under the assumption that the color look-up table 8 in the present embodiment has a sufficient compatibility with IMSG 171 by Inmos Limited.

Referring now to FIG. 5, there is shown in detail only that part of the color look-up table 8 which relates to writing operation from the CPU 6 into the color look-up table 8 in order to facilitate understandings of such writing operation. The color look-up table 8 thus includes the same table write circuits 83 and 84, color look-up table 81 for CPU, color data converter 85 and so forth as those shown in FIG. 4. An address bus 871 from the interface circuit 87 of FIG. 4 is connected to a decoder 891. When color data are to be written into the color look-up table 8, the CPU 6 precedently writes into an address latch 893 data of an address to which information is to be stored. In particular, if data representative of an address of the address latch 893 are inputted to the decoder 891 over the address bus 871, then an address latch writing signal 892 is outputted from the decoder 891, and during a duration or period of such output, address data transmitted over a data bus 872 are latched into the address latch 893. Then, color data are outputted to the data bus 872 while the data write address is inputted to the decoder 891 over the address bus 871. Consequently, a data write signal 894 is developed from the decoder 891 and transmitted to a write signal generator 895. As a result, the write signal generator 895 at first outputs an R-write signal 835 so that color data on the data bus 872 are written into an R-table 812 in the color look-up table 81 for CPU and an R-latch 815. It is to be noted that the address of the R-table 812 then is specified by the address data in the address latch 893 mentioned hereinabove. In subsequent color data writing operation, another data write signal 894 is produced similarly from the decoder 891 and transmitted to the write signal generator 895. Consequently, a G-write signal 836 is developed from the write signal generator 895, and in response to such G-write signal 836, color data on the data bus 872 are written into a G-table 813 and a G-latch 816. The address of the G-table 813 is specified by the address data in the address latch 893. In third color data writing operation, a B-write signal 837 is developed from the write signal generator 895, and color data are written into a B-table 814 and a B-latch 817. The color data written into the R-latch 815, G-latch 816 and B-latch 817 in this manner are outputted to an R-latch output bus 818, a G-latch output bus 819 and a B-latch output bus 820, respectively, and transmitted to the color data converter 85 over a color bus 832. The color data converter 85 is constructed to modify color data so that they may represent one of a number of colors which can be displayed by the relevant display unit. In the case of the display system of the present embodiment, for example, since the display unit is an LCD on which up to 16 different colors can be displayed, the color data converter 85 should be constructed to convert received color data into data of 4 bits. Meanwhile, color data to be inputted to the color data converter 85 should be data of 18 bits so that the color look-up table 8 may have a sufficient compatibility with IMSG171 by Inmos Limited. Thus, the color data converter 85 converts color data of 18 bits into data of 4 bits and outputs the thus converted data of 4 bits to a converted color bus 851. Thereupon, the write signal generator 895 detects completion of the R, G and B color data writing operations into the color look-up table 81 for CPU and develops a display table write signal 834. Such display table write signal 834 acts upon the table write circuit 84, and during the time, address data of the address latch 893 are transferred as data of an address of the color look-up table 82 to a display table address bus 841 over the address bus 831 in place of connection of the pixel data bus 873 to the display table address bus 841. The display table write signal 834 acts also upon the color look-up table 82 for display so that color data obtained from the color data converter 85 are written into a location of the address designated by the address data in the address latch 893.

Here, an example of method of conversion of color data executed by the color data converter 85 will be described in detail.

In the field of the computer graphics, an HSV color model is used commonly as a model of quantitative representation of a color. The model is represented by an inverted cone as shown in FIGs. 6A and 6B. In the model, a color is represented with a hue (H), a saturation (S) and a value (V). Hues are defined as angles around a center axis of the cone (the vertical axis) as starting from red at zero degrees and progressing counterclockwise. The value (V) of a color is defined as a distance along the vertical axis from black (V = 0) to white (V = 1). The saturation (S) of a color is defined as a distance from the value axis (S = 0) radially toward the surface of the cone. Colors on the value axis itself (where S = 0) are shades of gray. Pure hues are found at the edge of the cone where S = 1 and V = 1. All colors can be plotted in the cone.

An RGB model is employed most popularly to represent a particular color quantitatively. The transformation algorithm for representing a oolor represented in such RGB model in the HSV model. that is, the algorithm for converting R, G and B values into H, S and V values, is such as follows:

Normalize R, G and B values as
$0 \leq R, G, B \leq 1$
set
MAX = maximum of R, G, B
MIN = minimum of R, G, B
d = MAX - MIN
V = MAX
if d is nonzero, set
S = d/MAX
for d = 0, set S = 0 and H = undefined and return these values. Otherwise,
r = (MAX - R)/d
g = (MAX - G)/d
b = (MAX - B)/d
if R = Max then set h = b - g
if G = MAX then set h = r - b + 2
if B = MAX then set h = g - r + 4
if h < 0, set H = 60 x h + 360
if h > 0, set H = 60 x h

The HSV color model and transformation algorithms between RGB and HSV are described in detail in Lee Baldwin, "Color Considerations", Byte, September 1984, pp. 227-228, 230, 232, 234-235, 238, 240, 243-244 and 246.

In the present embodiment, the color data converter 85 converts color data of a total of 18 bits including 6 bits for each of R, G and B for one picture element supplied over the color bus 832 into different color data of a total of 4 bits including one bit for each of I (intensity), R, G and B for one picture element. In other words, the color data converter 85 converts 262,144 colors into 16 colors which can be displayed on the LCD 7. It is important in the conversion that one of the 16 colors which is most approximate to a color inputted to the color data converter 85 should be outputted from the color data converter 85. The HSV color model described hereinabove is used for such approximation.

FIGs. 7A, 7B, 7C and 7D illustrate plots on the aforementioned HSV color model of 16 colors which are commonly displayed by an ordinary personal computer. Each of the 16 colors can be represented by a code of 4 bits of I, R, G and B. Such codes are, for example, black 0000, dark gray 1000, light gray 0111, dark blue 0001, dark green 0010, dark cyan 0011, dark red 0100, dark magenta 0101, dark yellow 0110, light blue 1001, light green 1010, light cyan 1011, light red 1100, light magenta 1101, light yellow 1110 and white 1111.

In the present embodiment, the HSV color model is divided into 16 blocks as indicated by broken lines in FIGs. 8A, 8B, 8C and 8D such that each of the blocks may contain one of the 16 points which are plotted on the HSV color model shown in FIGs. 7A to 7D and represent such 16 colors as described above. It is determined that any and all colors included in each of the 16 blocks are represented by the aforementioned point contained in the block. The color data converter 85 determines H, S and V values from received color data including 6 bits for each of R, G and B using the conversion algorithm from RGB into HSV described hereinabove, determines from the H, S and V values to which one of the aforementioned 16 blocks the color should belong, and outputs color data of 4 bits representative of the point which is contained in the block and represents the block. The color data of 4 bits outputted from the color data converter 85 are written into the color look-up table 82 for display.

Such conversion can be made decisively by the aforementioned conversion algorithm from RGB into HSV only if divisional boundaries of the HSV color model shown in FIGs. 8A to 8D are decided. Accordingly, the color data converter 85 can be constructed from a logic circuit including a logical AND circuit and a logical OR circuit. (An application for a patent for such method of conversion of color data has been filed in Japan by three of the inventors of the present invention: Japanese Patent Application No. 63-134214, filed on May 31, 1988.)

As described above, a writing operation of color data of R, G and B into the color look-up table 8 can realize writing into the color look-up table 82 for display in addition to writing into the color look-up table 81 for CPU. The color data written in the color look-up table 82 are outputted to the display bus 801 at the same time with such writing. Meanwhile, since the pixel data bus 873 is used for transmission of data of an address of the color look-up table 82 for display except during such writing operation as described above, display data coincident with display data outputted to the pixel data bus 103 are outputted to the display bus 801 as shown in FIG. 3. Accordingly, data are displayed on the LCD 7 in a color designated by color data outputted from the color look-up table 82 for display.

Subsequently, reading operation with respect to the writing operation of color data described above will be described with reference to FIG. 9. FIG. 9 particularly shows only that part of the color look-up table 8 which relates to reading operation similarly to FIG. 5. The color look-up table 8 thus includes the same table readout circuit 86 and color look-up table 81 for CPU as those shown in FIG. 4. Similarly to the color data writing operation described hereinabove, when color data are to be read out from the color look-up table 8, the CPU 6 precedently writes into an address latch 864 data of an address from which information is to be read out. In particular, if data representative of an address of the address latch 864 are inputted to a decoder 862 over the address bus 871, then an

address latch writing signal 863 is outputted from the decoder 862, and during a duration of such output, address data transmitted over the data bus 872 are latched into the address latch 864. Then, if data of an address from which display data are to be read out are inputted to the decoder 862 over the address bus 871, then a data readout signal 865 is developed from the decoder 862 and transmitted to a readout signal generator 866. As a result, the readout signal generator 866 at first outputs a select signal 867 to a selector 868 so as to select an R-data bus 881 of the R-table 812. Meanwhile, the address of the R-table 812, that is, the address of the color look-up table 81 for CPU, is provided over a table address bus 884 in conformity with address data which has been written into the address latch 864 immediately before then. As a result of such operation, the color data stored in the R-table 812 are outputted to the R-data bus 881 and then to a data bus 861 by way of the selector 868. In subsequent color data readout operation, another data readout signal is produced similarly from the decoder 862 and transmitted to the readout signal generator 866. Consequently, another select signal 867 is outputted to the selector 868 so as to select a G-data bus 882. Data of the address transmitted to the G-table 813 coincide with the address data stored in the address latch 864 similarly as in the case of the R-table 812. Through the operation, color data stored in the G-table 813 is outputted to the data bus 861 by way of the G-data bus 882 and the selector 868. In further subsequent color data readout operation, a further select signal 867 is developed from the readout signal generator 866 to the selector 868 so as to select a B-data bus 883. Consequently, color data of the B-table 814 are outputted to the data bus 861 by way of the B-data bus 883 and the selector 868.

As described above, by three times of color data readout operation including writing of address data into the address latch 864, color data of a total of 18 bits including 6 bits for each of R, G and B can be read out from the color look-up table 81 for CPU, that is, the color look-up table 8 shown in FIG. 3.

According to the present embodiment described above, color data written in the color look-up table can be read out accurately due to provision of the color look-up table 81 for CPU, and a color on the display unit can be changed during writing operation of color data due to provision of the color look-up table 82 for display. Further, due to provision of the color data converter 85 at the preceding stage to the color look-up table 82 for display, the bit width of the color look-up table 82 for display can be reduced, and the circuit portion which requires the same speed of operation as the display speed is reduced to such color look-up table 82 for display. In addition, due to provision of the interface circuit 87, such a conventional color look-up table as described hereinabove can be replaced by the color look-up table of the present invention without any modification to the interfaces of the conventional color look-up table 2 to the video RAM 1, CPU 6 and controller 5. While the present embodiment has been described by way of an example of a color look-up table which may replace IMSG171 by Inmos Limited, the object of the present invention can naturally be attained with any other color look-up table although there is some difference in procedure of writing/readout operation of color data.

Further, while in the present embodiment the display unit is described being an LCD which can display 16 colors thereon, the present invention can naturally be applied to any display unit having a smaller number of displayable colors or displayable gray scales than a basic display unit, such as, for example, a PDP, an electroluminescence panel or a CRT.

FIG. 10 shows another embodiment of the present invention. In FIG. 10, only the color look-up table 82 for display of the color look-up table 8 shown in FIG. 4 and components around the same are shown. The display system of the present embodiment is different from the display system of the preceding embodiment only in that a latch 91 for storing color data therein is provided at the output stage of the color look-up table 82 for display and a latch signal 838 is supplied from the table write circuit 83 to the latch 91. FIG. 11 is a timing chart illustrating operation of the display system shown in FIG. 10, and reference numerals on the left-hand side in FIG. 11 denote the same reference numerals of the buses and signal lines shown in FIG. 10. For a period of time while the same display continues, display data inputted over the pixel data bus 873 are inputted to the table write circuit 84 and then to the color look-up table 82 for display by way of the display table address bus 841. The color look-up table 82 for display outputs color data to the display bus 821 in response to address data received thereby. The latch 91 is constructed to output an input signal thereto as it is unless a latch signal 838 is inputted thereto. Accordingly, color data outputted from the display bus 821 are outputted as they are from the latch 91 into the display bus 801 and thus transferred to the display unit. By the operation, display data P2 on the pixel data bus 873 shown in FIG. 11 are transmitted over the display table address bus 841 and make color data D2 on the display bus 821, which are outputted into the display bus 801. Subsequently, operation of writing color data into the color look-up table 82 for display will be described.

If data WA of a write address are outputted to the address bus 831 while write data WD are outputted to the data bus 851, then the table write circuit 83 outputs a display table write signal 834 in synchronism with the pixel data bus 873 as illustrated in FIG. 11. While the signal 834 continues to be received, the table write circuit 84 outputs the address data WA on the address bus 831 to the display table address bus 841. The display table 82 writes the write data WD on the data bus 851 in synchronism with the display table write signal 834 to an address thereof designated by the write address data WA. Meanwhile, the table write circuit 83 outputs a latch signal 838 to the latch 91 so as to latch data D0 immediately before such writing operation. Since the latch 91 maintains the data while the latch signal 838 continues to be received, it outputs D0 into the display bus 801 also during a writing operation. In particular, during a writing operation, data WD outputted to the display bus 821 but having no relation to display are not outputted to the display bus 801 nor transferred to the display unit.

As described above, according to the present embodiment, data having no relation to display are prevented from being transferred to the display unit due to provision at the output stage of the display table 82 of the latch 91 for storing therein color data which have been read out immediately before a writing period. Consequently, flickering of a display screen is reduced.

A further embodiment of the present invention will be described below with reference to FIGs. 12 and 13. The display system of the present embodiment can prevent flickering of a display screen during writing of color data into a color look-up table. The display system shown in FIG. 12 is different from the display system shown in FIG. 4 only in that the display table 82 of the color look-up table 8 is composed of a first color look-up table 935 for display and a second color look-up table 945 for display and that it further includes a table selector 922 for selecting either one of the two tables 935 and 945 and a delayed write circuit 92 for writing, upon writing of color data into the display table 82, color data at different timings into the two display tables 935 and 945. FIG. 13 illustrates flows of address data and color data around the display tables shown in FIG. 12, and operation of the display system shown in FIG. 12 will be described subsequently with reference to FIG. 13. During a display period, P0, P1, P2, P3 and P4 on the pixel data bus 873 are successively outputted to address buses 938 and 948 by way of address selectors 930 and 940, respectively. Latches 932 and 942 alternately latch the display data in response to latch signals 933 and 943 generated by a timing generator 921. In the display system of the present embodiment, even-numbered ones of the display data such as P0, P2, P4 and so forth are latched by the latch 942 connecting to the second display table 945 while odd-numbered ones of the display data such as P1, P3 and so forth are latched by the latch 932 connecting to the first display table 935. The first display table 935 outputs odd-numbered color data D1 and D3 Into a display bus 936 in response to the address data received. On the other hand, the second display table 945 outputs even-numbered color data D0, D2 and D4 to a display bus 946 in response to the address data received. The table selector 922 alternately selects the display bus 936 and the display bus 946 in response to a select signal 923 generated by the timing generator 921 and successively outputs the color data D0, D1, D2 and D3 in this order. As can be readily understood from the foregoing description, the relationship between the pixel data bus 873 and the display bus 801 is similar to that in any of the preceding embodiments. To the contrary, upon writing of color data, write address data WA are outputted to the address bus 831 while write data WD are outputted to the data bus 851. The timing generator 921 generates a signal such that writing operation may be performed on one of the display tables which is not selected by the table selector 922. As seen from FIG. 13, when writing operation is to be performed on the first display table 935, the timing generator 921 outputs an address select signal 931 to the address selector 930 so as to select the address bus 831 while it outputs a latch signal 933 to the latch 932 so that the latch 932 may latch write address data WA. Thus, write address data WA are transmitted to the first display table 935 over the address bus 934 while write data WD are transmitted to the first display table 935 over the data bus 851, and a table write signal 937 is developed from the timing generator 921 in order to perform a writing operation of the color data. While the write data WD are outputted to the display bus 936 during such operation, since the other display bus 946 is selected by the table selector 922, the write data WD are prevented from being outputted to the display bus 801 and correct color data D2 for the period can be transferred to the display unit. After completion of such writing operation into the first display table 935 as described above, another writing operation into the second display table 945 is executed subsequently. The writing operation is similar to the writing operation into the first display table 935. In particular, the timing generator 921 outputs an address select signal 941 to the address selector 940 so as to select the address bus 831 while it outputs a latch signal 943 to the latch 942 so that the latch 942 may latch write address data WA. Thus, write address data WA and write

data WD are transmitted to the second display table 945 while a table write signal 947 is transmitted from the timing generator 921 to the second display table 945 so as to perform a writing operation of the color data. During such operation, the write data WD which is no relation to display are outputted to the display bus 946 similarly as in the writing operation into the first display table 935, but since the table selector 922 selects the display bus 936, correct color data D3 for the period can be outputted into the display bus 801.

As described above, in the display system of the present embodiment, flickering of a display screen upon writing of color data can be prevented and only a correct picture can be displayed due to provision of the plurality of display tables, the selector for successively selecting the plurality of display tables to send out to the display unit color data which are outputted from the selected display table, and the delayed write circuit for writing color data into another display table which is not selected by the selector. While the present embodiment employs the construction wherein the two display tables are alternately selected, it can naturally applied to another construction wherein an arbitrary plural number of display tables are selected successively or at random. It is an important operation in the display system of the present embodiment that a writing operation is performed for the display table which is not selected.

FIG. 14 shows a display system according to a still further embodiment of the present invention. The display system includes such a display unit having a large number of displayable colors or displayable gray scales as employed in the conventional display unit described hereinabove and another display unit having a smaller number of displayable colors or displayable gray scales and selects either one or both of the two display units for making a display thereon. The display system of the present embodiment includes the same color look-up table 2, DAC 3 and CRT 4 as those shown in FIG. 1 and further includes the same LCD 7 as that of the display system shown in FIG. 3. The display system further includes the same video RAM 1, controller 5 and CPU 4 as those shown in FIG. 1 or 3. The display system further includes a color look-up table 97. The color look-up table 97 has a substantially same function as any of the color look-up tables included in the display systems of the preceding embodiments of the present invention described hereinabove except that it additionally includes a readout inhibit circuit 95 for inhibiting the CPU 6 from reading out color data from the color look-up table 97 and a display inhibit circuit 96 for inhibiting outputting of color data to the display bus 801. Accordingly, further detailed description of the internal structure of the color look-up table 97 will be omitted herein to avoid redundancy. Thus, display data read out from the video RAM 1 are inputted to the color look-up tables 2 and 97 over the pixel data bus 103. The color look-up tables 2 and 97 have display color data stored in advance from the CPU 6, and consequently, color data are read out from locations of the color look-up tables 2 and 97 at an address specified by the display data received. The color data read out from the color look-up tables 2 and 97 are transferred to the CRT 4 and the LCD 7, respectively. While writing of color data into the color look-up table 2 is executed from the CPU 6 using the address bus 201 and the data bus 202, writing into the color look-up table 97 is executed simultaneously in a parallel relationship with the color look-up table 2 because the color look-up table 97 of the present invention has a sufficient compatibility in external interface and operation with the conventional color look-up table 2 as described hereinabove in connection with the preceding embodiments. Subsequently, an operation of retrieving color data from the color look-up tables 2 and 97 into the CPU 6 will be described. The CPU 6 can read out stored color data from the color look-up table 2 using the address bus 201 and the data bus 202. However, since the other color look-up table 97 includes the readout inhibit circuit 95 therein, no data are outputted from the table 97 into the data bus 202. Accordingly, a possible contention between data is prevented, and coexistence of the two different color look-up tables 2 and 97 is realized. Further, where the display units, that is, the CRT 4 and LCD 7, are different from each other only in specifications of the horizontal frequency and the vertical frequency among various performances of them, flickering on the LCD or displacement of the display location can be prevented because transfer of display data to the LCD 7 can be inhibited by means of the display inhibit circuit 96. As described so far, according to the present embodiment, simultaneous display of two or more display units or very quick change-over between the display units can be realized without rewriting contents of the color look-up tables. Further, while in the present embodiment the two different color look-up tables are provided and one of them includes the readout inhibit circuit and the display inhibit means, the object of the present invention can be attained naturally even if an arbitrary number of color look-up tables are provided and an arbitrary number of readout inhibit circuits or display inhibit circuits are provided in an arbitrary number of color look-up tables.

According to the present invention, since a color look-up table for exclusive use with a CPU is provided in order to write color data sent out from the CPU into the same and read out written color

data from the same to be taken into the CPU, the compatibility on the software between the color look-up table and a conventional color look-up table can be maintained perfectly. Meanwhile, the capacity of a color look-up table for display can be reduced to a number equal to the number of displayable colors of a display unit, and devices which are required to make the same high speed operation as the display speed can be reduced. Therefore, according to the present invention, a color look-up table is provided which is suitable to be constructed as an integrated circuit. Thus, the color look-up table 8 which is composed of the various blocks shown in FIG. 4 can be formed as a single integrated circuit. Further, the color look-up table 97 which includes the readout inhibit circuit 95 and the display inhibit circuit 96 shown in FIG. 14 can also be formed as an integrated circuit. Besides, an integrated circuit of such color look-up table can readily replace an integrated circuit of a conventional color look-up table, and there is the possibility that a change in hardware may be made unnecessary.

Further, according to the present invention, flickering of a screen which may arise from writing of data into a color look-up table for display can be reduced very readily only by provision of a latch circuit at the output stage of the table.

Furthermore, according to the present invention, if a plurality of color look-up tables for display are provided, then flickering of a screen which may arise from writing of data into the tables can be eliminated.

In addition, according to the present invention, since a display system which includes a plurality of such color look-up tables as described hereinabove can be designed and produced, a plurality of display units which are different in number of displayable colors or displayable gray scales can be connected to a CPU without causing any trouble in access to the color look-up tables from the CPU, and data can be displayed simultaneously on the plurality of display units. Further, even when the display units do not make simultaneous display, color data can be written simultaneously into the plurality of color look-up tables. Accordingly, a change-over of display from one to another one of the display units can be made very rapidly without writing such data into the color look-up tables again.

Claims

1. A display system comprising:
first storage means (1) for storing therein data to be displayed;
a data source (202) for supplying first color data which specify a color or a gray scale of the data to be displayed;
color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify a color or a gray scale different from the color or the gray scale specified by the first color data;
second storage means (81) for storing therein the first color data supplied from said data source;
third storage means (82) for storing therein the second color data supplied from said color data conversion means; and
a display unit (7) for displaying thereon the data read out from said first storage means in the color or the gray scale specified by the second color data read out from said third storage means.

2. A display system according to claim 1, further comprising readout means (86) for reading out the first color data from said second storage means.

3. A display system according to claim 1, further comprising latch means (91) for latching therein the second color data read out from said third storage means, said latch means being adapted to latch therein during a period during which the second color data are written into said third storage means the second color data which have been read out from said third storage means immediately before the writing period and then supply the thus latched second color data to said display unit.

4. A display system comprising:
first storage means (1) for storing therein data to be displayed;
a data source (202) for supplying first color data which specify a color or a gray scale of the data to be displayed;
color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify a color or a gray scale different from the color or the gray scale specified by the first color data;
second storage means (81) for storing therein the first color data supplied from said data source;
a plurality of third storage means (935, 945) for storing therein the second color data supplied from said color data conversion means;
selective write means (92) for successively selecting any one of said plurality of third storage means and for writing the second color data supplied from said color data conversion means into a selected one of said plurality of third storage means;
selective readout means (922) for successively selecting any one of said third storage means which is not selected by said selective write means and for reading out the second color data from the selected one of said third storage means; and
a display unit (7) for displaying thereon the data

read out from said first storage means in the color or the gray scale specified by the second color data supplied from said selective readout means.

5. A display system according to claim 4, further comprising readout means (86) for reading out the first color data from said second storage means.

6. A display system according to claim 4, wherein said plurality of third storage means are two storage means (935, 945), and said selective write means alternately selects said two storage means (935, 945) while said selective readout means selects the other one of said two storage means (935, 945) which is not currently selected by said selective write means.

7. A display system comprising:
first storage means (1) for storing therein data to be displayed;
a data source (202) for supplying first color data which specify a color or a gray scale of the data to be displayed;
a display unit (7) having a number of displayable colors or displayable gray scales smaller than the number of colors or gray scales which can be specified by the first color data;
color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify one of the colors or the gray scales which can be displayed by said display unit;
second storage means (81) for storing therein the first color data supplied from said data source; and
third storage means (82) for storing therein the second color data supplied from said color data conversion means;
said display unit displaying thereon the data read out from said first storage means in the color or the gray scale specified by the second color data read out from said third storage means.

8. A display system according to claim 7, further comprising readout means (86) for reading out the first color data from said second storage means.

9. A display system according to claim 7, further comprising latch means (91) for latching therein the second color data read out from said third storage means, said latch means being adapted to latch therein during a period during which the second color data are written into said third storage means the second color data which have been read out from said third storage means immediately before the writing period and then supply the thus latched second color data to said display unit.

10. A display system comprising:
first storage means (1) for storing therein data tc be displayed;
a data source (202) for supplying first color data which specify a color or a gray scale of the data to be displayed;
a display unit (7) having a number of displayable colors or displayable gray scales smaller than the number of colors or gray scales which can be specified by the first color data;
color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify one of the colors or the gray scales which can be displayed by said display unit;
second storage means (81) for storing therein the first color data supplied from said data source;
a plurality of third storage means (935, 945) for storing therein the second color data supplied from said color data conversion means;
selective write means (92) for successively selecting any one of said plurality of third storage means and for writing the second color data supplied from said color data conversion means into a selected one of said plurality of third storage means; and
selective readout means (922) for successively selecting any one of said third storage means which is not selected by said selective write means and for reading out the second color data from the selected one of said third storage means;
said display unit displaying thereon the data read out from said first storage means in the color or the gray scale specified by the second color data supplied from said selective readout means.

11. A display system according to claim 10, further comprising readout means (86) for reading out the first color data from said second storage means.

12. A display system according to claim 10, wherein said plurality of third storage means are two storage means (935, 945), and said selective write means alternately selects said two storage means (935, 945) while said selective readout means selects the other one of said two storage means (935, 945) which is not currently selected by said selective write means.

13. An integrated circuit for use with a display system which includes first storage means (1) for storing therein data to be displayed, a data source (202) for supplying first display data which specify a color or a gray scale of the data to be displayed, and a display unit (7) having a number of displayable colors or displayable gray scales smaller than the number of colors or gray scales which can be specified by the first color data, comprising:
color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify one of the colors or the gray scales which can be displayed by said display unit;
second storage means (81) for storing therein the first color data supplied from said data source; and

third storage means (82) for storing therein the second color data supplied from said color data conversion means.

14. An integrated circuit according to claim 13, further comprising readout means (86) for reading out the first color data from said second storage means.

15. A display system comprising:

first storage means (1) for storing therein data to be displayed;

a data source (202) for supplying first color data which specify a color or a gray scale of the data to be displayed;

a first display unit (4) capable of displaying thereon the color or the gray scale specified by the first color data;

a second display unit (7) having a number of displayable colors or displayable gray scales smaller than the number of colors or gray scales which can be specified by the first color data;

an integrated circuit including color data conversion means (85) for converting the first color data supplied from said data source into second color data which specify one of the colors or the gray scales which can be displayed by said second display unit, second storage means (81) for storing therein the first color data supplied from said data source, and third storage means (82) for storing therein the second color data supplied from said color data conversion means; and

fourth storage means (2) for storing therein the first color data supplied from said data source;

wherein said first display unit displays thereon the data read out from said first storage means in the color or the gray scale specified by the first color data read out from said fourth storage means while said second display unit displays thereon the data read out from said first storage means in the color or the gray scale specified by the second color data read out from said third storage means.

16. A display system according to claim 15, further comprising readout inhibit means for setting said system so as to inhibit the first color data from being read out from said second storage means, and display inhibit means for setting said system so as to inhibit the second color data from being sent out to said second display unit.

FIG. 1

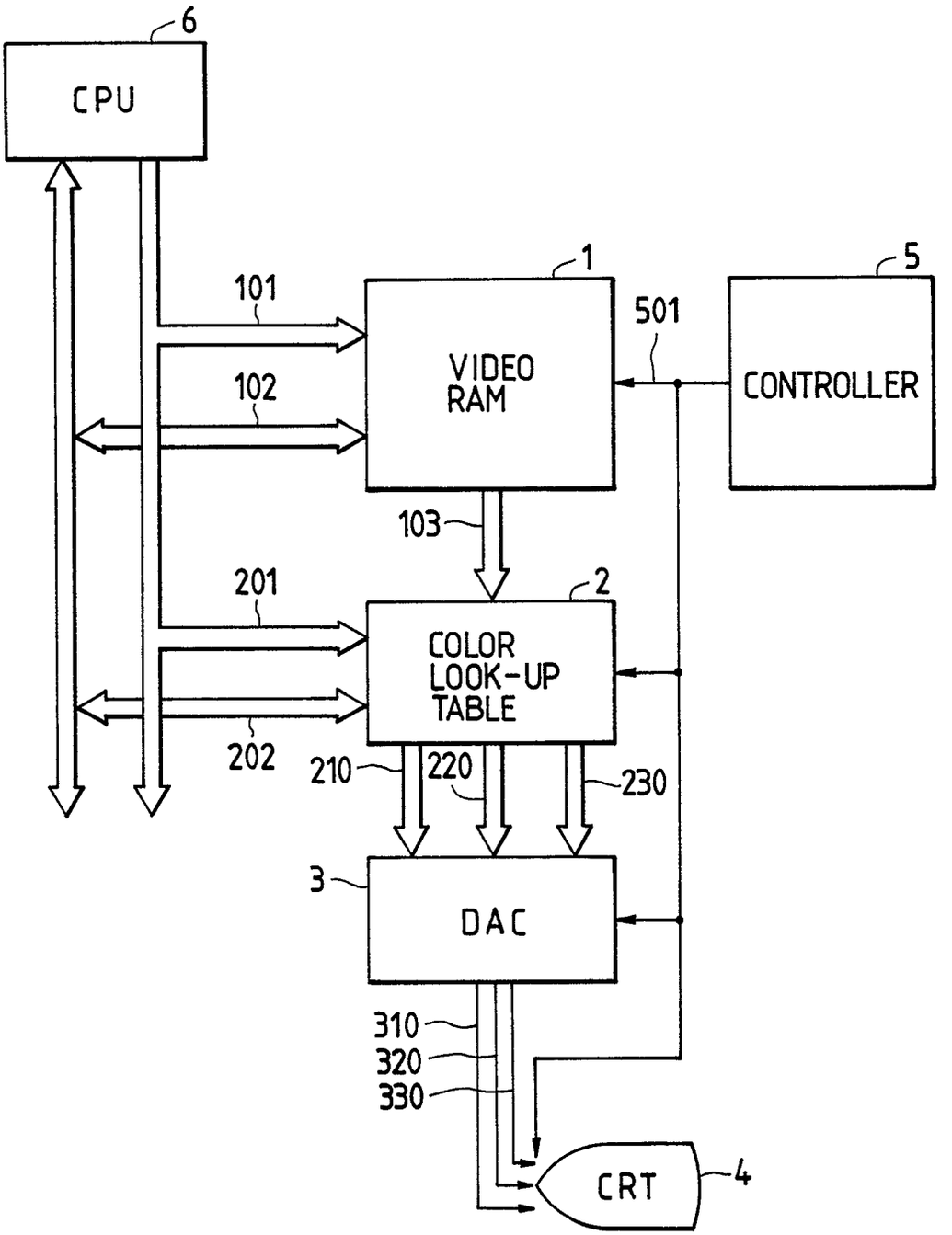

6
CPU
1
VIDEO RAM
5
CONTROLLER
501
101
102
103
201
202
2
COLOR LOOK-UP TABLE
210
220
230
3
DAC
310
320
330
CRT
4

FIG. 2

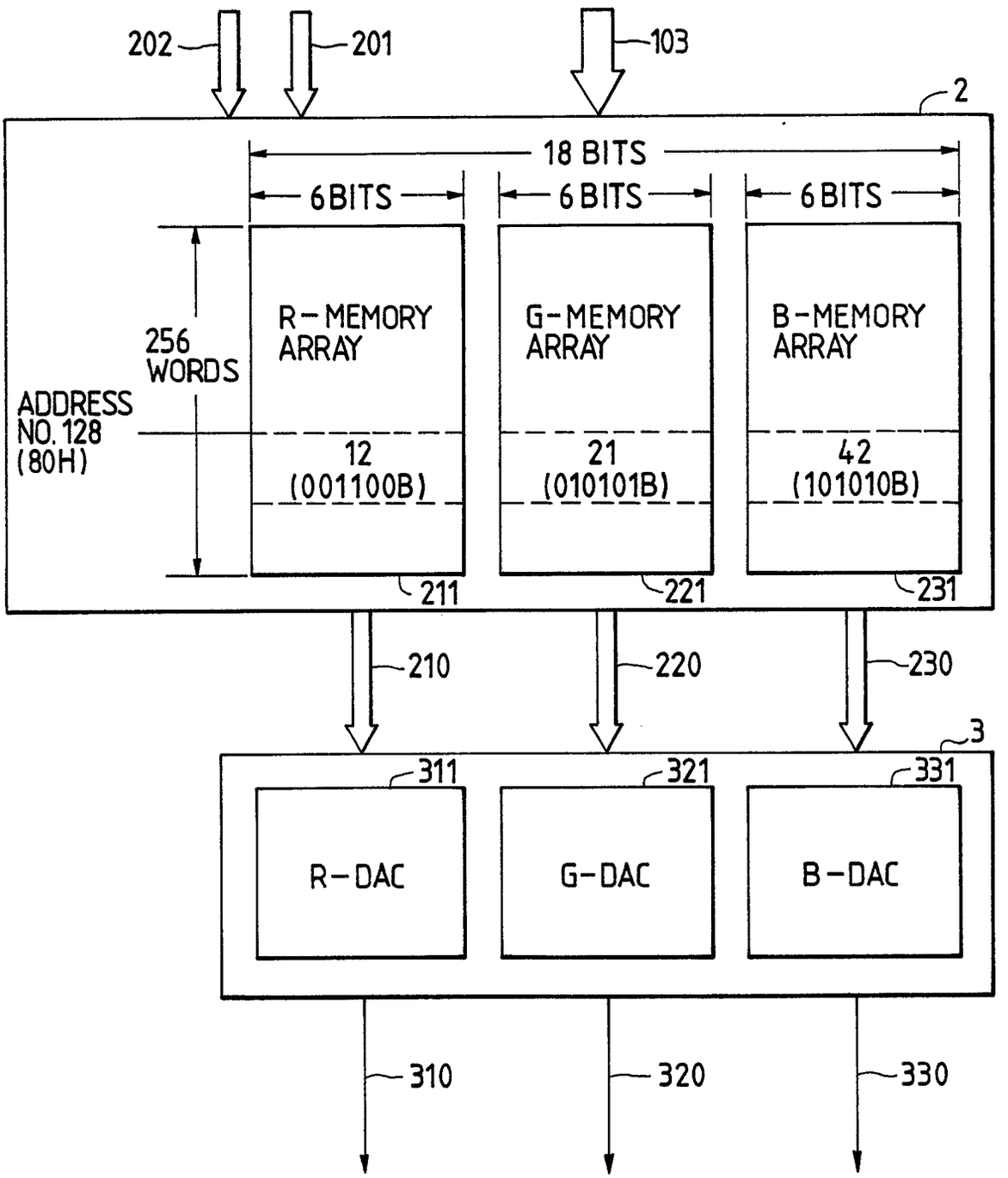

202
201
103
2
18 BITS
6 BITS
6 BITS
6 BITS
256 WORDS
ADDRESS NO. 128 (80H)
R-MEMORY ARRAY
G-MEMORY ARRAY
B-MEMORY ARRAY
12 (001100B)
21 (010101B)
42 (101010B)
211
221
231
210
220
230
3
311
321
331
R-DAC
G-DAC
B-DAC
310
320
330

FIG. 3

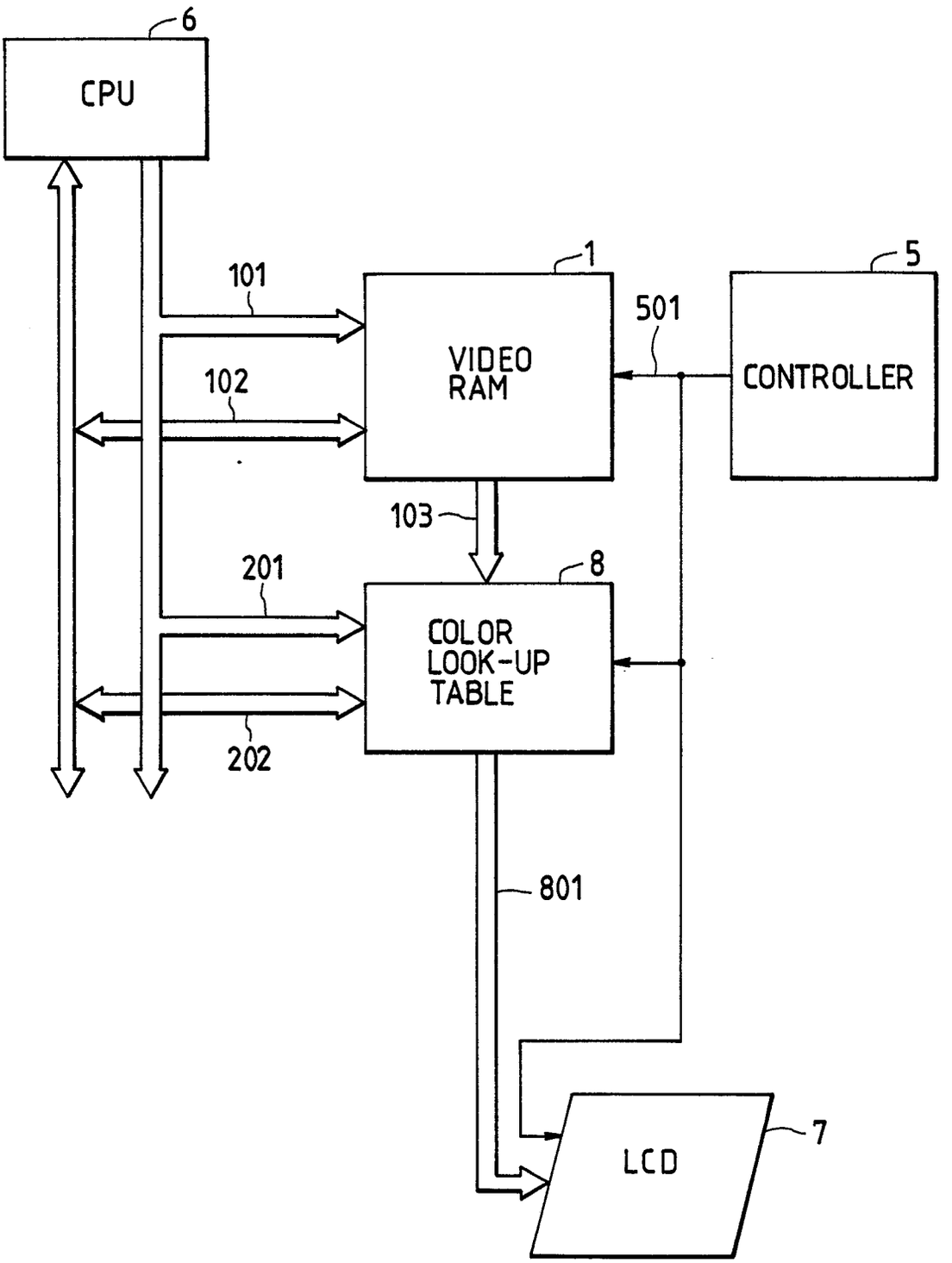

6
CPU
101
102
1
VIDEO RAM
501
5
CONTROLLER
103
201
8
COLOR LOOK-UP TABLE
202
801
LCD
7

FIG. 4

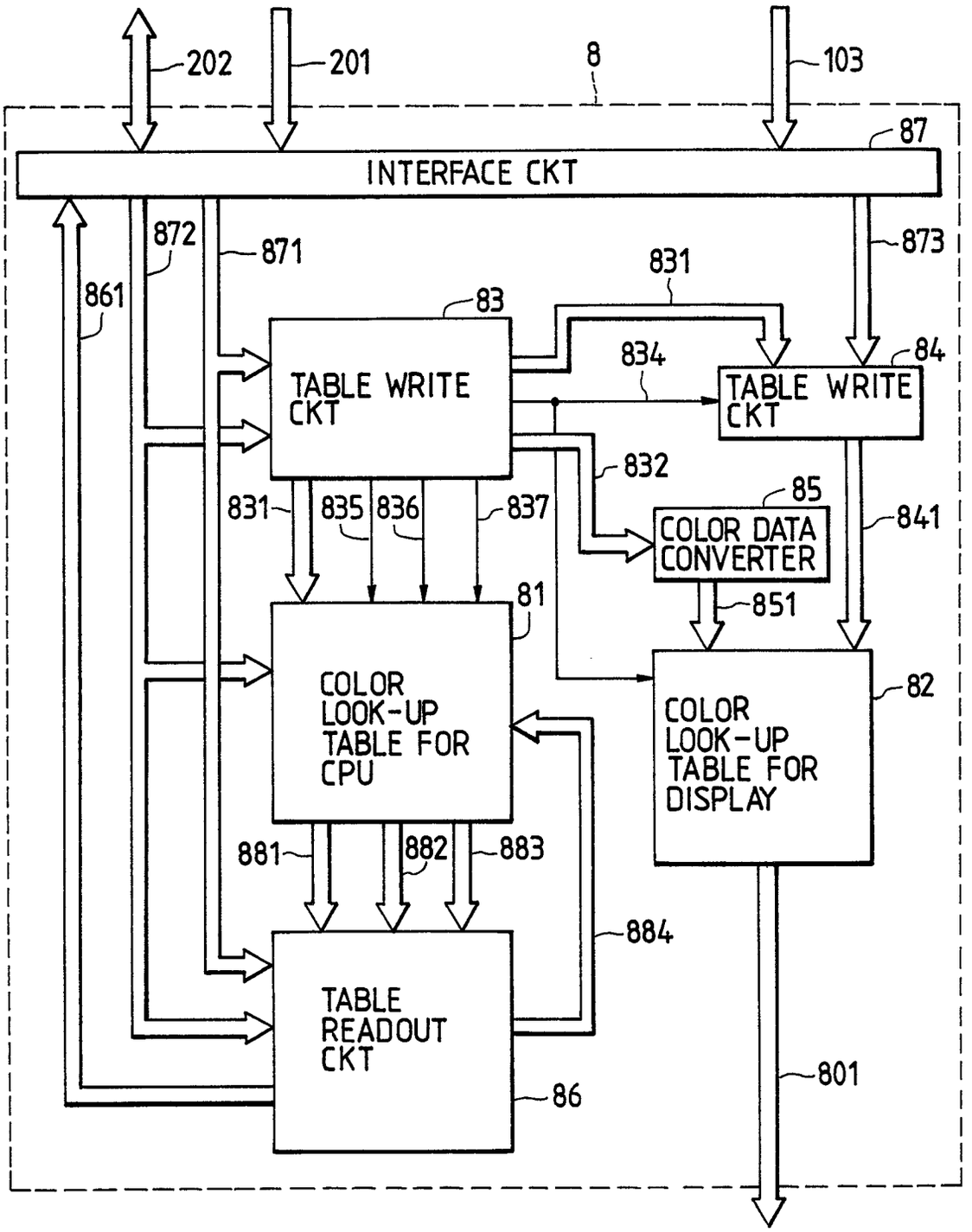

202
201
8
103
87
INTERFACE CKT
872
871
873
831
861
83
84
834
TABLE WRITE CKT
TABLE WRITE CKT
832
85
831
835
836
837
COLOR DATA CONVERTER
841
81
851
COLOR LOOK-UP TABLE FOR CPU
82
COLOR LOOK-UP TABLE FOR DISPLAY
881
882
883
884
TABLE READOUT CKT
86
801

FIG. 5

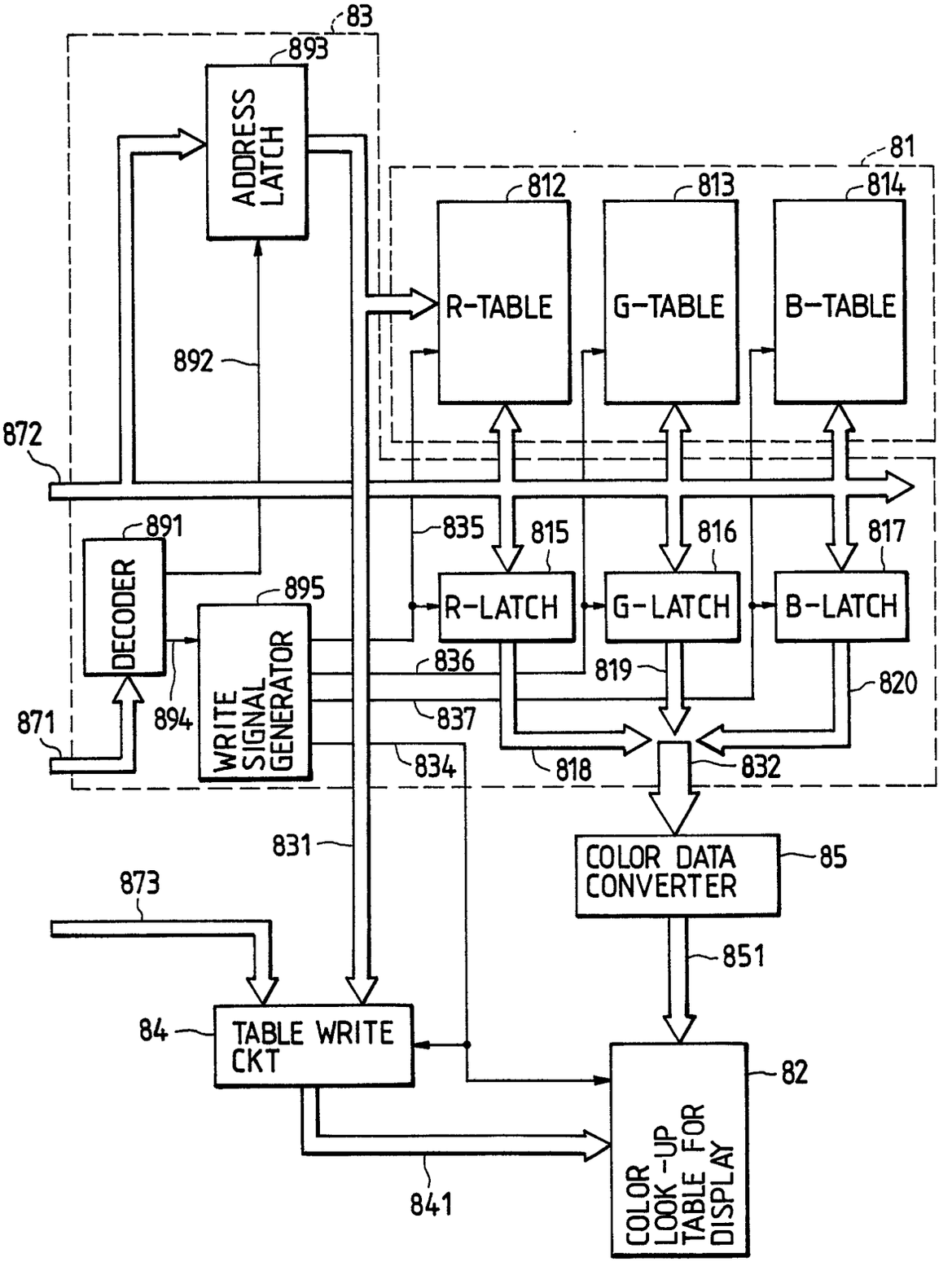

83
893
ADDRESS LATCH
81
812
813
814
R-TABLE
G-TABLE
B-TABLE
892
872
891
835
815
816
817
DECODER
895
R-LATCH
G-LATCH
B-LATCH
836
819
820
871
894
WRITE SIGNAL GENERATOR
837
834
818
832
831
COLOR DATA CONVERTER
85
873
851
84
TABLE WRITE CKT
82
COLOR LOOK-UP TABLE FOR DISPLAY
841

FIG. 6A

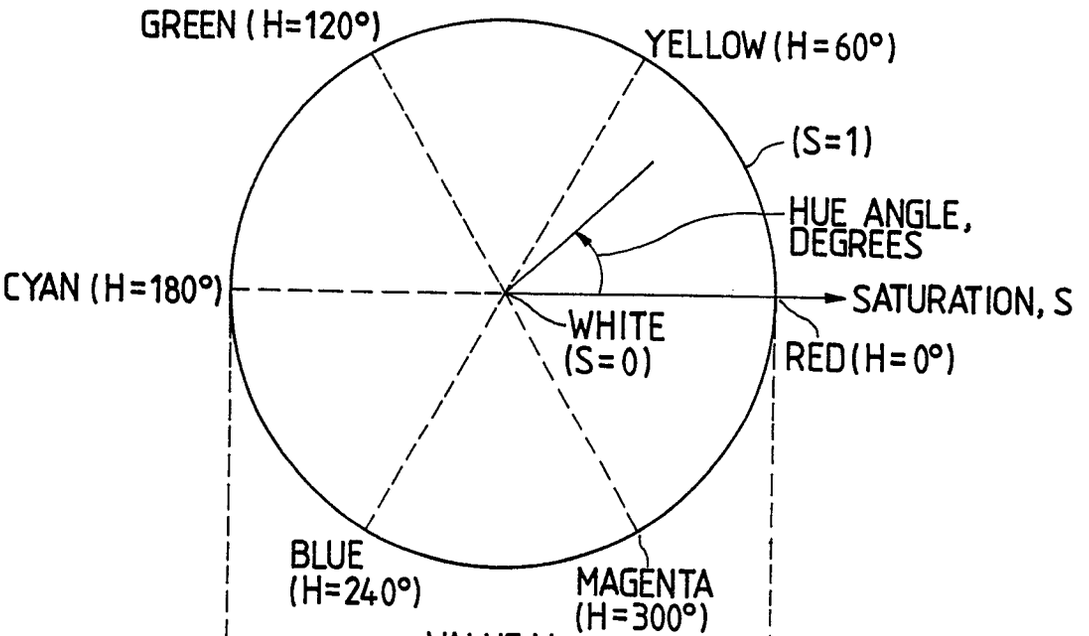

GREEN (H=120°)
YELLOW (H=60°)
(S=1)
HUE ANGLE, DEGREES
CYAN (H=180°)
SATURATION, S
WHITE (S=0)
RED (H=0°)
BLUE (H=240°)
MAGENTA (H=300°)

FIG. 6B

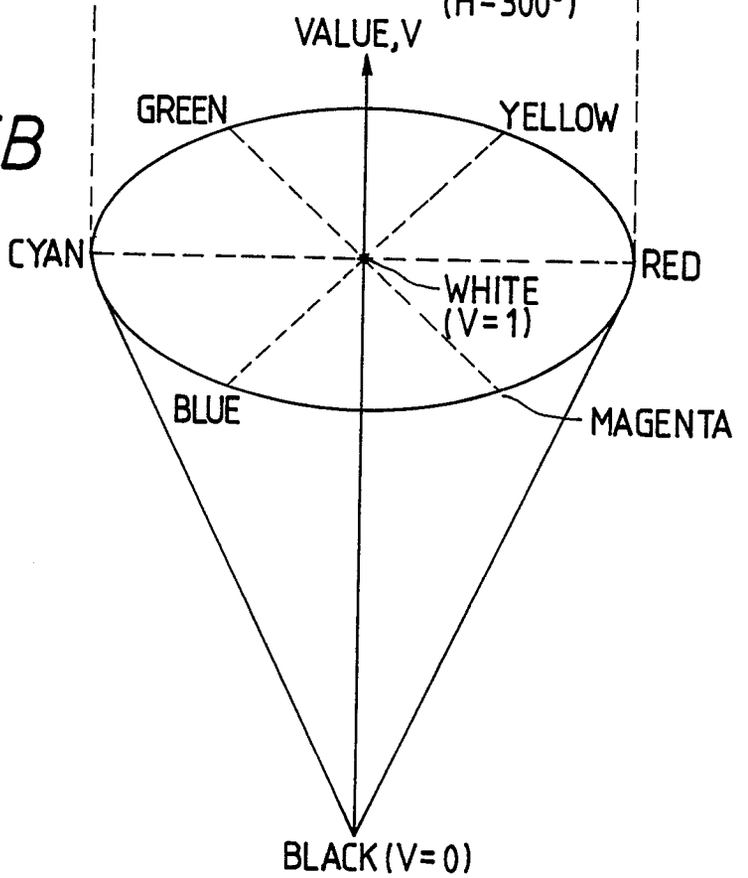

VALUE, V
GREEN
YELLOW
CYAN
RED
WHITE (V=1)
BLUE
MAGENTA
BLACK (V=0)

FIG. 7A

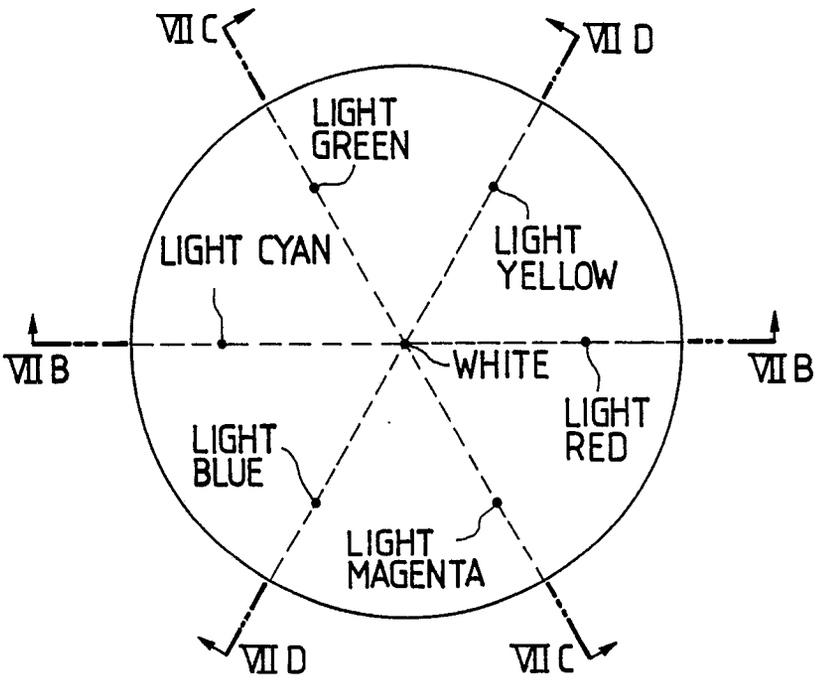

VII C
VII D
LIGHT GREEN
LIGHT CYAN
LIGHT YELLOW
VII B
WHITE
VII B
LIGHT RED
LIGHT BLUE
LIGHT MAGENTA
VII D
VII C

FIG. 7B

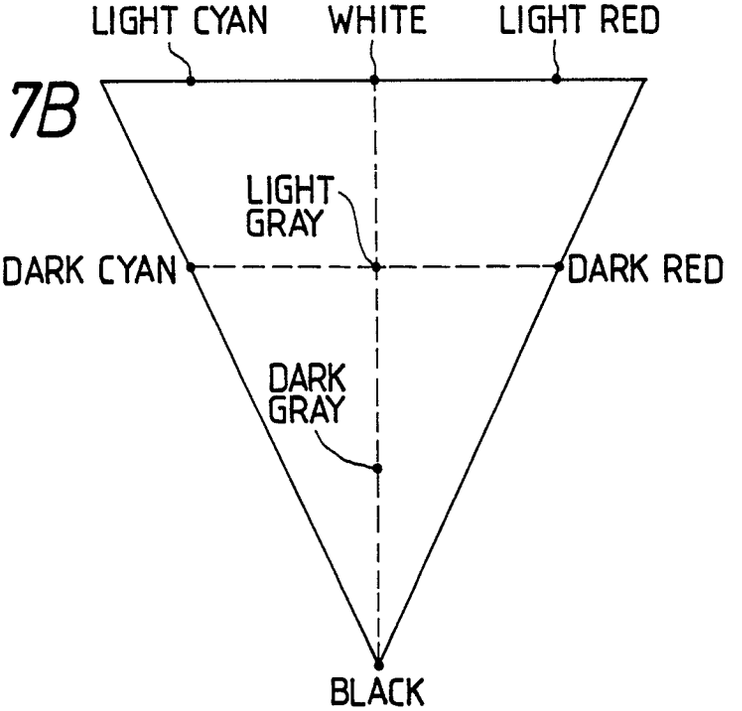

LIGHT CYAN
WHITE
LIGHT RED
LIGHT GRAY
DARK CYAN
DARK RED
DARK GRAY
BLACK

FIG. 7C

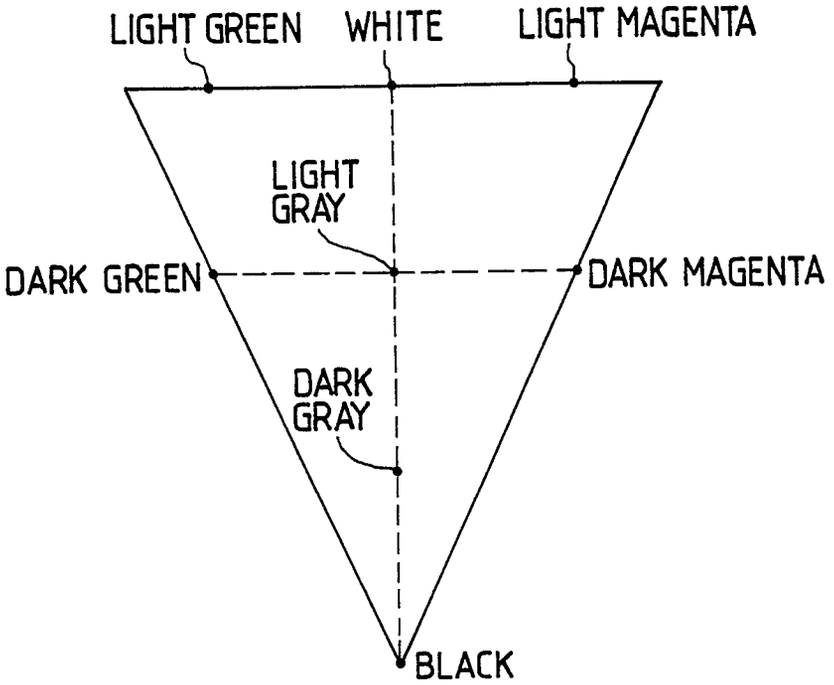

LIGHT GREEN
WHITE
LIGHT MAGENTA
LIGHT GRAY
DARK GREEN
DARK MAGENTA
DARK GRAY
BLACK

FIG. 7D

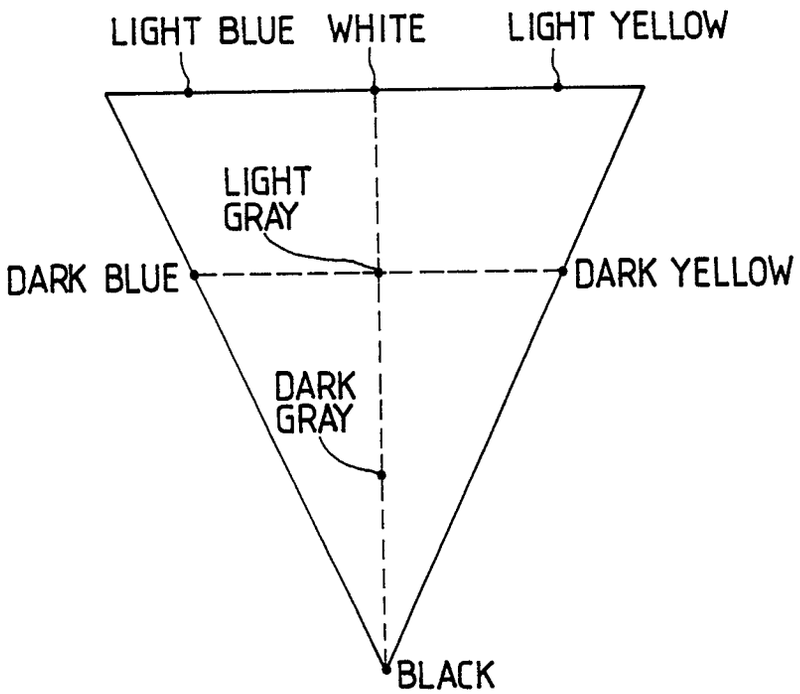

LIGHT BLUE
WHITE
LIGHT YELLOW
LIGHT GRAY
DARK BLUE
DARK YELLOW
DARK GRAY
BLACK

FIG. 8A

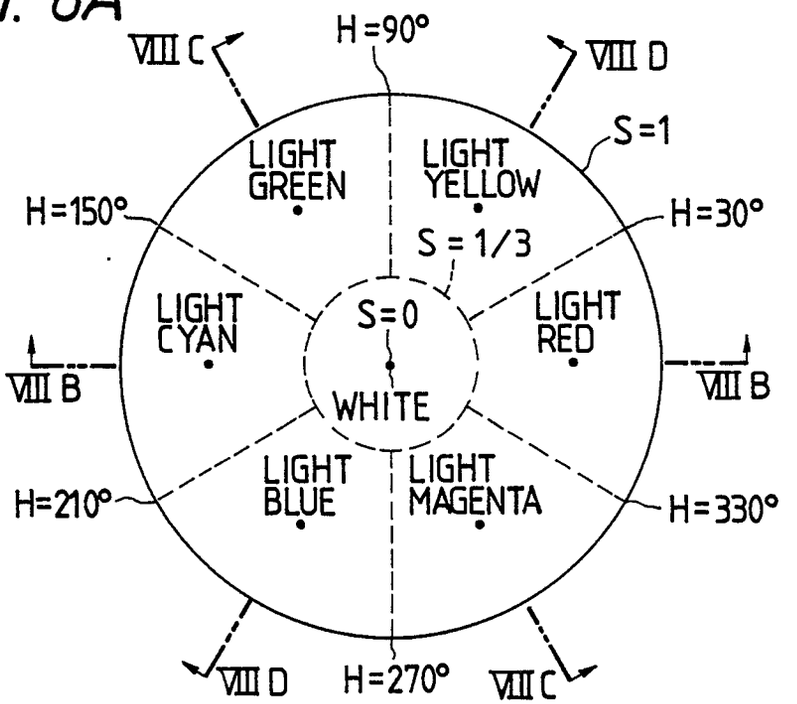

H=90°
VIII C
VIII D
S=1
LIGHT GREEN
LIGHT YELLOW
H=150°
H=30°
S=1/3
LIGHT CYAN
S=0
LIGHT RED
VIII B
VIII B
WHITE
LIGHT BLUE
LIGHT MAGENTA
H=210°
H=330°
VIII D
H=270°
VIII C

FIG. 8B

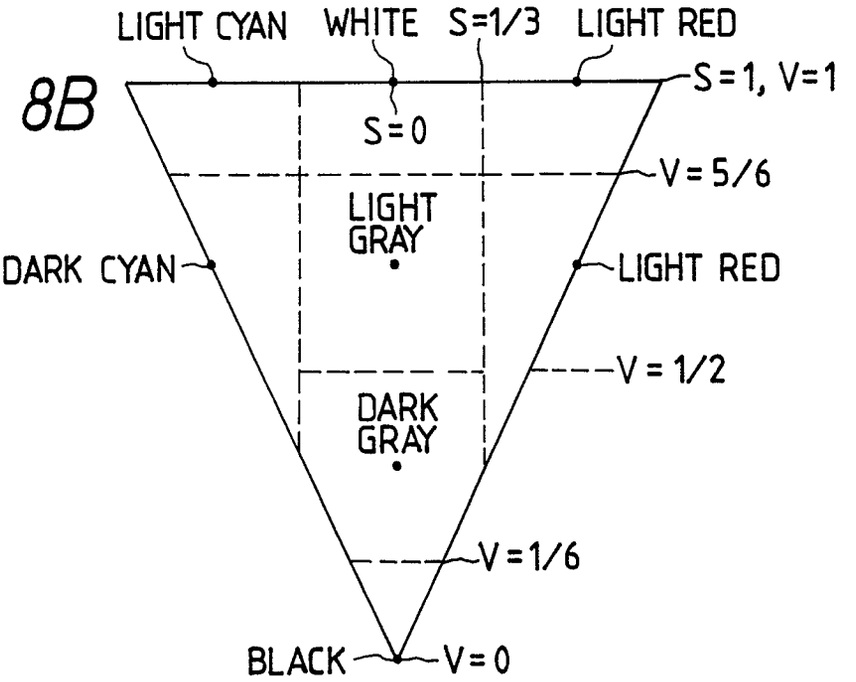

LIGHT CYAN
WHITE
S=1/3
LIGHT RED
S=1, V=1
S=0
V=5/6
LIGHT GRAY
DARK CYAN
LIGHT RED
V=1/2
DARK GRAY
V=1/6
BLACK
V=0

FIG. 8C

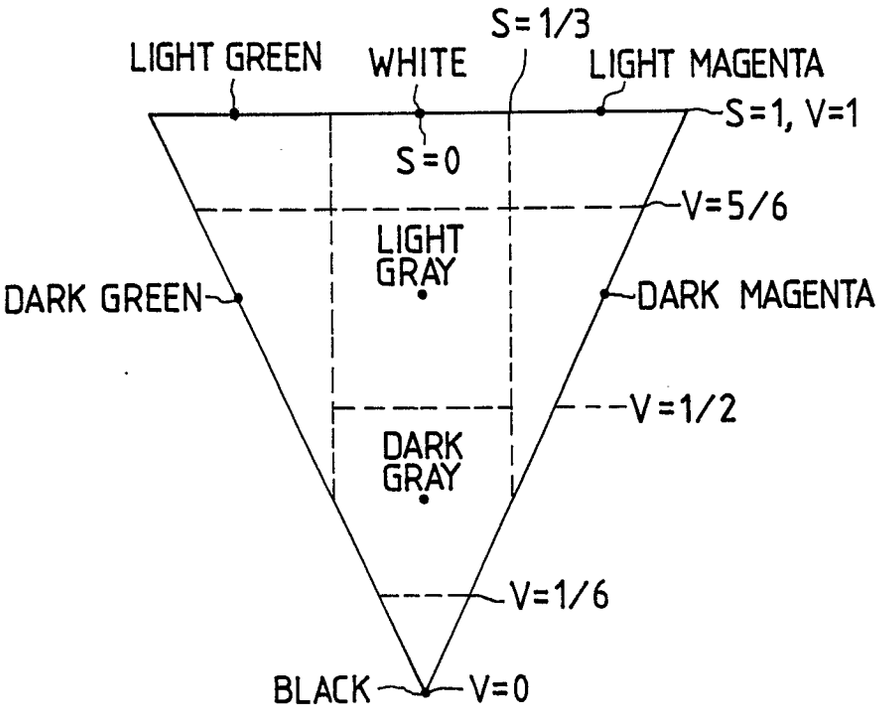

S=1/3
LIGHT GREEN
WHITE
LIGHT MAGENTA
S=1, V=1
S=0
V=5/6
LIGHT GRAY
DARK GREEN
DARK MAGENTA
V=1/2
DARK GRAY
V=1/6
BLACK
V=0

FIG. 8D

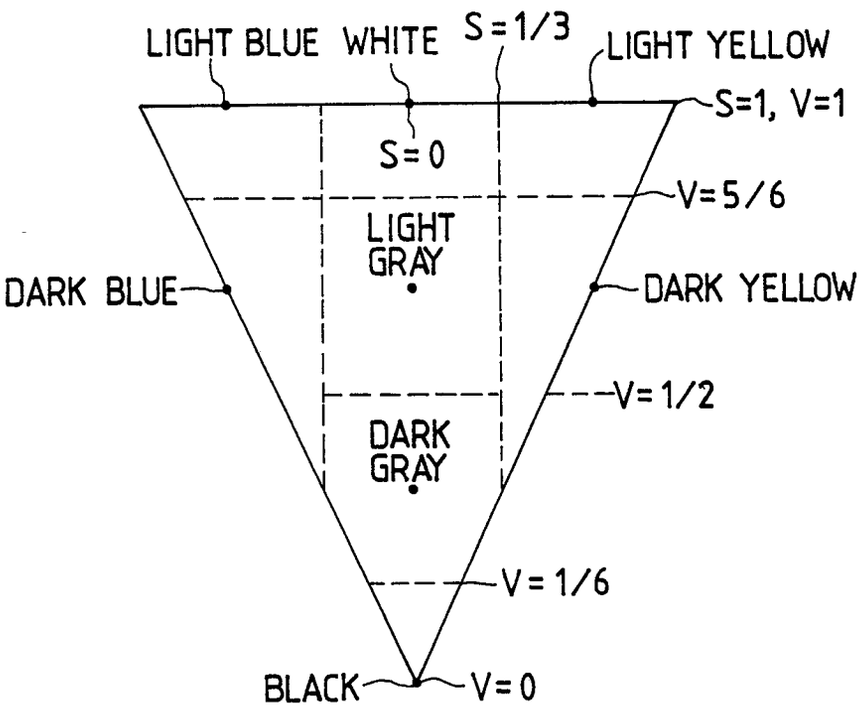

LIGHT BLUE
WHITE
S=1/3
LIGHT YELLOW
S=1, V=1
S=0
V=5/6
LIGHT GRAY
DARK BLUE
DARK YELLOW
V=1/2
DARK GRAY
V=1/6
BLACK
V=0

FIG. 9

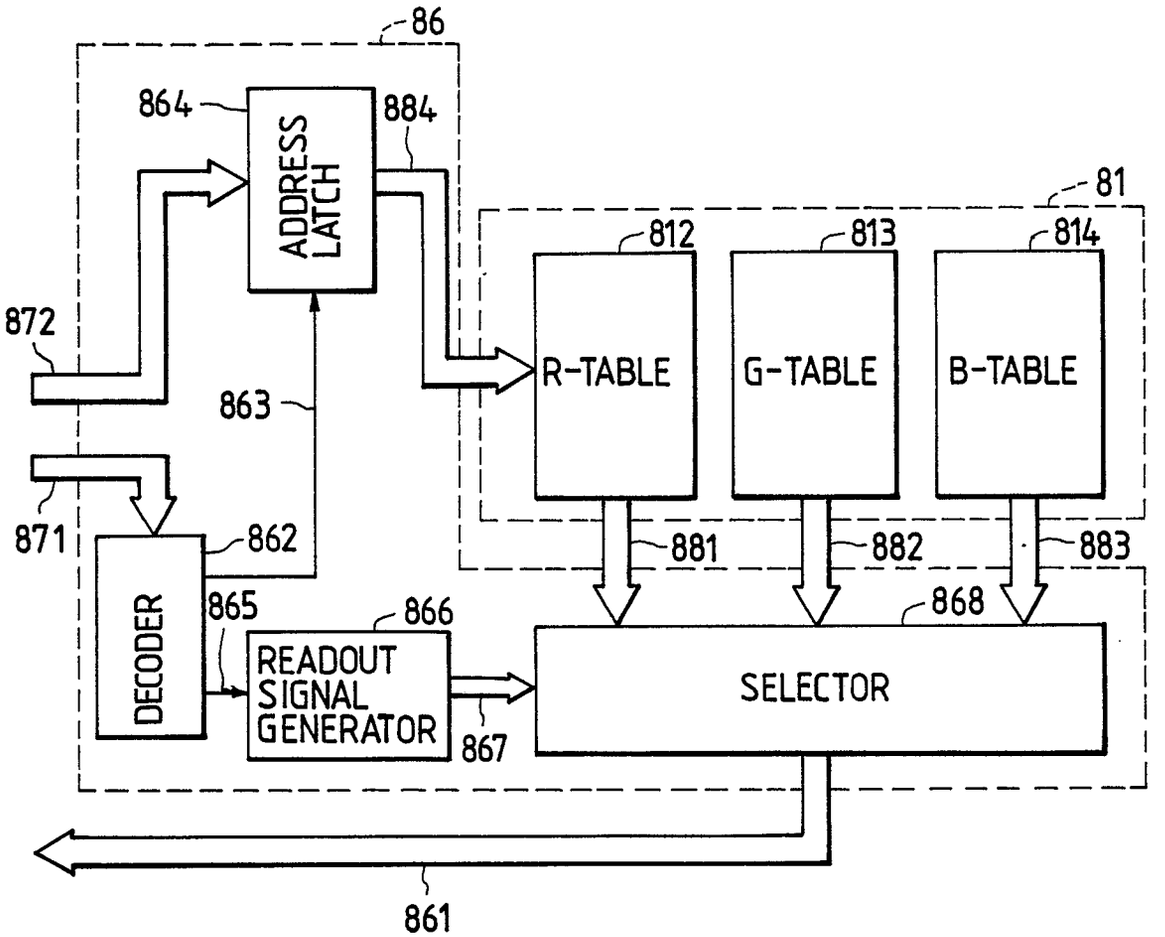

86
864
ADDRESS LATCH
884
81
812
813
814
872
R-TABLE
G-TABLE
B-TABLE
863
871
862
881
882
883
865
866
868
DECODER
READOUT SIGNAL GENERATOR
867
SELECTOR
861

FIG. 10

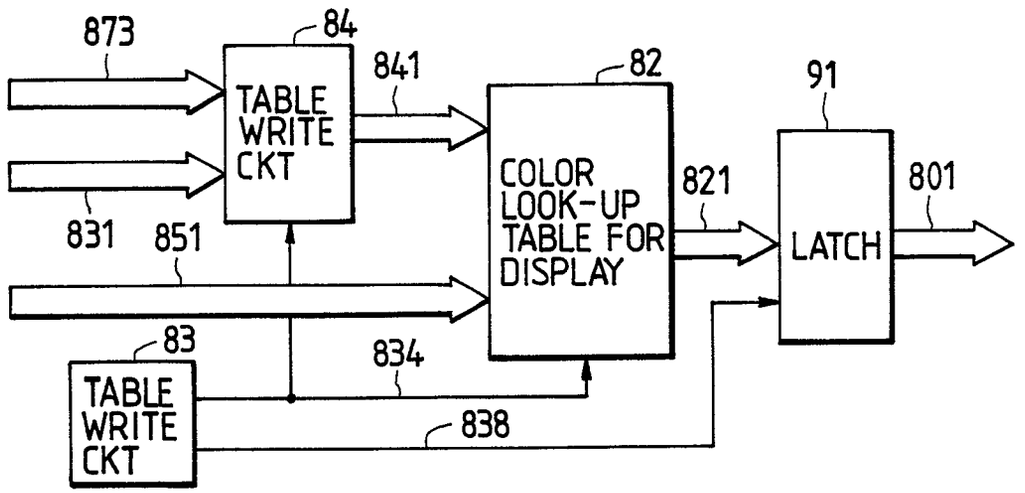

873
84
TABLE WRITE CKT
841
82
91
COLOR LOOK-UP TABLE FOR DISPLAY
821
LATCH
801
831
851
83
TABLE WRITE CKT
834
838

FIG. 11

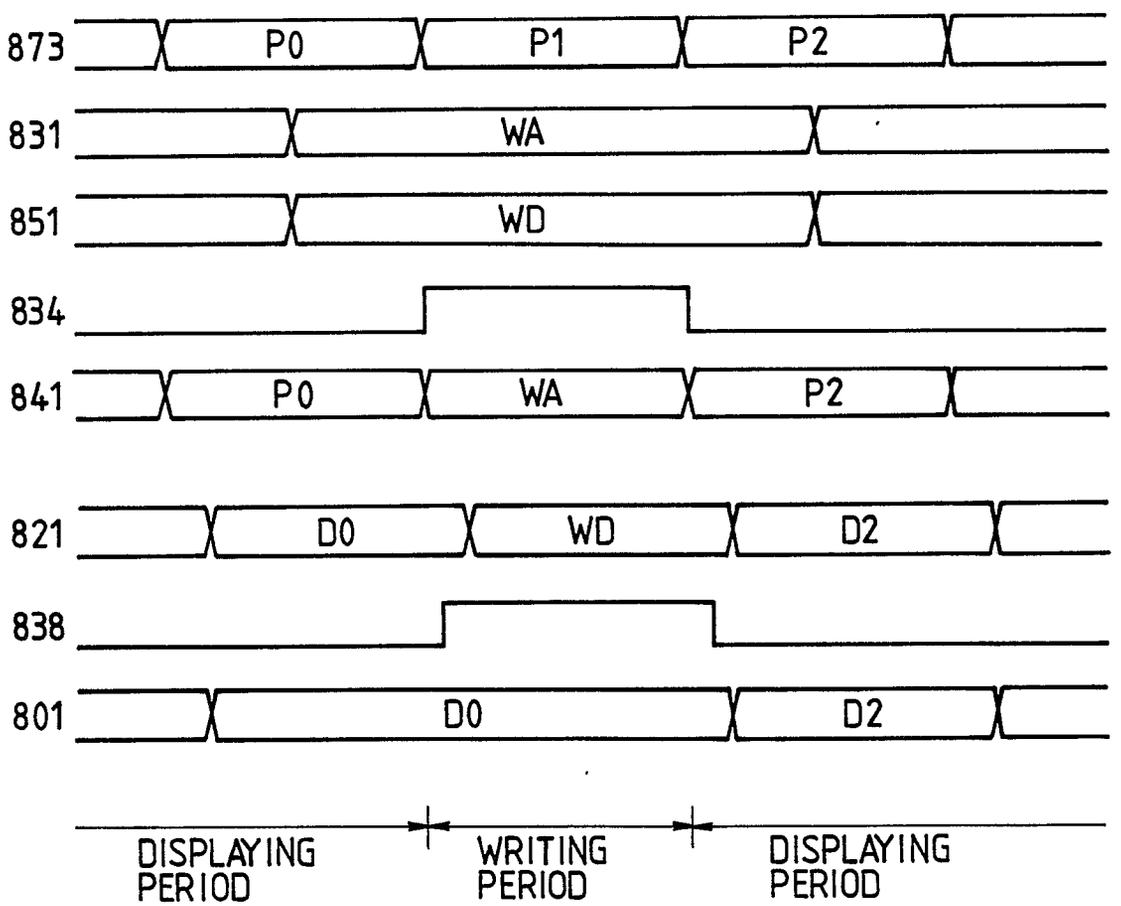

873
P0
P1
P2
831
WA
851
WD
834
841
P0
WA
P2
821
D0
WD
D2
838
801
D0
D2
DISPLAYING PERIOD
WRITING PERIOD
DISPLAYING PERIOD

FIG. 12

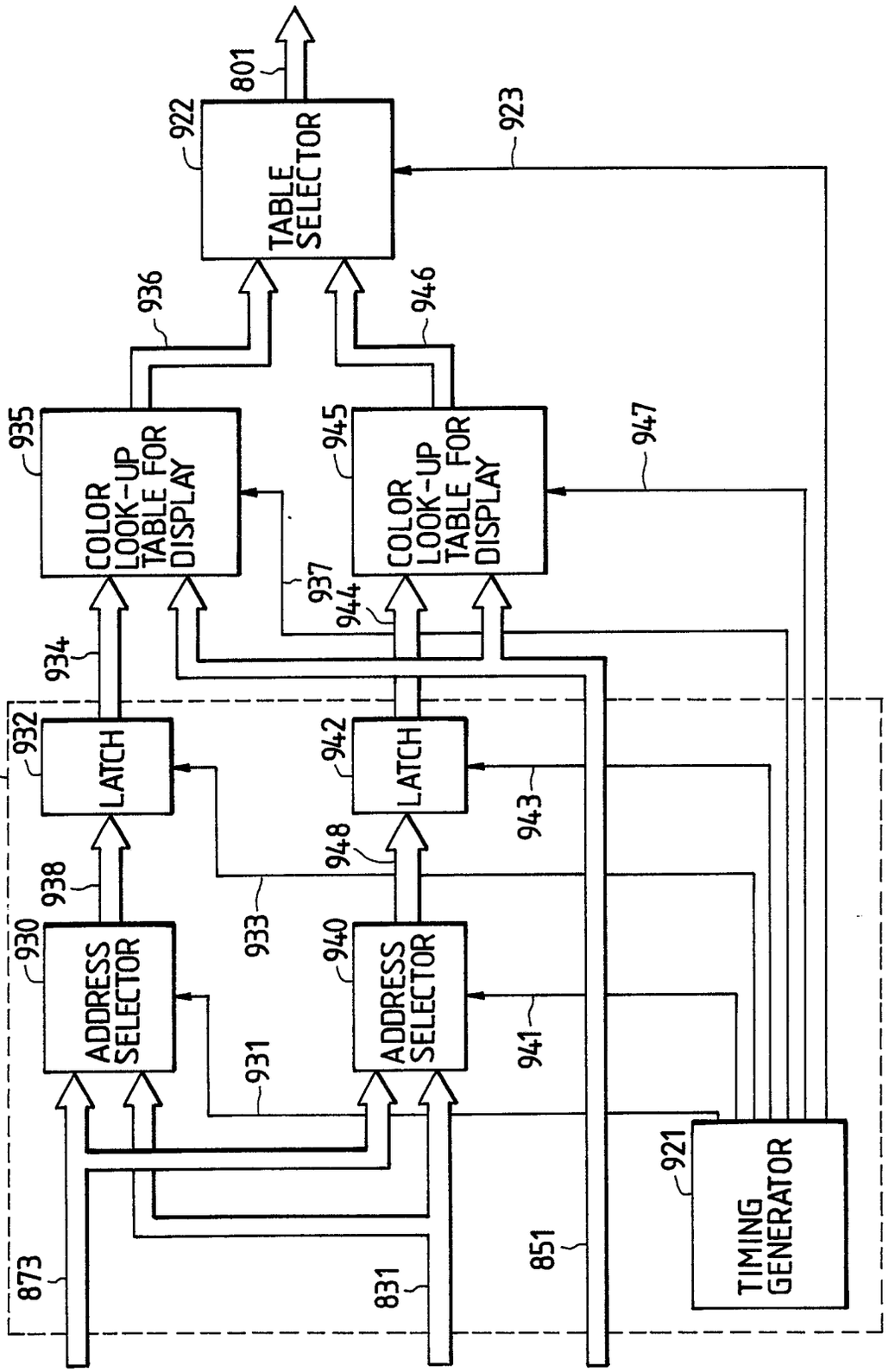

801
922
TABLE SELECTOR
923
936
946
935
COLOR LOOK-UP TABLE FOR DISPLAY
945
COLOR LOOK-UP TABLE FOR DISPLAY
947
937
944
934
92
932
LATCH
942
LATCH
943
948
938
933
930
ADDRESS SELECTOR
940
ADDRESS SELECTOR
941
931
921
TIMING GENERATOR
873
831
851

FIG. 13

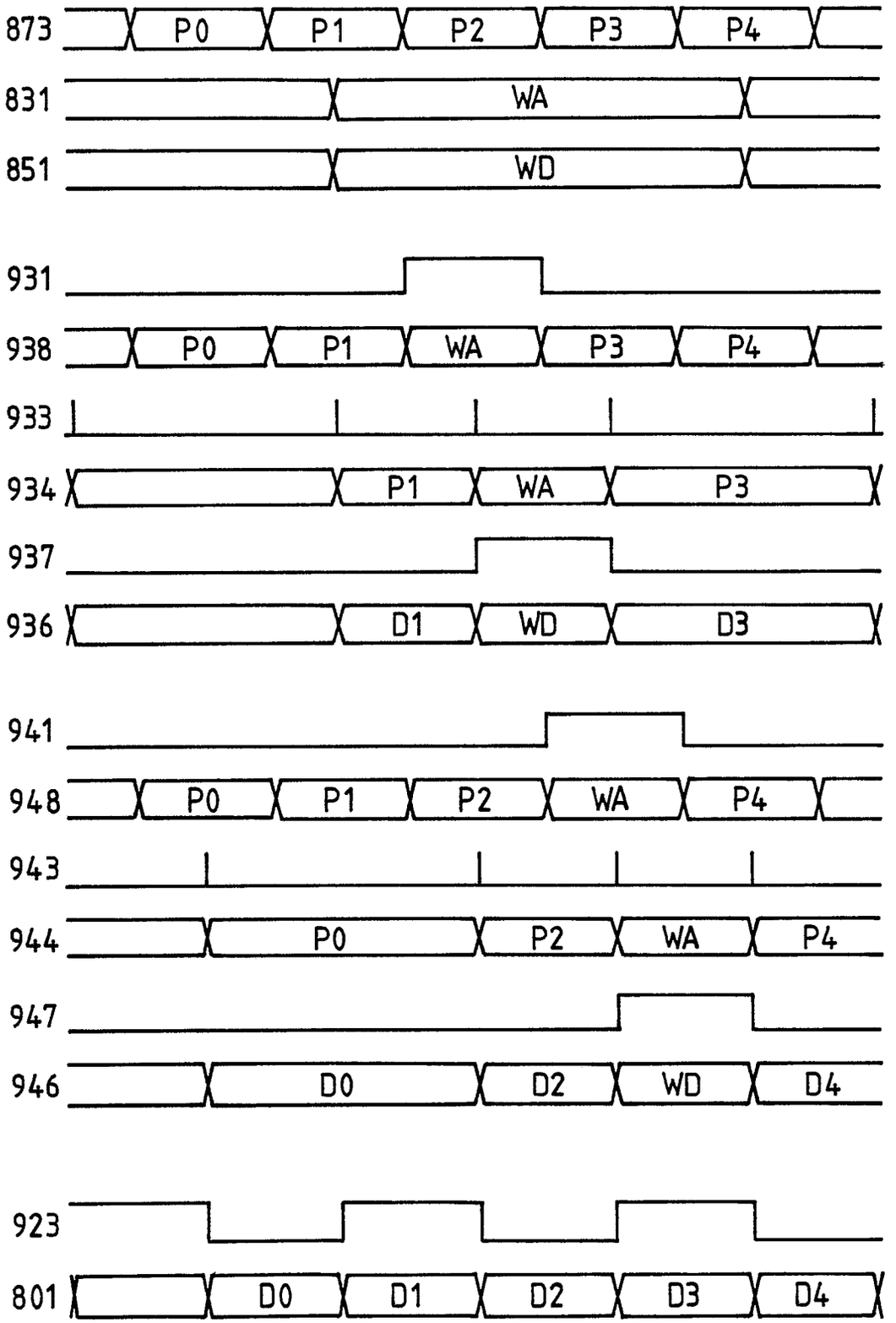
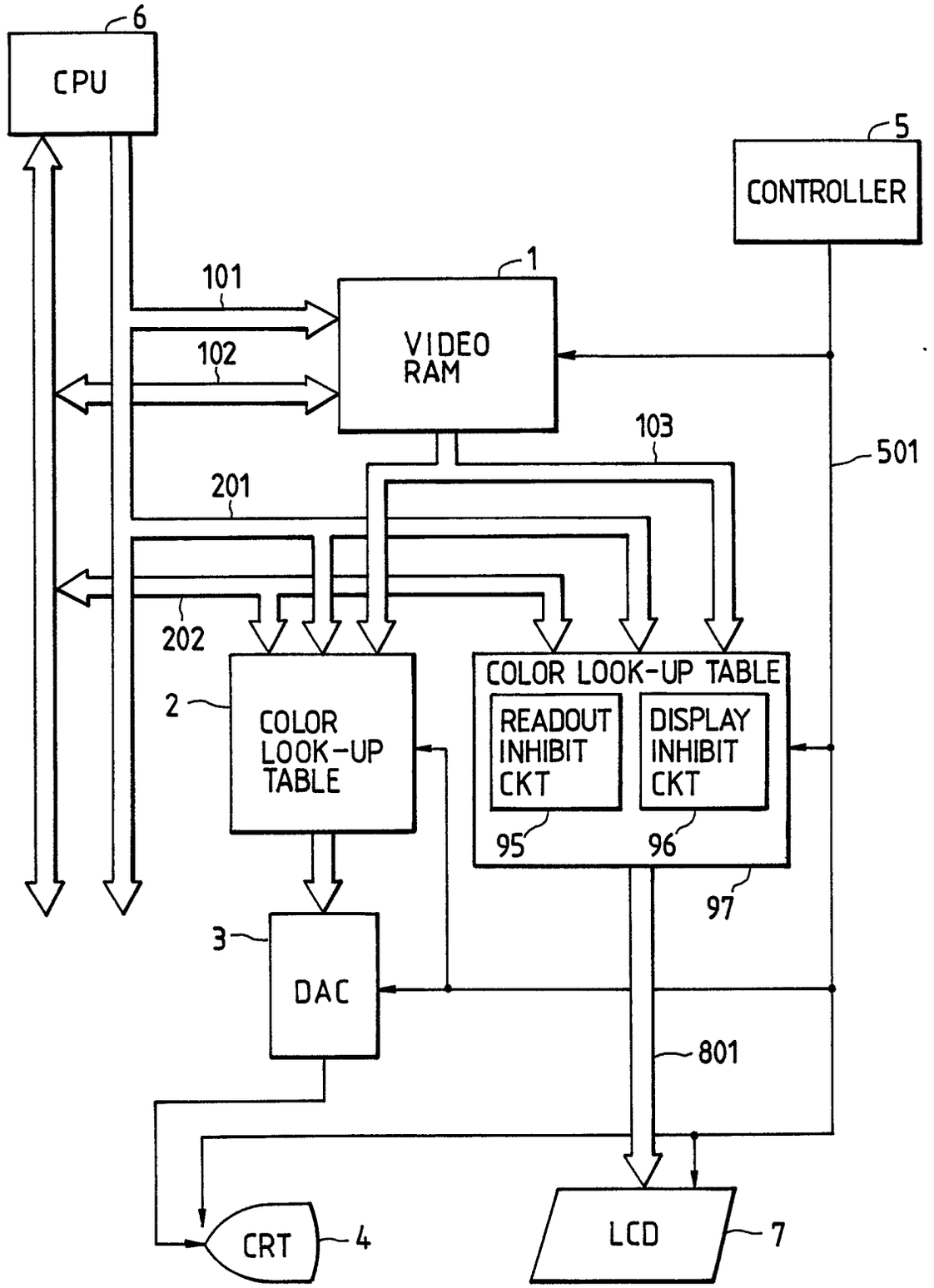

873
P0
P1
P2
P3
P4
831
WA
851
WD
931
938
P0
P1
WA
P3
P4
933
934
P1
WA
P3
937
936
D1
WD
D3
941
948
P0
P1
P2
WA
P4
943
944
P0
P2
WA
P4
947
946
D0
D2
WD
D4
923
801
D0
D1
D2
D3
D4

FIG. 14


6
CPU
5
CONTROLLER
101
1
VIDEO RAM
102
103
501
201
202
2
COLOR LOOK-UP TABLE
COLOR LOOK-UP TABLE
READOUT INHIBIT CKT
DISPLAY INHIBIT CKT
95
96
97
3
DAC
801
CRT
4
LCD
7