



12

EUROPEAN PATENT SPECIFICATION

45 Date of publication of patent specification :
18.01.95 Bulletin 95/03

51 Int. Cl.⁶ : **G11C 8/00, G11C 11/412**

21 Application number : **89480146.3**

22 Date of filing : **26.09.89**

54 **Memory cell and read circuit.**

30 Priority : **31.10.88 US 265075**

43 Date of publication of application :
09.05.90 Bulletin 90/19

45 Publication of the grant of the patent :
18.01.95 Bulletin 95/03

84 Designated Contracting States :
DE FR GB

56 References cited :
EP-A- 0 135 137
US-A- 4 447 891
IEEE JOURNAL OF SOLID STATE CIRCUITS,
vol. 23, no. 5, October 1988, pages 1030-1040;
T.-S. YANG et al.: "A 4-ns 4K X 1-bit two-port
BiCMOS SRAM"

73 Proprietor : **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

72 Inventor : **Dawson, James William**
32 Bart Drive
Poughkeepsie, N.Y. 12603 (US)
Inventor : **Phillips, Panagiotis Andrew**
1 Hideaway Lane
Newburgh, N.Y. 12550 (US)

74 Representative : **Schuffenecker, Thierry**
Compagnie IBM France,
Département de Propriété Intellectuelle
F-06610 La Gaude (FR)

EP 0 367 703 B1

Note : Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid (Art. 99(1) European patent convention).

Description

Cross-Reference to Related Application

The invention relates to a static all-CMOS memory cell of cross-coupled transistors having an additional bit line driver/isolation stage configured as a CMOS inverter between one cell node and a read-select transistor.

Background of the Invention

The present invention relates to a memory cell, and more particularly to a single-bit, dual-port cell, and a single-sided read circuit for use with one or more such cells. The cell may, in one embodiment, be used in a static random access memory (RAM) array, and may be implemented in BICMOS technology (i.e., having both bipolar and CMOS or NMOS field-effect transistors (FETs)) on an integrated circuit. Several alternative embodiments are also disclosed.

Static RAM CMOS memory cells are well known. A typical prior art cell is shown in block diagram form in FIG. 1. Such a device typically is comprised of a bit storage unit 10 coupled to pass or transfer devices 12 and 14 for the writing and reading of data, respectively. Write pass device 12, coupled to an input 11 of storage unit 10, permits data on a write bit line (WBL) 16 to be written into the storage unit upon receipt of a signal, such as a write enable or write word signal, sent over write word line (WWL) 20. The data is typically a binary signal (logical "1" or "0"), represented by a low signal level or high signal level on the write bit line 16. A read operation is accomplished when a read enable or read word signal is sent over a read word line (RWL) 22, which activates read pass device 14 to allow data to be read out of storage unit 10 through output 13 and pass device 14 onto read bit line (RBL) 18. The cell of FIG. 1 thus operates as a dual-port memory cell, the first port being the write bit line/write word line pair and the second port being the read bit line/read word line pair.

A specific circuit implementation of the prior art cell of FIG. 1 is shown in FIG. 2. Such a cell, commonly known as a "6-device cell," is comprised of six FETs, specifically transistors 24, 26, 28, 30, 32 and 34 in the diagram. This type of circuit is disclosed, for example, in U.S. Patent Nos. 4,580,245; 4,638,461; 4,644,500; and IBM Technical Disclosure Bulletin, Vol. 31, No. 1, June 1988, at p. 291; and a similar cell is disclosed in IBM Technical Disclosure Bulletin, Vol. 17, No. 11, April 1975, at p. 3338.

The primary feature of such cells is a bit storage unit comprised of a flip-flop or latch. The flip-flop is formed from four FETs, specifically 24, 26, 28, 30, in a dual, cross-coupled inverter configuration. Transistor 24 is typically of the opposite conductivity type from transistor 26, and transistor 28 is typically of the

opposite conductivity type from transistor 30. For example, transistors 24 and 28 usually are P-channel FETs (PFETs) and transistors 26 and 30 usually are N-channel FETs (NFETs). The source-drain current paths of transistors 24 and 26 are coupled in series with each other and between a voltage source V_c 31 and a ground terminal 33. Similarly, the source-drain current paths of transistors 28 and 30 are coupled in series with each other and between voltage source 31 and ground terminal 33. The gates of transistors 24 and 26 are coupled together and the gates of transistors 28 and 30 are similarly coupled together. A connection from the gates of transistors 28 and 30 to the intersection of the source-drain current paths of transistors 24 and 26 forms a first internal node 25 of the cell, and a connection from the gates of transistors 24 and 26 to the intersection of the source-drain current paths of transistors 28 and 30 forms a second internal node 29.

The input (for writing) of the storage unit 10 is the first internal node 25, coupled through the source-drain current path of write pass transistor 32 to write bit line 16. Transistor 32 is controlled by an enable signal applied to its gate over write word line 20 to permit data on line 16 to flow into the flip-flop, setting it into one of two bistable states. An analogous arrangement is provided on the output or read side of the device. The second internal node 29 is coupled through the source-drain current path of read pass transistor 34 to read bit line 18. Reading is accomplished by applying an enable signal to the gate of transistor 34 over read word line 22.

Although the prior art cell of FIG. 2 accomplishes a basic data read and data write function in a two-port manner, problems sometimes arise in the operation of this device. One problem is that both the write operation and the read operation require a voltage level change on the appropriate bit line. For example, the reading of a "1" may require the voltage on read bit line 18 to be "pulled-up" or "pulled-down." If the pass transistor 34 alone is relied upon for this operation, a delay may result because transistor 34, being an FET, typically cannot handle high currents or switch rapidly. The delay is increased if several cells are attached to the same bit lines, thus increasing the capacitive load that must be overcome. Also, the voltage swing on read bit line 18 will be limited.

Another problem with the cell of FIG. 2 is that the data stored in the flip-flop is sometimes disturbed by the read operation itself. The activation of pass transistor 34 by the enable signal on read word line 22 sometimes permits the data current or other spurious currents on read bit line 18 to flow through transistor 34 into or out of the flip-flop device, which currents may be high enough either to change the state of the cell, thus destroying the data, or to slow down the operation of the cell. The size of transistor 34 is critical with respect to the flip-flop device sizes. If the correct

size limits on transistor 34 are not observed, then the cell is subject to disturb problems.

European Patent Application EP-A-229 317 describes a transducer system which comprises a flip-flop memory cell and a first and second FETs, the source-drain current paths therethrough being coupled together in series between ground and a bit line, the gate of the first FET being coupled to an output terminal of the flip-flop memory cell and the gate of second FET being coupled to a word line.

Summary of the Invention

The present invention is intended to remedy the above-mentioned disadvantages and provide a memory cell capable of extremely rapid reading of information and having a very low susceptibility to read disturb problems. Several alternative embodiments are disclosed, including a cell having a single-sided read circuit with isolation and fast bit-line drive; a cell having two read ports; a cell having a differential read; a read circuit for an entire array of cells; and a continuous-read cell. The embodiments may be implemented in BICMOS technology.

In accordance with a first aspect, the present invention comprises:

- a storage unit for storing a data signal,
- a pass device and a pass/isolation device, each having a signal path and a control terminal, the control terminal of the pass device being coupled to an enable line and the control terminal of the pass/isolation device being coupled to an output terminal of the storage unit,

and is characterized in that:

- the signal paths of the pass device and pass/isolation device are coupled together in series between a control node and a read line, and

- it further comprises a driver having a signal path coupled between the read line and a constant-signal node, and having a control terminal coupled to the control node, and arranged to cause a read signal proportional to the data signal to appear on the read line in response to an enable signal on the enable line.

In accordance with a second aspect, the present invention comprises a memory device, comprising:

- a common read bit line;
- a plurality of read word lines;
- a plurality of single-bit storage units, each having an output coupled to the gate terminal of a first field-effect transistor (FET) associated with such storage unit, such first FET comprising a pass/isolation device, the source-drain current path of such FET being coupled at one end to one end of the source-drain current path of a second FET associated with such storage unit, such second FET comprising a pass device, the other end of such current path being coupled to the common read line, the gate of the second FET being coupled to a particular read

word line;

and is characterized in that:

- the source-drain current path of each said first FET is coupled at the other end to a common control line,

- it comprises a bipolar transistor comprising a common bit line driver device, the collector of which is coupled to the common read bit line, the emitter of which is coupled to ground and the base of which is coupled to the common control line, and

- it comprises an FET comprising an impedance device, the source-drain current path of which is coupled between the common control line and ground, and the gate of which is coupled to the common read bit line.

Other variations and embodiments of the invention are also disclosed, and are discussed more fully in the detailed description below.

Brief Description of the Drawings

To facilitate further description of the invention, the following drawings are provided in which:

FIG. 1 is a block diagram of a typical prior art single-bit, dual-port static RAM cell.

FIG. 2 is a schematic circuit diagram of a typical prior art implementation of the memory cell of FIG. 1.

FIG. 3 is a block diagram of one embodiment of the present invention.

FIG. 4 is a schematic circuit diagram of one embodiment of FIG. 3.

FIG. 5 is a schematic circuit diagram of an alternative embodiment of FIG. 3.

FIG. 6 is a schematic circuit diagram of an embodiment of the invention using two of the read circuits of FIG. 4 to form a cell with two read ports.

FIG. 7 is a block diagram of an embodiment of the present invention in which the read circuit is used with more than one memory cell.

FIG. 8 is a schematic circuit diagram of one embodiment of FIG. 7.

FIG. 9 is a block diagram of an alternative embodiment of the cell of the present invention.

FIG. 10 is a schematic circuit diagram of one embodiment of FIG. 9.

FIG. 11 is a block diagram of another alternative embodiment of the invention in which the cell is capable of a continuous read, or latch, operation.

FIG. 12 is a schematic circuit diagram of one embodiment of FIG. 11.

FIG. 13 is a timing diagram of a read operation of the embodiment of FIG. 4.

FIG. 14 is a timing diagram of a read operation of the embodiment of FIG. 10.

FIG. 15 is a timing diagram of a write operation from "high" to "low" of the embodiment of FIG. 4.

FIG. 16 is a timing diagram of a write operation from "low" to "high" of the embodiment of FIG. 4.

Detailed Description of the Preferred Embodiments

Referring now to FIG. 3, there is shown therein a functional block diagram of one embodiment of the present invention. The present invention is not, however, limited to this particular configuration or to the configuration shown in any other drawing.

In FIG. 3, a storage unit 10 is provided for the storage of data, such as a single bit. Storage unit 10, which may comprise a flip-flop, has an input 11 for writing, which is coupled to one of a signal path of a pass device 12. The other end of this signal path is coupled to a write bit line 16, and the signal path is controlled by signals on a write word line (WWL) 20. Information (represented, for example, by a high or low level signal) present on write bit line 16 may be gated into storage unit 10 through pass device 12 in response to a write enable (word select) signal sent over write word line 20 to the control terminal of pass device 12.

The present invention may also be used in connection with a read-only memory (ROM), in which case elements 11, 12, 16 and 20 need not be present, or may be present but non-operational.

A feature of the present invention is the read circuit shown generally by elements 40, 42, 44 and 46 of FIG. 3. The read or output terminal 13 of storage unit 10 is coupled to a control terminal of a pass/isolation device 40. Pass/isolation device 40 also has a signal path that is coupled in series with a signal path of a second pass device 42. Pass device 42 is, in turn, coupled through its signal path to a read bit line (RBL) 18, and is controlled by signals from read word line (RWL) 22 input to a control terminal of device 42. The signal path of pass/isolation device 40 is further coupled to a control node 45 and then through an impedance 46 to a constant signal node 33, which could be ground or any other constant signal source or sink, such as a voltage terminal of a power supply. Element 44 is a read line driver having a signal path that is coupled between read bit line 18 and constant signal node 33, and a control terminal that is coupled to control node 45.

The primary function of pass device 42 is to allow a read operation to take place from storage unit 10 by way of a read enable (word select) signal applied over read word line 22 to the control terminal of pass device 42. Pass device 42 is not needed if a continuous read or latch function is desired. In such a case, device 42 may be replaced by a signal path connecting pass/isolation device 40 directly to read bit line 18.

Pass/isolation device 40, as the name implies, performs two functions -- operating as a pass device in conjunction with pass device 42 to enable the reading of data, and providing isolation between storage unit 10 and read bit line 18, so as to prevent read or stray signals from read bit line 18 from entering storage unit 10 and adversely affecting the data stored in

such unit.

A primary purpose of read line driver 44 is to cause a rapid transition of the signal level on read bit line 18 to take place if, at the beginning of a read operation, the signal level in storage unit 10 is at a different level from the standby signal level on read bit line 18. For a high-speed memory operation, the signal level on read bit line 18 should move from a low level to a high level or vice versa as rapidly as possible without causing interference with the data in storage unit 10. This change of levels is sensed by a sense amplifier (not shown) to read the data.

A primary function of impedance 46 is to prevent the control terminal of read line driver 44 from "floating" between memory cycles, so that the driver is not turned on at the wrong time in the memory cycle. Impedance 46 is not, however, needed if the control terminal of driver 44 is not susceptible to "floating" problems.

Preferred circuit implementations of the cell of FIG. 3 are shown in FIGS. 4 and 5. In FIG. 4, the storage unit 10, shown in dashed lines, is comprised of 4 transistors, preferably FETs, as in the prior art cell of FIG. 2. Transistors 24 and 28 are preferably PFETs, although they could be resistors instead. Transistors 26 and 30 are preferably NFETs. Internal power to these transistors is supplied by a voltage between voltage terminal V_c 31 and ground. Internal node 25 forms the input for writing and also the output for reading. Alternatively, internal node 29 could form the output. The differential voltage on these two internal nodes equals V_c minus ground, the maximum possible.

Pass device 12 in the preferred embodiment of FIG. 4 comprises an NFET 32, which has its source-drain current path coupled between internal node 25 and write bit line 16. The source terminal of transistor 32 is preferably coupled to internal node 25, and the drain terminal of transistor 32 is preferably coupled to write bit line 16. The gate terminal of transistor 32 comprises its control terminal, and it is coupled to write word line 20.

The read circuit of the present invention is preferably implemented by way of four transistors, specifically two NFETs 50 and 52, an NPN bipolar transistor 54 and an NFET 56, to form a single-sided read circuit. Transistor 50 comprises the pass/isolation device 40 of FIG. 3, and transistor 52 comprises the pass device 42 of FIG. 3. The source-drain current paths of transistors 50 and 52 are coupled together in series and between the read bit line 18 and the control node 45, as shown. In a preferred embodiment, the source terminal of transistor 50 is coupled to node 45, the drain terminal of this transistor is coupled to the source terminal of transistor 52 and the drain terminal of transistor 52 is coupled to read bit line 18. The gate terminal of transistor 50 is coupled to the internal node 25 of the storage unit 10, and the gate ter-

terminal of transistor 52 is coupled to the read word line 22. Transistor 52 could be removed (shorted out across its source-drain current path) if a continuous read or latch function is desired.

The read bit line driver 44 (FIG. 3) in the preferred embodiment of FIG. 4 comprises a bipolar transistor 54, preferably of the NPN type. The collector terminal of this transistor is preferably coupled to the read bit line 18, the emitter terminal is coupled to constant signal node 33 (which is ground in this embodiment), and the base terminal is coupled to control node 45.

The impedance 46 (FIG. 3) comprises an NFET in the preferred embodiment of FIG. 4, although a resistor could be used instead. If an NFET is used, the source-drain current path is coupled between control node 45 and ground (the source terminal preferably being grounded) and the gate terminal is coupled to the read bit line.

An alternative embodiment of the circuit of FIG. 4 is shown in FIG. 5. FIG. 5 is identical to FIG. 4, except that the gate of transistor 50 is coupled to internal node 29 of storage unit 10 instead of to internal node 25, as in FIG. 4. The read operation of the memory cell of FIG. 3 will now be described, with particular reference to FIG. 5. Assume, first, that a logical "0" has previously been stored in storage unit 10. In order to read this 0 level out, read bit line 18 will normally be "precharged" to a high level. (Precharging circuitry could, for example be provided by a resistive load coupled between voltage terminal V_c 31 and read bit line 18, with a switch coupled to the timing circuitry for the memory). When a 0 is stored in storage unit 10, internal node 29 is at a high level and internal node 25 is at a low level.

The reading of the 0 data is enabled by a signal sent over read word line 22 to the gate of transistor 52. When this device turns on, transistor 52 provides a conducting signal path between read bit line 18 and transistor 50. Since internal node 29 is high and is coupled to the gate of transistor 50, transistor 50 also conducts. With both devices 50 and 52 conducting, a completed current path is established between the read bit line 18 and control node 45, and then to the base of the bipolar transistor 54. The base of transistor 54 was initially at a low level because transistor 56 had previously been on and conducting to the ground terminal 33 by way of the high signal from read bit line 18 to the gate of transistor 56.

As soon as bipolar transistor 54 turns on and conducts, the voltage at the collector quickly drops toward ground level, and consequently quickly pulls the voltage on read bit line 18 down to ground. A sense amplifier (not shown), coupled to read bit line 18, senses the change of voltage on read bit line 18 from high to low and interprets this as the reading of a 0 from the memory cell. Transistor 56 is small in comparison with the other transistors and cannot hold the base of transistor 54 low when the transistors 50 and

52 are conducting. The purpose of transistor 56 is to prevent the base of transistor 54 from "floating" to a level higher than ground when transistors 50 or 52 are off (i.e., when the cell is in a standby mode or a write mode). Should transistor 54 be provided with a non-floating base, or another mechanism to prevent false turn-ons, then transistor 56 would not be required.

Assume now that a logical "1" has been stored in the storage unit 10 of FIG. 5, and it is desired to read this data. Internal node 29 will show a low signal level and internal node 25 will show a high signal level in this event. With node 29 "low", transistor 50 will not turn on, even when transistor 52 is turned on by the enable signal at its gate from read word line 22. Thus, control node 45 will stay at a low voltage level and will also keep the base of transistor 54 low, preventing transistor 54 from conducting along its collector-emitter current path. Read bit line 18 was previously precharged high, as before. Since transistor 54 does not conduct upon a read signal, read bit line 18 will stay high, and a "1" is read by the sense amplifier (not shown). The read operations described above could either be clocked or non-clocked.

The operation of the circuit of FIG. 4 is the same as the operation of the circuit of FIG. 5, except that the data on the read bit line 18 is inverted relative to the data on the read bit line 18 of FIG. 5. FIG. 4 also has a faster write time than FIG. 5.

An advantage offered by the circuits of FIGS. 4 and 5 over the prior art circuit of FIG. 2 is that the data stored in storage unit 10 is much less susceptible to being disturbed by the read operation going on in read bit line 18 and its associated circuitry, elements 50, 52, 54 and 56. Transistor 50 provides a type of isolation between read bit line 18 and storage unit 10, there being very little leakage current between the source-drain current path and the gate terminal of transistor 50. Thus, it is difficult for signals on read bit line 18 to change the data in storage unit 10 by going back through the gate of transistor 50.

An additional, significant feature of the present invention is the fast switching speed and high current handling ability of bipolar transistor 54. Since bipolar transistors generally switch on and off much faster than FETs of comparable size, the use of a bipolar type in this particular configuration in the read circuitry permits extremely rapid switching times for read bit line 18 (i.e., transition times from low level to high level and vice versa). Larger voltage and current levels than the levels in storage unit 10 can also be handled. Bipolar transistors are, however, generally larger and require more power than FETs, so it is often not desirable to construct the entire memory cell circuit with only bipolar transistors. The use of only one bipolar transistor for bit line switching, while continuing to use CMOS devices for storage unit 10, thus accomplishes the goal of rapid switching time, while permitting the cell to be kept to a very small size on an in-

tegrated circuit chip. The cell is also able to draw a lower total current than would be drawn by an all-bipolar cell.

Another feature of the invention is the use of an impedance, specifically transistor 56, to maintain the base of transistor 54 at a low level during standby operation. Without transistor 56 to tie the base of transistor 54 to ground, transistor 54 could be subject to "floating" or unpredictable voltage levels at its base from control node 45. Such a floating level might, in some cases, be such as to cause transistor 54 to conduct, thus sending a false bit of information onto read bit line 18 and possibly also back into storage unit 10. Transistor 56 could, instead, be a resistor or other type of impedance sufficient to maintain the base of transistor 54 at or close to ground when the cell is not being read.

Another noteworthy feature of the cell of FIG. 4 is the special arrangement of the internal nodes 25 and 29 of storage unit 10. In particular, the internal node 25 is used as the output node (i.e., coupled to the gate of transistor 50), whereas in FIG. 5 the internal node 29 is used as the output node. This configuration permits the cell of FIG. 4 to write substantially faster than the cell of FIG. 5. It also causes the data signal on read bit line 18 of FIG. 4 to be inverted relative to the data signal on the same line of FIG. 5.

Although the cells of FIGS. 4 and 5 show implementations of the invention in the form of 2-port, single-sided read cells, other implementations are also possible. For example, FIG. 6 shows a 3-port cell having one write port and two read ports, each read port having a read circuit ("A" or "B") that is similar to the read circuit of FIG. 4. Two separate read word lines 22A, 22B and two separate read bit lines 18A, 18B are provided, one of each per port. Both ports are attached to internal node 25, or to 29 if desired. This permits access to the same data from two or more independent ports. A similar arrangement is possible for the writing of data -- multiple ports could be attached to internal node 25 for writing.

Another possible implementation of the invention is in a differential read circuit. For example, if FIG. 6 is modified to connect read circuit "B" to internal node 29 instead of to internal node 25, and to connect read word line 22B to read word line 22A, the cell becomes a 2-port cell having a differential read capability, assuming the proper sense amplifier is connected to both read bit lines 18A and 18B.

Still another feature of the present invention is that the read circuit with the bipolar driver transistor may be used with more than one memory cell. Referring now to the block diagram of FIG. 7, there is illustrated a plurality of memory cells comprising for example, a column or array of cells. Each cell consists of a storage unit 10 coupled via output 13 to a pass/isolation device 40 which, in turn, is coupled to a pass device 42, in a manner similar to that shown

in FIG. 3.

A specific circuit embodiment of FIG. 7 is shown in FIG. 8. It is instructive to compare FIG. 8 with FIGS. 4 and 5. With the circuit configuration of FIGS. 7 and 8, it is not necessary to include a read line driver 44 and an impedance 46 with every cell, as is done in the circuits of FIGS. 3-5. Instead, a single driver and a single impedance may be used to read an entire column of cells. As shown in FIG. 7, all of the pass/isolation gates 40, 40', etc. associated with their respective storage units 10, 10', etc. are coupled via a common control line 47 to a single control node 45. Similarly, all of the pass gates 42, 42', etc. are coupled to a single, common read bit line 18.

In this way, read line driver 44 may drive read bit line 18 if any one of the storage units transmits a data signal to control node 45 over line 47 from its associated pass/isolation device. Only one impedance 46 is needed to keep the control terminal of driver 44 from floating. Driver 44 and impedance 46, which form a common read circuit, are coupled to read bit line 18 and common constant signal node 33 in the same manner as that shown in FIG. 3, the only difference being the plurality of lines feeding into node 45 and into bit line 18.

The operation of the circuit of FIG. 7 is similar to the operation of the circuit of FIG. 3, except that since several memory cells are provided per read line, each memory cell preferably has its own separate read word line 22, 22', etc. to permit the individual addressing of cells.

An advantage provided by the circuit of FIGS. 7 and 8 is that fewer devices per memory cell are required. In particular, as shown in FIG. 8, a separate bipolar transistor 54 is not required for each cell. This not only permits a smaller size cell to be fabricated on an integrated circuit chip, but also reduces the capacitance on read bit line 18. Since the capacitance of the collector of a bipolar transistor is relatively high, the fewer collectors coupled to read bit line 18, the lower the total line capacitance will be, and the faster the line switching speed, and hence the read operation, can be.

The read circuit arrangement of FIGS. 7 and 8 is preferred when only a few memory cells are coupled to the same read bit line 18, and the circuit arrangement of FIGS. 3 and 4 is preferred when numerous cells are coupled to read bit line 18. The exact point at which the design of FIGS. 7 and 8 is chosen over the design of FIGS. 3 and 4 depends upon several factors, including the type of fabrication process used for the memory cell transistors, the capacitances of the cell connections and lines, the collector and base capacitances of bipolar transistor 54, the source capacitances of transistors 50 and 50', the size of the individual memory cell transistors and others.

Yet another embodiment of the present invention is the cell shown in FIGS. 9 and 10. In comparing FIG.

9 with FIG. 3, it can be seen that the same elements are used for both cells, but in a slightly different arrangement. In FIG. 9, pass device 42 and read line driver 44 are each coupled to a constant signal terminal V_c 31, instead of to read bit line 18 as in FIG. 3. The other signal terminal of read line driver 44 is, however, coupled to read bit line 18, as before, and pass/isolation device 40 and impedance 46 are also coupled in the same way.

In FIG. 10, it can be seen that the primary difference between this embodiment and the specific embodiment of FIG. 4 is that the bipolar transistor 54 is emitter coupled to read bit line 18 in FIG. 10 instead of being collector coupled to this line, as in FIGS. 4 and 5. This permits bipolar transistor 54 to operate as a pull-up driver for read bit line 18 instead of a pull-down driver as in FIG. 4 and 5. In other words, in operation, bipolar transistor 54 will cause the signal level on read bit line 18 to move from low to high (high being equal to V_c) when transistor 54 turns on. Thus, precharging of the read bit line to a high level is not necessary.

Another difference between FIG. 10 and FIGS. 4 and 5 is that the gate of transistor 56 in FIG. 10 is coupled to the read word line 22, instead of to the read bit line 18 in FIGS. 4 and 5. In addition, transistors 60 and 62 of FIG. 10, which correspond to the pass/isolation device 40 and the pass device 42 of FIG. 9, are of a type different from the analogous transistors 50 and 52 of FIGS. 4 and 5. In particular, transistors 60 and 62 comprise PFETs in the preferred embodiment of FIG. 10 instead of NFETs in the preferred embodiments of FIGS. 4 and 5. Thus, the cell could read when the read word line 22 is low.

Aside from the above differences, however, many similarities remain. For example, transistor 62 could be removed (shorted out across its source-drain current path) if a continuous read or latch function is desired, in a manner analogous to the removal of transistor 52 in FIG. 4, as described previously. In addition, a second read circuit could be attached to node 25 to form a dual read port cell, or to node 29 to form a differential read cell, in a manner analogous to that shown in FIG. 6.

The operation of the circuit of FIG. 10 is similar to the operation of the circuits of FIGS. 4 and 5, except that a read operation is initiated by a low level signal on read word line 22 instead of a high level signal as in FIGS. 4 and 5, and read bit line 18 need not be precharged to a high level prior to reading.

An advantage of FIG. 10 is that the bipolar transistor 54 is emitter coupled to read bit line 18. Since the emitter of a typical bipolar transistor generally has less capacitance than the collector of the bipolar transistor, emitter coupling produces a smaller capacitance loading on the read bit line. This permits the read bit line to be switched from low to high or vice versa faster than if the bipolar transistor were collec-

tor coupled. The total switching speed of the cell will, however, also depend upon the characteristics of transistors 60 and 62.

Still another alternative embodiment of the invention is shown in FIG. 11. This circuit is similar in some ways to the circuit of FIG. 3, except that pass device 42 has been removed (replaced with a line), and a second driver 48 has been added. Removal of pass device 42 permits a continuous read operation to take place, thus causing the cell to function as a latch. Terminal 20A could receive a clock signal to write. Adding the second driver 48 permits a rapid push-pull operation to be used for driving the read bit line 18. A specific circuit implementation of the cell of FIG. 11 is shown in FIG. 12, where a second bipolar transistor 64 comprises the second driver 48 of FIG. 11. In this circuit, transistor 50 functions both as a pass/isolation device and as a device to prevent transistor 54 from saturating.

To aid in the understanding of the operation of some of the various embodiments, time-response diagrams are shown in FIGS. 13-26. FIG. 13 shows the voltages over time of various points of the circuit of FIG. 4 during a "read 0" operation. V_{RWL} is the "read enable" voltage signal sent over read word line 22 to the gate of transistor 52; V_{49} is the voltage at node 49 of the circuit; V_{45} is the voltage at control node 45; and V_{RBL} is the voltage on the write bit line 18. At time $t=0$, it is assumed that a "0" is stored in storage unit 10, meaning that internal node 25 is "high" and V_{RBL} is also "high" (having been precharged). As V_{RWL} goes "high", V_{49} and V_{45} will also rapidly go "high," indicating that transistors 52 and 50 are rapidly turning on. V_{RBL} will then be rapidly pulled "low" by transistor 54, as shown, indicating that a "0" has been sensed. It can be seen that the read operation has been accomplished very quickly, even before V_{RWL} has stabilized.

FIG. 14 shows voltages over time of the circuit of FIG. 10 during a "read 1" operation. Here, V_{RBL} is initially "low" (read bit line 18 not having been precharged), and V_{RWL} is sent from "high" to "low" to initiate a read. It can be seen that V_{RBL} rapidly goes "high" to accomplish the read.

FIG. 15 shows voltages over time of the circuit of FIG. 4 during a "write 0" operation. It is assumed that the cell is initially storing a "1," meaning that the voltage at internal node 25 (V_{25}) is "high," and the voltage at internal node 29 (V_{29}) is "low." It can be seen that both V_{25} and V_{29} undergo a very rapid transition in opposite directions, meaning that the storage unit 10 had changed state, in response to a "write enable" signal (V_{WWL}) sent over write word line 20 to the gate of transistor 32. (Write bit line 16 was initially precharged "high" in this case.)

FIG. 16 shows voltages over time of the circuit of FIG. 4 during a "write 1" operation, the cell having initially stored a "0." Again, it can be seen that a very rapid switching (and hence writing) time is accomplished

for this cell.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention. For example, the NFET transistors in the embodiments could be replaced by PFET transistors, and vice versa, with little or no modification, and the bipolar transistor 54 could be a PNP type instead of an NPN type if transistors 50, 52 and 56 are changed to PFETs. The invention may also, for example, find application in other types of memories, such as optical or electro-optical, in which case the "signals" referred to herein could be light pulses instead of voltage levels.

Claims

1. A memory cell comprising:
a storage unit (10) for storing a data signal,
a pass device (42) and a pass/isolation device (40), each having a signal path and a control terminal, the control terminal (22) of the pass device (42) being coupled to an enable line (RWL) and the control terminal (13) of the pass/isolation device (40) being coupled to an output terminal (13) of the storage unit (10),
characterized in that:
the signal paths of the pass device (42) and pass/isolation device (40) are coupled together in series between a control node (45) and a read line (RBL), and
it further comprises a driver (44) having a signal path coupled between the read line (RBL) and a constant-signal node (33), and having a control terminal coupled to the control node (45), and arranged to cause a read signal proportional to the data signal to appear on the read line in response to an enable signal on the enable line.
2. The cell of claim 1 characterized in that the storage unit (10) comprises a flip-flop formed from two cross-coupled inverters, each inverter comprising two field-effect transistors (FETs).
3. The cell of claim 1 characterized in that the control terminal of the driver (44) comprises the base of a bipolar transistor (54) and the signal path of the driver comprises a current path between the collector and the emitter of the bipolar transistor (54), the collector being coupled to the read line (RBL) and the emitter being coupled to the constant-signal node (33).
4. The cell of claim 1 characterized in that an impedance (46) is coupled between the control node

(45) and the constant-signal node (33).

5. The cell of claim 4 characterized in that the impedance (46) comprises an FET (56), the source-drain current path of which is coupled between the control node (45) and the constant-signal node, and the gate of which is coupled to the read line (RBL).
6. The cell of claim 1 characterized in that the read line (RBL) is precharged, prior to the application of the enable signal on the enable line, to a signal level different from a signal level maintained at the constant-signal node.
7. The cell of claim 1 characterized in that it further includes:
a second pass device (52B) and a second pass/isolation device (50B), each having a signal path and a control terminal, the signal paths therethrough being coupled together in series between a second control node (45B) and a second read line (RBLB), the control terminal of the second pass device (52B) being coupled to a second enable line (RWLB) and the control terminal of the second pass/isolation device (50B) being coupled to the output terminal (13) of the storage unit (10); and
a second driver (54B) having a signal path coupled between the second read line and the constant-signal node, and having a control terminal coupled to the second control node, and arranged to cause a read signal proportional to the data signal to appear on the second read line in response to a second enable signal on the second enable line;
to form a second, independent read circuit and port for the storage unit.
8. A single-bit dual-port BICMOS static RAM memory cell according to claim 4 characterized in that: it comprises a write word line (WWL) and a write bit line (WBL);
said enable and read lines are a read word line (RWL) and a read bit line (RBL), respectively;
said storage unit (10) comprises two cross-coupled inverters, the first inverter comprising first and second field-effect transistors of opposite types, the source-drain current path of the first FET (24) being coupled between a voltage source (31) and a first internal node (25), the source-drain current path of the second FET (26) being coupled between the first internal node (25) and ground, and the gate terminals of the first and second FETs being coupled together and to a second internal node (29), and the second inverter comprising third and fourth FETs of opposite types, the source-drain current path of

the third FET (28) being coupled between the voltage source (31) and the second internal node (29), the source-drain current path of the fourth FET (30) being coupled between the second internal node (29) and ground, and the gate terminals of the third and fourth FETs being coupled together and to the first internal node (25);

it comprises a write pass device comprising a fifth FET (32), the source-drain current path of which is coupled between the write bit line (WBL) and the first internal node (25), and the gate of terminal which is coupled to the write word line (WWL);

the pass device (42) and the pass/isolation device (40) comprise, respectively, sixth (52) and seventh (50) FETs, having their source-drain current paths coupled in series and between the read bit line (RBL) and said control node (45), the gate terminal of the sixth FET (52) being coupled to the read word line (RWL) and the gate terminal of the seventh FET (50) being coupled to the first internal node (25);

said impedance (46) comprises an eighth FET (56), the source-drain current path of which is coupled between the control node (45) and ground, and the gate terminal of which is coupled to the read bit line (RBL); and

said driver (44) comprises a bipolar transistor (54), the collector of which is coupled to the read bit line (RBL), the emitter of which is coupled to ground and the base of which is coupled to the control node (45).

9. The memory cell of claim 8 characterized in that the gate terminal of the seventh FET (50) is coupled to the second internal node (29) but not to the first internal node (25).

10. The memory cell of claim 8 characterized it further includes:

a second read bit line (RBLB) and a second read word line (RWLB);

a second pass device and a second pass/isolation device comprising, respectively, ninth (52B) and tenth (50B) FETs, having their source-drain current paths coupled in series and between the second read bit line (RBLB) and a second control node (45B), the gate terminal of the ninth FET (52B) being coupled to the second read word line (RWLB) and the gate terminal of the tenth FET (50B) being coupled to the second internal node (29);

a second impedance comprising an eleventh FET (56B), the source-drain current path of which is coupled between the second control node (45B) and ground, and the gate terminal of which is coupled to the second read bit line (RBLB); and a second driver comprising a second bipolar tran-

sistor (54B), the collector of which is coupled to the second read bit line (RBLB), the emitter of which is coupled to ground and the base of which is coupled to the second control node (45B); to form a memory cell having a differential read capability.

11. A memory device comprising:

a common read bit line (RBL);

a plurality of read word lines (RWL, RWL');

a plurality of single-bit storage units (10, 10'), each having an output (13, 13') coupled to the gate terminal of a first field-effect transistor (FET) (50, 50') associated with such storage unit, such first FET comprising a pass/isolation device, the source-drain current path of such FET being coupled at one end to one end of the source-drain current path of a second FET (52, 52') associated with such storage unit, such second FET comprising a pass device, the other end of such current path being coupled to the common read line (RBL), the gate of the second FET being coupled to a particular read word line (RWL, RWL');

characterized in that:

the source-drain current path of each said first FET (50, 50') is coupled at the other end to a common control line (47),

it comprises a bipolar transistor (54) comprising a common bit line driver device, the collector of which is coupled to the common read bit line (RBL), the emitter of which is coupled to ground and the base of which is coupled to the common control line (47), and

it comprises an FET (56) comprising an impedance device, the source-drain current path of which is coupled between the common control line (47) and ground, and the gate of which is coupled to the common read bit line (RBL).

Patentansprüche

1. Speicherzelle umfassend:

eine Speichereinheit (10) zum Speichern eines Datensignals,

ein Durchschaltbauelement (42) und ein Durchschalt-/Trennbauelement (40), jedes einen Signalpfad und einen Steueranschluß besitzend, wobei der Steueranschluß (22) des Durchschaltbauelementes (42) an eine Freigabeleitung (RWL) angeschlossen ist und wobei der Steueranschluß (13) des Durchschalt-/Trennbauelementes (40) an einen Ausgangsanschluß (13) der Speichereinheit (10) angeschlossen ist, dadurch gekennzeichnet, daß:

die Signalpfade des Durchschaltbauelementes (42) und des Durchschalt-/Trennbauelementes

- (40) in Reihe zwischen einen Steuerknoten (45) und eine Leseleitung (RBL) geschaltet sind und daß sie weiterhin einen Treiber (44) umfaßt, dessen Signalpfad zwischen der Leseleitung (RBL) und einem Knoten mit konstantem Pegel (33) liegt und der einen Steueranschluß besitzt, welcher an den Steuerknoten (45) angeschlossen ist, wobei er so verschaltet ist, daß er ein Lesesignal erzeugt, das dem Datensignal proportional ist und in Abhängigkeit von einem Freigabesignal auf der Freigabeleitung auf der Leseleitung bereitgestellt wird.
2. Speicherzelle nach Anspruch 1, dadurch gekennzeichnet, daß die Speichereinheit (10) ein Flip-Flop umfaßt, das aus zwei über Kreuz verschalteten Invertern gebildet wird, wobei jeder Inverter zwei Feldeffekttransistoren (FETs) umfaßt.
 3. Speicherzelle nach Anspruch 1, dadurch gekennzeichnet, daß der Steueranschluß des Treibers (44) durch die Basis eines Bipolartransistors (54) gebildet wird und daß der Signalpfad des Treibers den Strompfad zwischen Kollektor und Emitter des Bipolartransistors (54) umfaßt, wobei der Kollektor an die Leseleitung (RBL) angeschlossen ist und wobei der Emitter an den Knoten mit konstantem Pegel (33) angeschlossen wird.
 4. Speicherzelle nach Anspruch 1, dadurch gekennzeichnet, daß eine Impedanz (46) zwischen den Steuerknoten (45) und den Knoten mit konstantem Pegel geschaltet ist.
 5. Speicherzelle nach Anspruch 4, dadurch gekennzeichnet, daß die Impedanz (46) einen FET (56) umfaßt, wobei dessen Source-Drain-Strompfad zwischen den Steuerknoten (45) und den Knoten mit konstantem Pegel geschaltet ist und wobei dessen Gate an die Leseleitung (RBL) angeschlossen ist.
 6. Speicherzelle nach Anspruch 1, dadurch gekennzeichnet, daß die Leseleitung, bevor ein Freigabesignal an die Freigabeleitung angelegt wird, auf einen Signalpegel vorgeladen wird, der sich von dem Pegel an dem Knoten mit konstantem Pegel unterscheidet.
 7. Speicherzelle nach Anspruch 1, dadurch gekennzeichnet, daß sie weiterhin enthält:
ein zweites Durchschaltbauelement (52B) und ein zweites Durchschalt-/Trennbauelement (50B), jedes einen Signalpfad und einen Steueranschluß besitzend, wobei deren Signalpfade in Reihe zwischen einen zweiten Steuerknoten (45B) und eine zweite Leseleitung (RBLB) geschaltet sind, wobei der Steueranschluß des zweiten Durchschaltbauelementes (52B) an eine zweite Freigabeleitung (RWLB) angeschlossen ist und wobei der Steueranschluß des zweiten Durchschalt-/Trennbauelementes (50B) an den Ausgangsanschluß (13) der Speichereinheit (10) angeschlossen ist; und
einen zweiten Treiber (54B), dessen Signalpfad zwischen der zweiten Leseleitung und dem Knoten mit konstantem Pegel liegt und der einen Steueranschluß besitzt, welcher an den zweiten Steuerknoten angeschlossen ist, wobei er so verschaltet ist, daß er ein Lesesignal erzeugt, das dem Datensignal proportional ist und in Abhängigkeit von einem zweiten Freigabesignal auf der zweiten Freigabeleitung auf der zweiten Leseleitung bereitgestellt wird;
um eine zweite unabhängige Leseschaltung und ein unabhängiges Port für die Speichereinheit zu bilden.
 8. Eine Einzel-Bit Dual-Port BICMOS statische RAM-Speicherzelle nach Anspruch 4, dadurch gekennzeichnet, daß
sie eine Wort-Schreibleitung (WWL) und eine Bit-Schreibleitung (WBL) umfaßt;
die Freigabe- und Leseleitungen eine Wort-Leseleitung (RWL) beziehungsweise eine Bit-Leseleitung (RBL) darstellen;
die Speichereinheit (10) zwei über Kreuz verschaltete Inverter umfaßt, der erste Inverter umfaßt erste und zweite Feldeffekttransistoren entgegengesetzten Typs, wobei der Source-Drain-Strompfad des ersten FETs (24) zwischen eine Spannungsquelle (31) und einen ersten internen Knoten (25) geschaltet ist, wobei der Source-Drain-Strompfad des zweiten FETs (26) zwischen den ersten internen Knoten (25) und Masse geschaltet ist und wobei die Gateanschlüsse des ersten und zweiten FETs miteinander und mit einem zweiten internen Knoten (29) verbunden sind und der zweite Inverter dritte und vierte FETs entgegengesetzten Typs umfaßt, wobei der Source-Drain-Strompfad des dritten FETs (28) zwischen die Spannungsquelle (31) und den zweiten internen Knoten (29) geschaltet ist, wobei der Source-Drain-Strompfad des vierten FETs (30) zwischen den zweiten internen Knoten (29) und Masse geschaltet ist und wobei die Gateanschlüsse des dritten und vierten FETs miteinander und mit dem ersten internen Knoten (25) verbunden sind;
sie ein Schreiben-Durchschaltbauelement umfaßt, das einen fünften FET (32) enthält, wobei der Source-Drain-Strompfad dieses Bauelementes zwischen die Bit-Schreibleitung (WBL) und den ersten internen Knoten (25) geschaltet ist und wobei dessen Gateanschluß an die Wort-

Schreibleitung (WWL) angeschlossen ist; das Durchschaltbauelement (42) beziehungsweise das Durchschalt-/Trennbauelement (40) sechste (52) und siebente (50) FETs umfassen, wobei deren Source-Drain-Strompfade in Reihe zwischen die Bit-Leseleitung (RBL) und den zweiten Steuerknoten (45) geschaltet sind, wobei der Gateanschluß des sechsten FETs (52) an die Wort-Leseleitung (RWL) angeschlossen ist und wobei der Gateanschluß des siebenten FETs (50) an den ersten internen Knoten (25) angeschlossen ist; die Impedanz (46) einen achten FET (56) umfaßt, dessen Source-Drain-Strompfad zwischen den Steuerknoten (45) und Masse geschaltet ist und dessen Gateanschluß an die Bit-Leseleitung (RBL) angeschlossen ist; und der Treiber (44) einen Bipolartransistor (54) umfaßt, dessen Kollektor an die Bit-Leseleitung (RBL) angeschlossen ist, dessen Emitter mit Masse verbunden ist und dessen Basis an den Steuerknoten (45) angeschlossen ist.

9. Speicherzelle nach Anspruch 8, dadurch gekennzeichnet, daß der Gateanschluß des siebenten FETs (50) an den zweiten internen Knoten (29) und nicht an den ersten internen Knoten (25) angeschlossen ist.

10. Speicherzelle nach Anspruch 8, dadurch gekennzeichnet, daß sie weiterhin enthält: eine zweite Bit-Leseleitung (RBLB) und eine zweite Wort-Leseleitung (RWLB); ein zweites Durchschaltbauelement und ein zweites Durchschalt-/Trennbauelement, umfassend neunte (52B) und zehnte (50B) FETs, wobei deren Source-Drain-Strompfade zwischen der zweiten Bit-Leseleitung (RBLB) und einem zweiten Steuerknoten (45B) in Reihe geschaltet sind, wobei der Gateanschluß des neunten FETs (52B) an die zweite Wort-Leseleitung (RWLB) angeschlossen ist und wobei der Gateanschluß des zehnten FETs (50B) an den zweiten internen Knoten (29) angeschlossen ist; eine zweite Impedanz, die einen elften FET (56B) umfaßt, dessen Source-Drain-Strompfad zwischen den zweiten Steuerknoten (45B) und Masse geschaltet ist und dessen Gateanschluß an die zweite Bit-Leseleitung (RBLB) angeschlossen ist; und einen zweiten Treiber, der einen zweiten Bipolartransistor (54B) umfaßt, dessen Kollektor an die zweite Bit-Leseleitung (RBLB) angeschlossen ist, dessen Emitter an Masse angeschlossen ist und dessen Basis an den zweiten Steuerknoten (45B) angeschlossen ist; um eine Speicherzelle zu bilden, bei der ein Differenzsignal ausgelesen werden kann.

11. Speichervorrichtung umfassend: eine gemeinsame Bit-Leseleitung (RBL); eine Anzahl Wort-Leseleitungen (RWL, RWL'); eine Anzahl Einzel-Bit-Speichereinheiten (10, 10'), von denen jede einen Ausgang (13, 13') besitzt, der mit dem Gateanschluß eines ersten Feldeffekttransistors (FET) (50, 50') verbunden ist, welcher dieser Speichereinheit zugeordnet ist, wobei dieser erste FET ein Durchschalt-/Trennbauelement umfaßt, dessen Source-Drain-Strompfad auf einer Seite mit einer Seite des Source-Drain-Strompfades eines zweiten FETs (52, 52') verschaltet ist und dessen andere Strompfadseite an die gemeinsame Bit-Leseleitung (RBL) angeschlossen ist, und wobei der Gateanschluß des zweiten FETs an eine spezielle Wort-Leseleitung (RWL, RWL') angeschlossen ist; dadurch gekennzeichnet, daß: der Source-Drain-Strompfad jedes ersten FETs (50, 50') mit der anderen Seite an eine gemeinsame Steuerleitung (47) angeschlossen ist, sie einen Bipolartransistor (54) umfaßt, der ein Treiberbauelement für eine gemeinsame Bitleitung darstellt, wobei dessen Kollektor an die gemeinsame Bit-Leseleitung (RBL) angeschlossen ist, wobei dessen Emitter an Masse angeschlossen ist und wobei dessen Basis an die gemeinsame Steuerleitung (47) angeschlossen ist und daß sie einen FET (56) umfaßt, der ein Impedanzelement darstellt, wobei dessen Source-Drain-Strompfad zwischen die gemeinsame Steuerleitung (47) und Masse geschaltet ist und wobei dessen Gate an die gemeinsame Bit-Leseleitung angeschlossen ist.

Revendications

1. Cellule de mémoire comprenant :
un élément de stockage (10) pour stocker un signal de données
un dispositif de passage (42) et un dispositif de passage/isolation (40), ayant chacun un trajet de signal et une borne de commande, la borne de commande (22) du dispositif de passage (42) étant connectée à une ligne de mise en condition (RWL) et la borne de commande (13) du dispositif (40) de passage/isolation étant reliée à une borne de sortie (13) de l'élément de stockage (10),
caractérisée en ce que :
les trajets de signal du dispositif de passage (42) et du dispositif de passage/isolation (40) sont reliés en séries entre le noeud de commande (45) et la ligne de lecture (RBL), et
elle comprend en outre un circuit d'attaque (44) ayant un trajet de signal placé entre la ligne de lecture (RBL) et un noeud à signal cons-

- tant (33), et ayant une borne de commande reliée au noeud de commande (45), et conçu pour entraîner l'apparition d'un signal de lecture proportionnel au signal de données sur la ligne de lecture en réponse à un signal de mise en condition sur la ligne de mise en condition.
- 5
2. Cellule selon la revendication 1 caractérisée en ce que l'élément de stockage (10) comprend un flip-flop formé de deux inverseurs en couplage croisé, chaque inverseur comprenant deux transistors à effet de champ (FET).
- 10
3. Cellule selon la revendication 1 caractérisée en ce que la borne de commande du dispositif d'attaque (44) comprend la base d'un transistor bi-polaire (54) et le trajet de signal du dispositif d'attaque comprend un trajet de courant entre le collecteur et l'émetteur du transistor bi-polaire (54), le collecteur étant relié à la ligne de lecture (RBL) et l'émetteur étant relié au noeud à signal constant (33).
- 15
4. Cellule selon la revendication 1 caractérisée en ce que une impédance (46) est placée entre le noeud de commande (45) et le noeud à signal constant (33).
- 20
5. Cellule selon la revendication 4 caractérisée en ce que l'impédance (46) comprend un FET (56), dont le trajet de courant source-drain est placé entre le noeud de commande (45) et le noeud à signal constant, et dont la grille est reliée à la ligne de lecture (RBL).
- 25
6. Cellule selon la revendication 1 caractérisée en ce que la ligne de lecture (RBL) est pré-chargée, avant l'application du signal de mise en condition sur la ligne de mise en condition, à un niveau de signal différent du niveau de signal maintenu au noeud à signal constant.
- 30
7. Cellule selon la revendication 1 caractérisée en ce qu'elle comprend en outre :
- 35
- un second dispositif de passage (52B) et un second dispositif de passage/isolation (50B), ayant chacun un trajet de signal et une borne de commande, les trajets de signaux étant reliés en série entre un second noeud de commande (45B) et une seconde ligne de lecture (RBLB), la borne de commande du second dispositif de passage (52B) étant reliée à une seconde ligne de mise en condition (RWLB), et la borne de commande du second dispositif de passage/isolation (50B) étant reliée à la borne de sortie (13) de l'élément de stockage (10) ; et
- 40
- un second dispositif d'attaque (54B) ayant un trajet de signal placé entre la seconde ligne de
- 45
- lecture et le noeud à signal constant, et ayant une extrémité de commande reliée au second noeud de commande, et conçu pour entraîner l'apparition d'un signal de lecture proportionnel au signal de données sur la seconde ligne de lecture en réponse à un second signal de mise en condition sur la seconde ligne de mise en condition ;
- de façon à former un second circuit de lecture et port indépendant pour l'élément de stockage.
8. Cellule de mémoire RAM statique BICMOS à port-dual à bit unique selon la revendication 4 caractérisée en ce que :
- elle comprend une ligne d'écriture de mot (WWL) et une ligne d'écriture de bit (WBL) ;
- lesdites lignes de lecture et de mise en condition étant respectivement une ligne de lecture de mot (RWL) et une ligne de lecture de bit (RBL), respectivement ;
- ledit élément de stockage (10) comprend deux inverseurs en couplage croisé, le premier inverseur comprenant un premier et un second transistors à effet de champ de types opposés, le trajet de courant source-drain du premier FET (24) étant placé entre une source de tension (31) et un premier noeud interne (25), le trajet de courant source-drain du second FET (26) étant placé entre le premier noeud interne (25) et la masse, et les bornes de grille des premier et second FETs étant reliées entre elles ainsi qu'à un second noeud interne (29), et le second inverseur comprenant des troisième et quatrième FETs de types opposés, le trajet de courant source-drain du troisième FET (28) étant placé entre la source de tension (31) et le second noeud interne (29), le trajet de courant source-drain du quatrième FET (30) étant placé entre le second noeud interne (29) et la masse, et les bornes de grille des troisième et quatrième FETs étant reliées entre elles et au premier noeud interne (25) ;
- elle comprend un dispositif de passage d'écriture comprenant un cinquième FET (32), dont le trajet de courant source-drain est placé entre la ligne d'écriture de bit (WBL) et le premier noeud interne (25), et la borne de grille reliée à la ligne d'écriture de mot (WWL) ;
- le dispositif de passage (42) et le dispositif de passage/isolation (40) comprennent respectivement, les sixième (52) et septième (50) FETs, dont les trajets de courant source-drain sont placés en séries entre la ligne de lecture de bit (RBL) et ledit second noeud de commande (45), l'électrode de grille du sixième FET (52) étant reliée à la ligne de lecture de mot (RWL) et l'électrode de grille du septième FET (50) étant reliée au premier noeud interne (25) ;
- ladite impédance (46) comprend un huitième

- me FET (56) dont le trajet de courant source-drain est placé entre le noeud de commande (45) et la masse, et l'électrode de grille est reliée à la ligne de lecture de bit (RBL) ; et
- ledit dispositif d'attaque (44) comprend un transistor bipolaire (54), dont le collecteur est relié à la ligne de lecture de bit (RBL), dont l'émetteur est relié à la masse et dont la base est reliée au noeud de commande (45).
9. Cellule de mémoire selon la revendication 8 caractérisée en ce que l'électrode de grille du septième transistor FET (50) est reliée au second noeud interne (29) mais pas au premier noeud interne (25).
10. Cellule de mémoire selon la revendication 8 caractérisée en ce qu'elle comprend en outre :
- une seconde ligne de lecture de bit (RBLB) et une seconde ligne de lecture de mot (RWBL) ;
 - un second dispositif de passage et un second dispositif de passage/isolation comprenant respectivement, un neuvième (52B) et un dixième (50B) FETs, dont les trajets de courant source-drain sont reliés en série entre la seconde ligne de lecture de bit (RBLB) et un second noeud de commande (45B), l'électrode de grille du neuvième FET (52B) étant reliée à la seconde ligne de lecture de mot (RWLB) et l'électrode de grille du dixième FET (50B) étant reliée au second noeud interne (29) ;
 - une seconde impédance comprenant un onzième FET (56B), dont le circuit de courant source-drain est placé entre le second noeud de commande (45B) et la masse, et dont l'électrode de grille est reliée à la seconde ligne de lecture de bit (RBLB) ; et
 - un second dispositif d'attaque comprenant un second transistor bi-polaire (54B) dont le collecteur est relié à la seconde ligne de lecture de bit (RBLB), dont l'émetteur est relié à la masse et dont la base est reliée au second noeud de commande (45B) ;
 - de façon à former une cellule de mémoire offrant une possibilité de lecture différentielle.
11. Elément de mémoire comprenant :
- une ligne de lecture de bit commune (RBL) ;
 - un ensemble de lignes de lecture de mot (RWL, RWL') ;
 - un ensemble d'éléments de stockage à un bit (10, 10'), ayant chacun une sortie (13, 13') reliée à la grille d'un premier transistor à effet de champ (FET) (50, 50') associées à chacun desdits éléments de stockage, ledit premier FET comprenant un dispositif de passage/isolation, le trajet de courant source-drain d'un tel FET étant

relié d'une part à une extrémité du circuit de courant source-drain d'un second transistor FET (52, 52') associé à un tel élément de stockage, un tel second FET comprenant un dispositif de passage, l'autre extrémité d'un tel circuit de courant étant reliée à la ligne de lecture commune (RBL), la grille du second FET étant reliée à une ligne de lecture de mot particulier (RWL, RWL') ;

caractérisé en ce que :

le circuit de courant source-drain de chacun desdits premier FET (50, 50') est relié à l'autre extrémité d'une ligne de commande commune (47),

il comprend un transistor bi-polaire (54) comprenant un dispositif d'attaque de ligne de bit commun, dont le collecteur est relié à la ligne de lecture de bit commune (RBL), dont l'émetteur est relié à la masse et dont la base est reliée à la ligne de commande commune (47), et

il comprend un FET (56) comprenant un élément d'impédance, dont le circuit de courant source-drain est relié entre la ligne de commande commune (47) et la masse, et dont la grille est reliée à la ligne de lecture de bit commune (RBL).

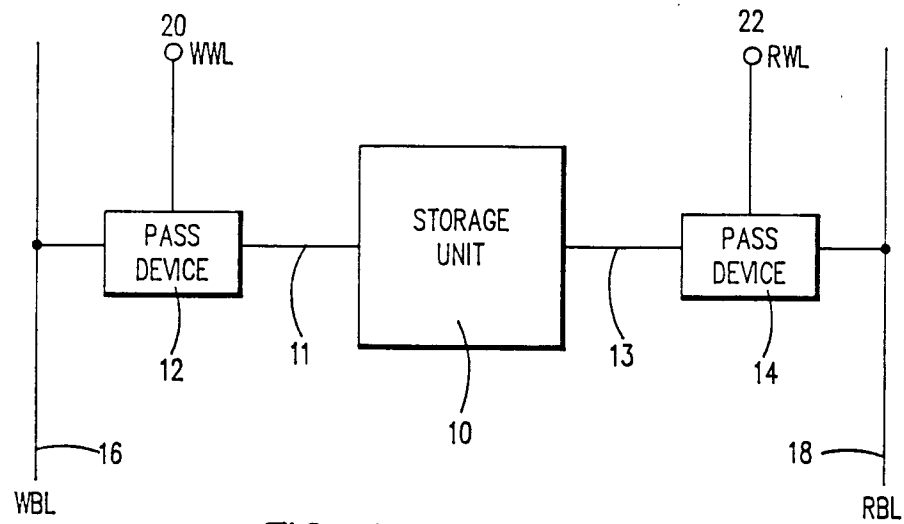


FIG. 1 (PRIOR ART)

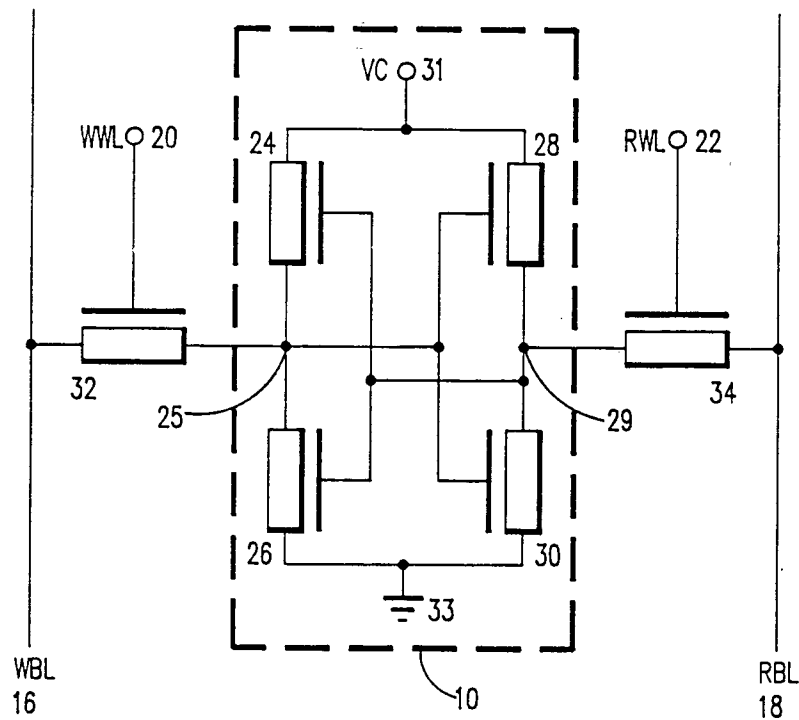
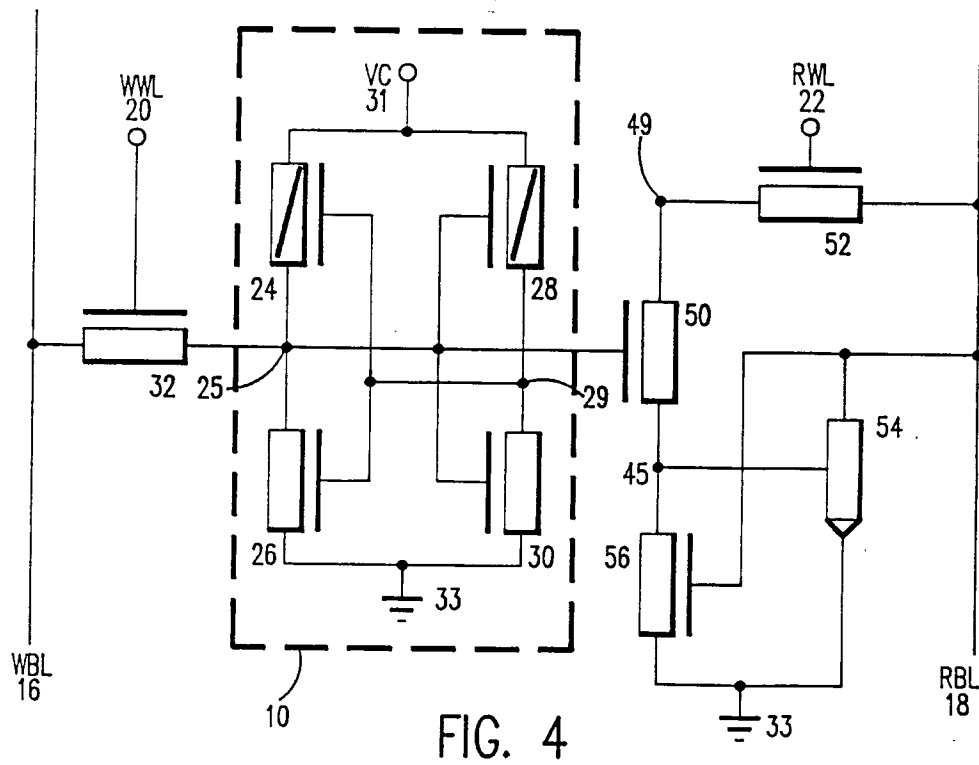
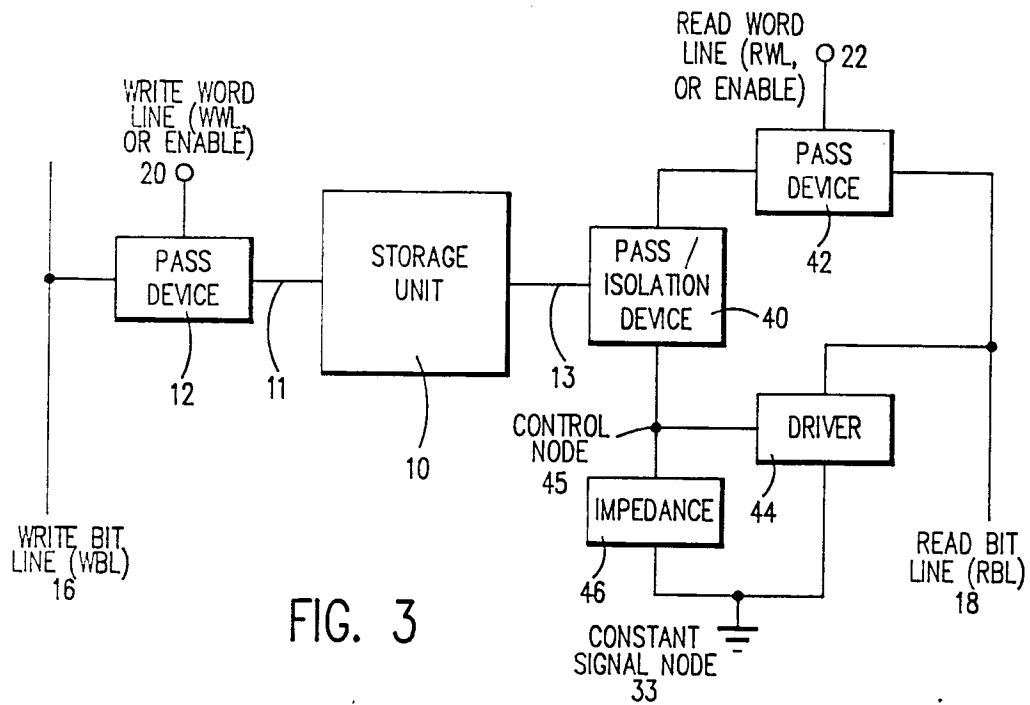


FIG. 2 (PRIOR ART)



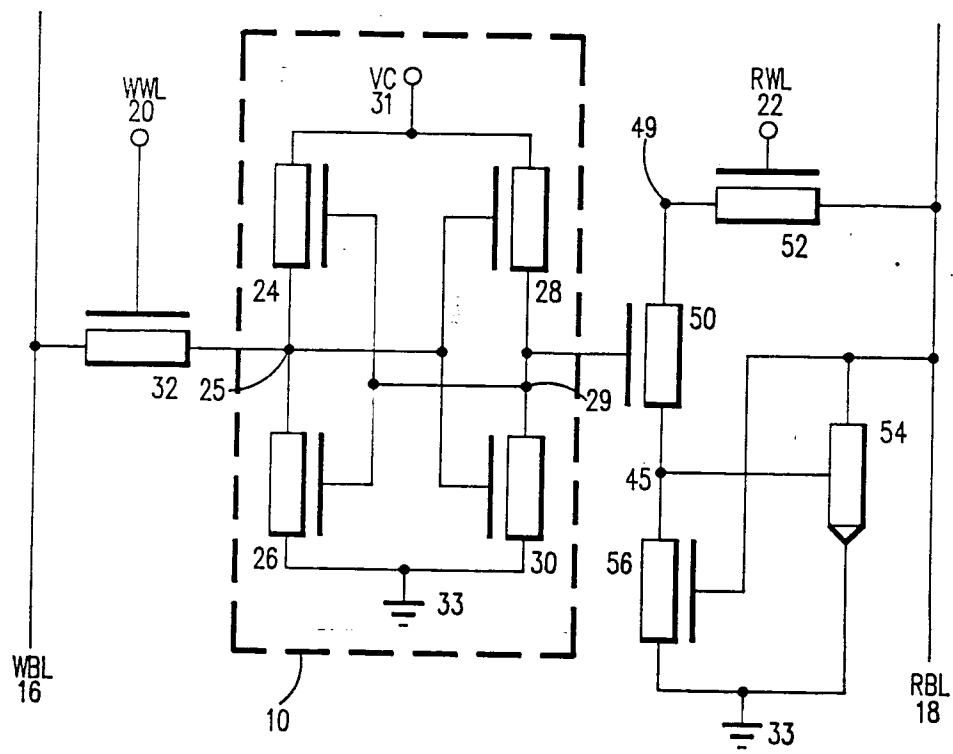


FIG. 5

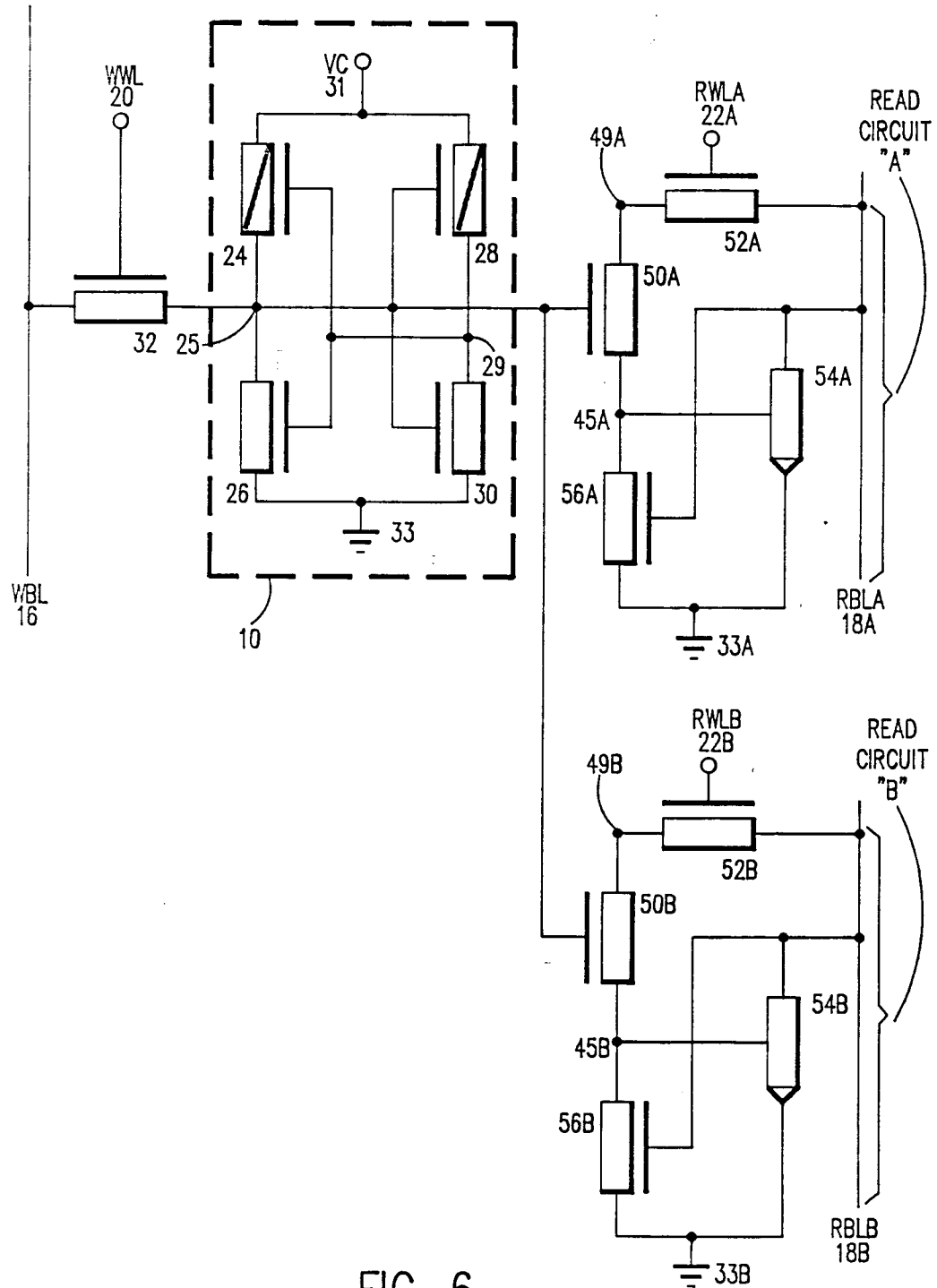


FIG. 6

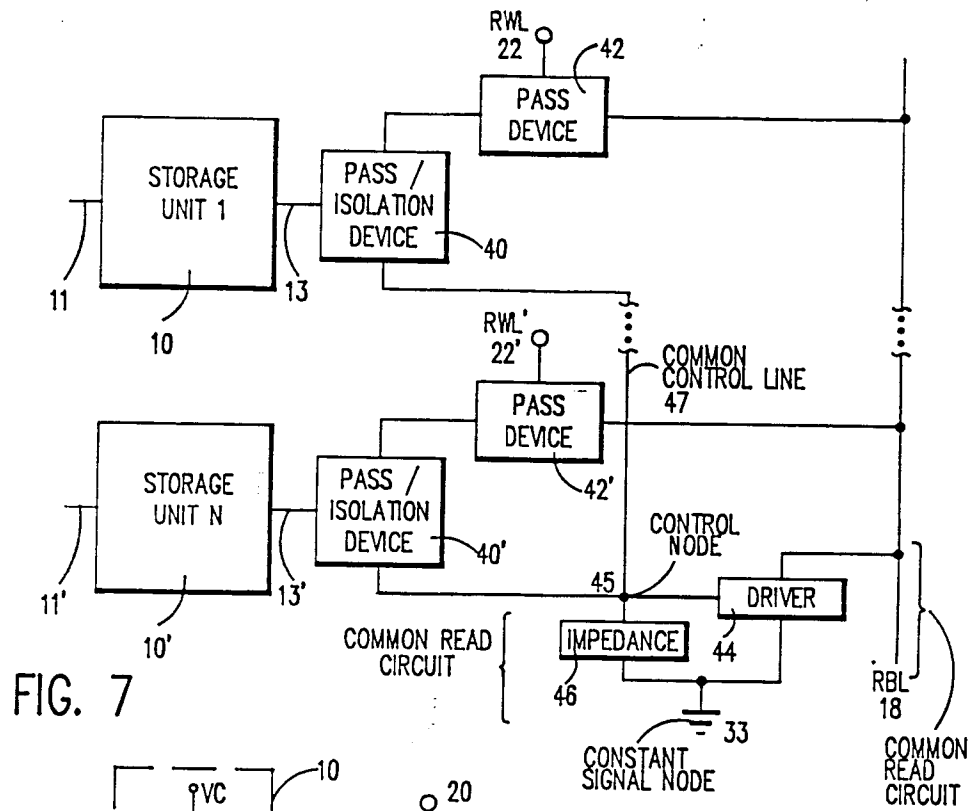


FIG. 7

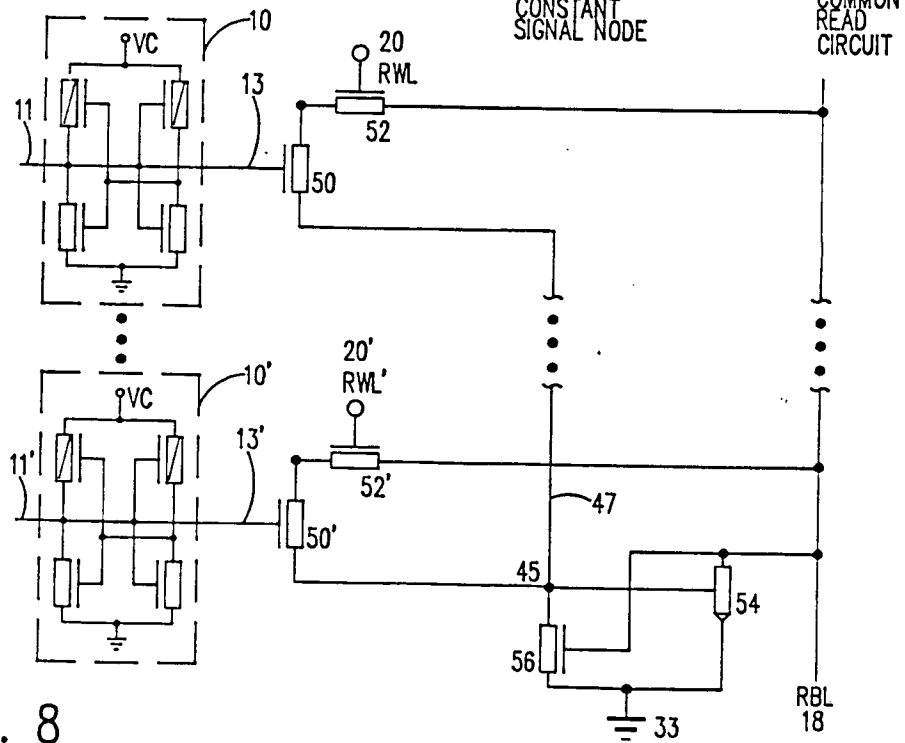


FIG. 8

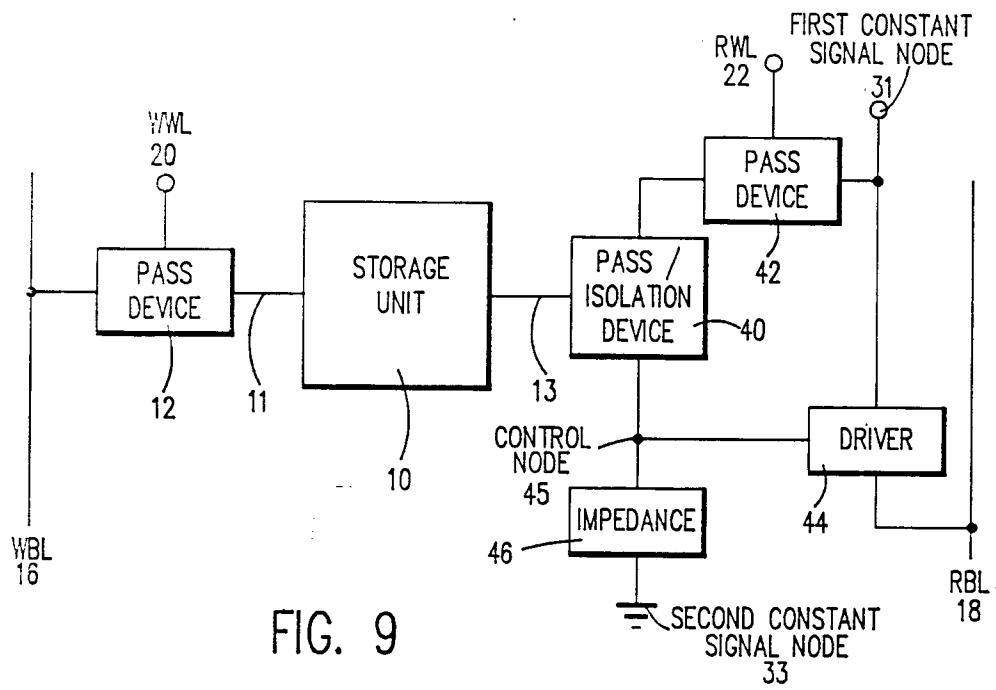


FIG. 9

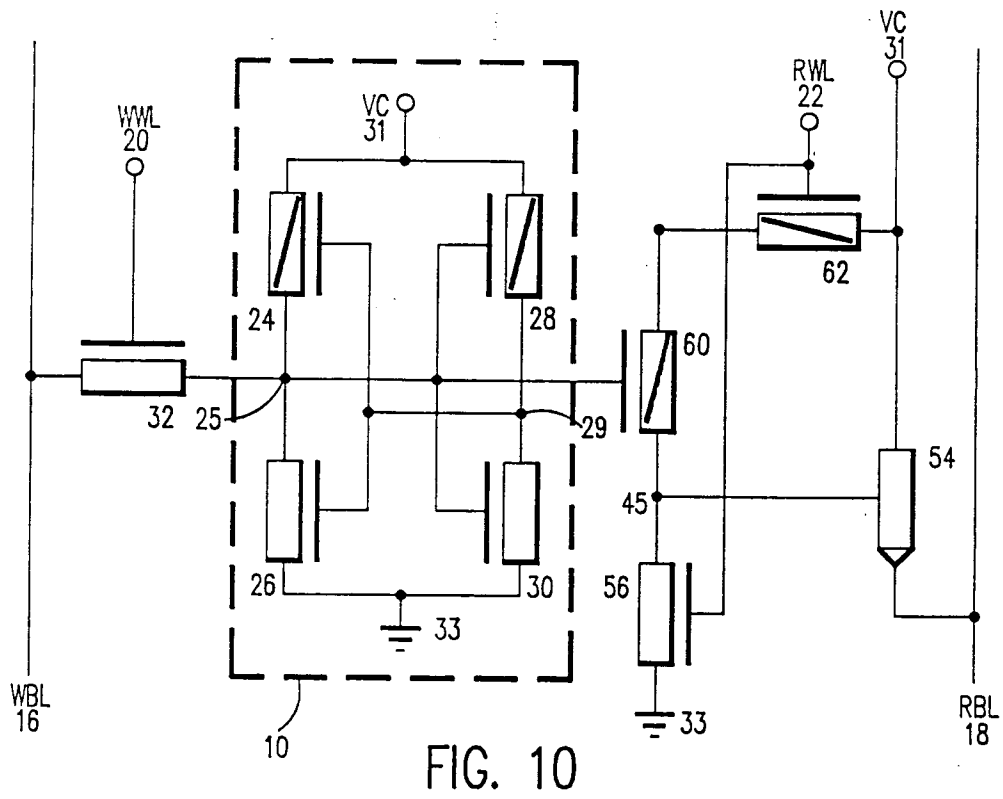


FIG. 10

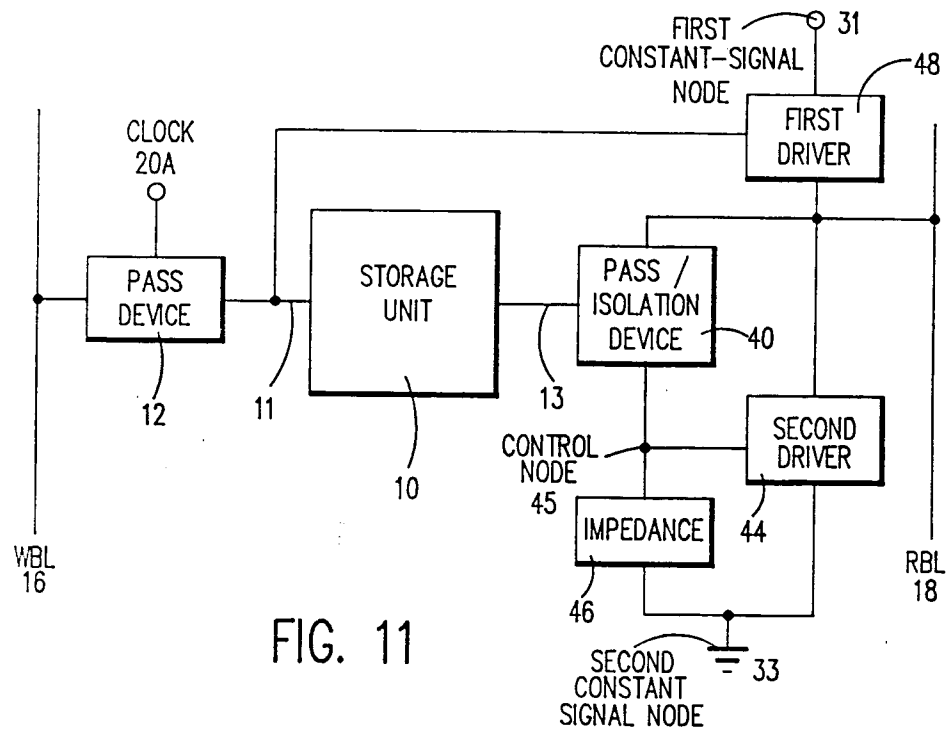


FIG. 11

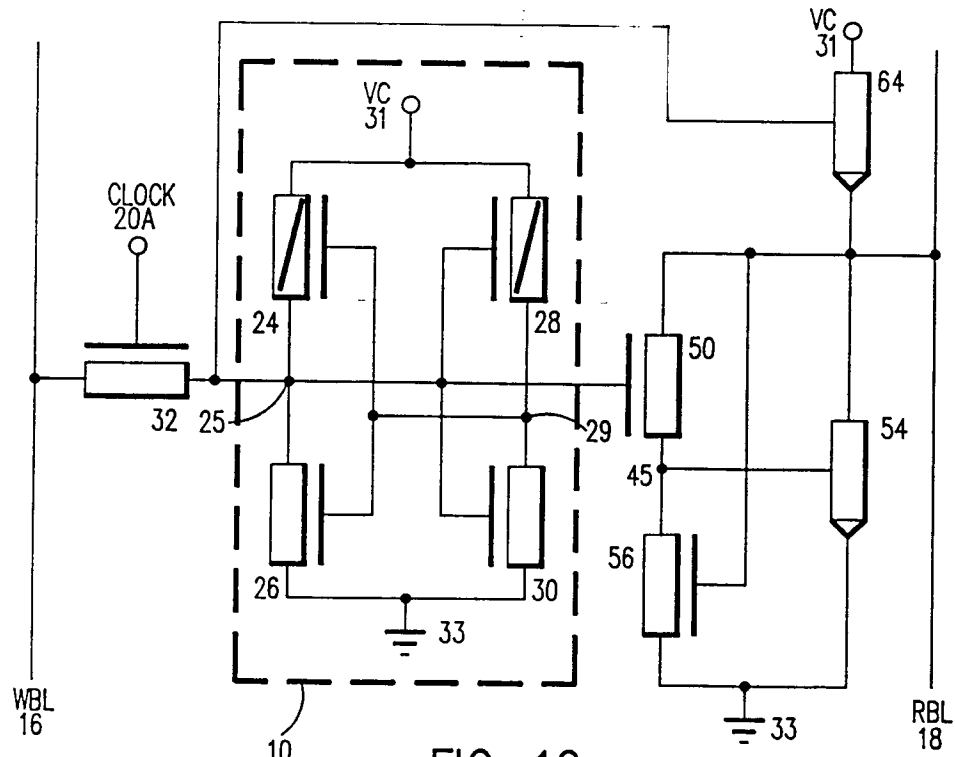


FIG. 12

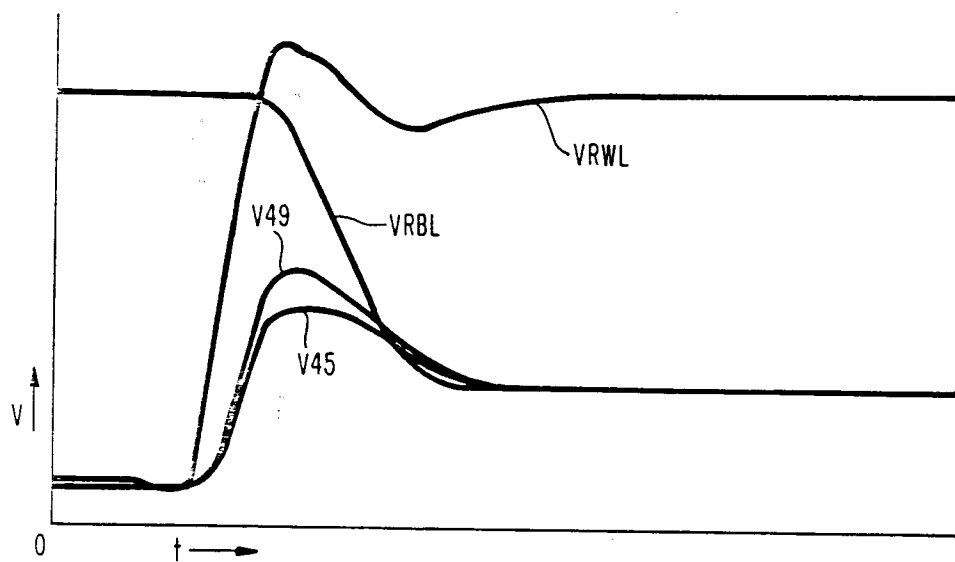


FIG. 13

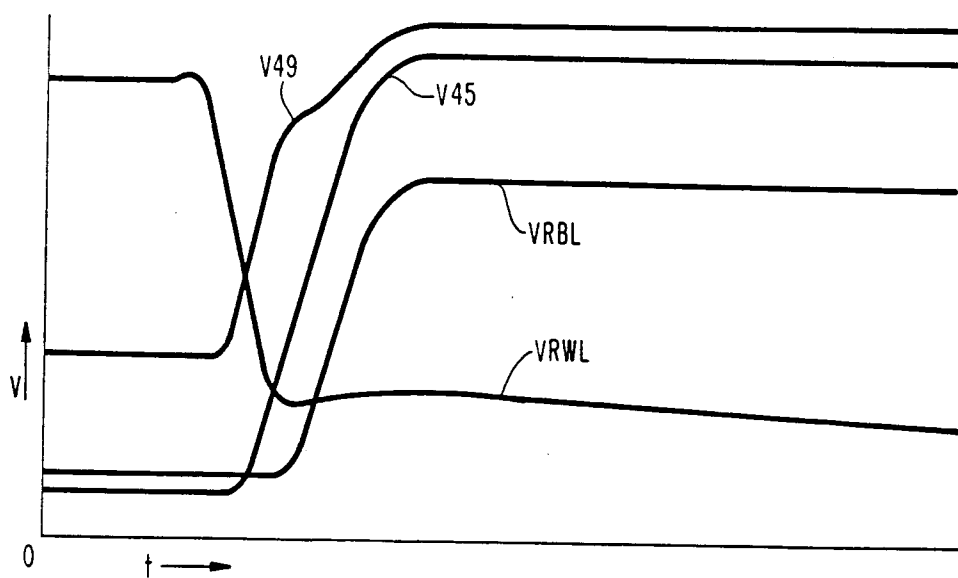


FIG. 14

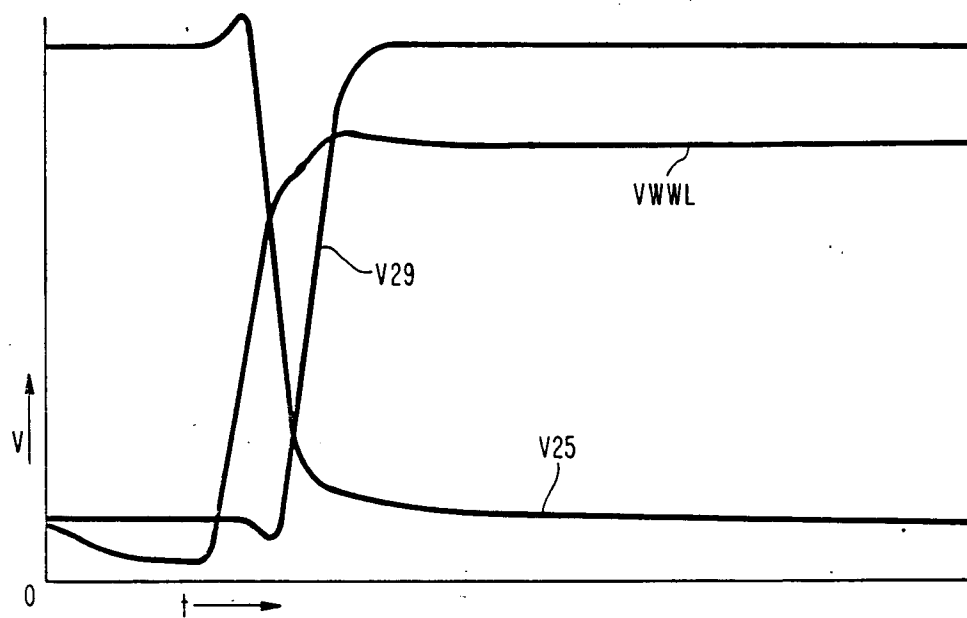


FIG. 15

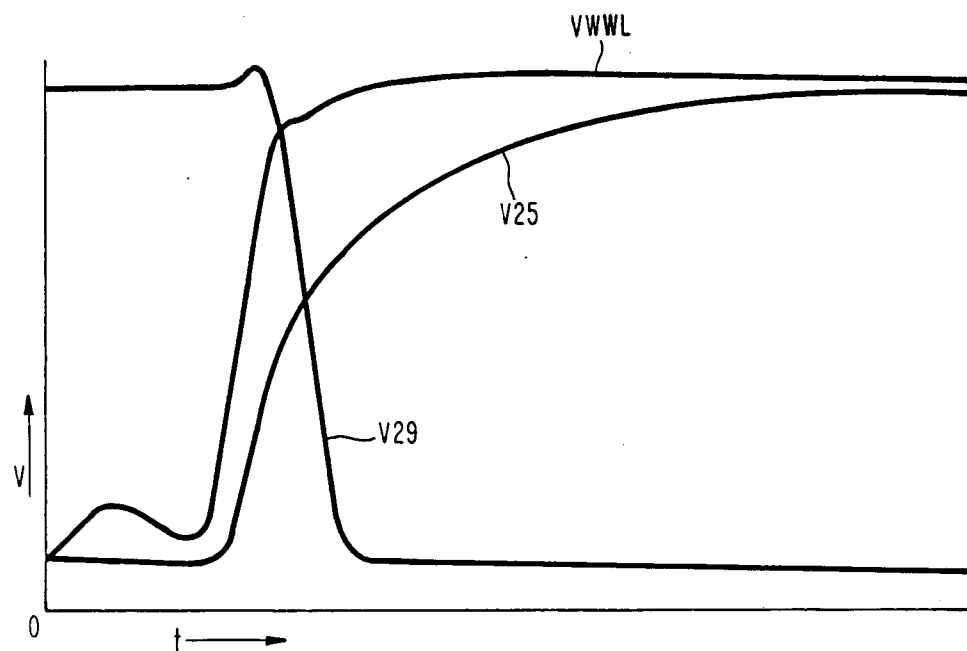


FIG. 16