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(54) Image memory control apparatus.

(57) An image memory control apparatus containing a memory device (220) for storing image data and control data. The apparatus includes a display address generator (210) for generating addresses of the stored image data, a display address selector (211) for selecting desired image data addresses sequentially in a fixed order, a control address generator (100) for generating addresses of the stored control data, an access selector (220) for combining the image data addresses and the control data address and a controller (214) for controlling the access selector (220), wherein the controller (214) includes a circuit (214) for shifting the control of the access selector (220) to immediately access the stored control data in response to an access requesting signal.

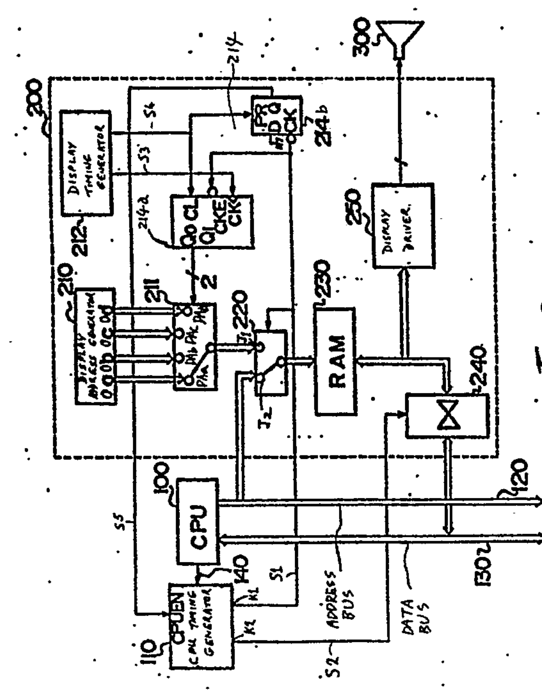

Fig. 3

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IMAGE MEMORY CONTROL APPARATUS

The present invention relates to an image memory control apparatus, and more particularly to an image memory control apparatus for use in a cyclic steal image display system.

Recently, an image memory control apparatus for use in a cyclic steal image display system has been developed. Such a system operates to insert an interval allowing a central processing unit (hereinafter, referred to as CPU) to access an image memory during an image data processing period. The system controls an image memory so that a display image, such as a teletext image, a videotex image or a computer graphic image, is appropriately displayed, in connection with the image memory control apparatus.

An image memory control apparatus for a cyclic steal image display system know to the applicant is constructed as shown in Fig. 1. Such a conventional apparatus is used in the Toshiba image control IC; TC9017N.

In Fig. 1, the conventional image memory control apparatus comprises a CPU 100, a CPU timing generator 110 and an image memory controller 200. The image memory controller 200 comprises an address generator 210, a display timing generator 212, an address selector controller 213, an address selector 211, an access selector 220, a RAM (random access memory) 230, a data buffer 244 and a display driver 250. The display driver 250 is connected to an image display, such as a CRT 300. The address selector controller 213 includes a 2-bit counter 213a.

The CPU 100 provides an access requesting signal 140 to the CPU timing generator 110. The CPU timing generator 110 receives an access control signal S1 from the display timing generator 212 in the image memory controller 200 and supplies a data access signal S2 to the data buffer 240 in the image memory controller 200. The CPU 100 has an address bus 120 and a data bus 130 which are coupled to the image memory controller 200. That is, the address bus 120 is coupled to the access selector 220 for accessing control data stored in the RAM 230 through the access selector 220. When control addresses CA are applied to the RAM 230, control data is read from the RAM 230 and supplied to the data buffer 240 and the display driver 250. The data bus 130 is coupled to the data buffer 240. In addition, the address bus 120 and the data bus 130 are coupled to usable circuits outside this image memory control apparatus.

In the image memory controller 200, the address generator 210 generates four display addresses DAa, DAb, DAc and DAd, associated with image data stored in the RAM 230. These display addresses DAa, DAb, DAc and DAd are applied to four switchable input terminals Ia, Ib, Ic and Id or the address selector 211, respectively. The output terminal of the address selector 211 is coupled to a first input terminal J1 of the access selector 220, while a second input terminal J2 of the access selector 220 is coupled to the address bus 120 for receiving an address from the CPU 100. The output terminal of the access selector 220 is coupled to an address input of the RAM 230. The RAM 230 communicates with the data buffer 240 and the display driver 250 through a controller data bus 260.

The display timing generator 212 generates a clock signal S3, a clear signal S4 and the access control signal S1. The clock signal S3 and the clear signal S4 are applied to a clock terminal CK and a clear terminal CL of the 2-bit counter 213a. The access control signal S1 is applied to the access selector 220, as well as to the CPU timing generator 110.

The operation of the image memory control apparatus of Fig. 1 will be briefly explained hereinafter, in reference to Fig. 2. Fig. 2 shows timing charts of signals in the apparatus. The apparatus reads image data from the RAM 230. The image data is converted to color video data, e.g., R-data (red data), G-data (green data) and B-data (blue data) by the display driver 250. The display driver 250 supplies the color video data to the CRT 300.

Graph 2A in Fig. 2 shows the clock signal S3 generated by the display timing generator 212. The 2-bit counter 213a counts up the clock signal S3. Hereupon, as an example it is supposed that the image data to be read from the RAM 230 is constituted by four lots of image data IDa, IDb, IDc and IDd. This image data IDa, IDb, IDc and IDd is commonly used for decoding the color video date, i.e., the R-data, the G-data and the B-data. The image data IDa, IDb, IDc and IDd is read by the display addresses DAa, DAb, DAc and DAd given to the RAM 230. One cycle for reading the set of the four lots of image data IDa, IDb, IDc and IDd is called herein a unit display cycle. The unit display cycle includes the image data access periods of the image data IDa, IDb, IDc and IDd and a CPU access period, as shown in Graph 2B of Fig. 2. Graph 2B shows a RAM address output from the access selector 220. The CPU access period is shown by "CPU" on Graph 2B.

The address generator 210 generates the display addresses DAa, DAb, DAc and DAd from its output terminals Oa, Ob, Oc and Od. Thus the display addresses DAa, DAb, DAc and DAd are applied in parallel to the input terminals Ia, Ib, Ic and Id of the address selector 211. These input terminals Ia, Ib, Ic and Id are selectively connected to the output terminal of the address selector 211, under control of the 2-bit counter 213a. Outputs Q0 and Q1 of the 2-bit counter 213a periodically change to logic states "00", "01", "10" and "11", as shown in Graph 2C of Fig. 2. These logic states "00", "01", "10" and "11" are associated for selecting the input terminals Ia, Ib, Ic and Id, respectively. Thus the display addresses DAa, DAb, DAc and DAd on the input terminals Ia, Ib, Ic and Id of the address selector 211 are sequentially and periodically provided to the first input terminal J1 of the access selector 220, while the control address CA from the CPU 100 is connected to the second input terminal J2 of the access selector 220, as described above.

The access selector 220 is controlled by the access control signal S1, as shown in Graph 2D of Fig. 2. The access control signal S1 is supplied from the display timing generator 212, as described above. The access control signal S1 periodically changes between the "0" logic state and the "1" logic state. Thus the display addreses DAa, DAb, DAc and DAd on the first input terminal J1 and the control address CA on the second input terminal J2 are periodically selected by the access control signal S1, i.e., by the "0" logic state and the "1" logic state, respectively. The "0" logic state has a long period corresponding to the duration of the display addresses DAa, DAb, DAc and DAd, while the "1" logic state has a short period corresponding to the CPU access period.

When the access control signal S1 from the display timing generator 212 is in the "1" logic state, the access selector 220 selects the second input terminal J2, so that the control address CA from the CPU 100 given to the RAM 230. Therefore, the RAM address combining the display addresses and the control address, as shown in Graph 2B of Fig. 2, is obtained.

The access control signal S1 is also given to the CPU timing generator 110. The CPU timing generator 110 outputs the data access signal S2 in the CPU access period. The data access signal S2 opens a gate of the data buffer 240 and allows the CPU 100 to access the image data stored in the RAM 230. In this connection, Graph 2E of Fig. 2 shows a clear signal CL applied to the 2-bit counter 213a from the display timing generator 212.

In the above decribed apparatus, the CPU access period is fixed in the unit display period. Thus, the conventional apparatus has a drawback in that the CPU 100 cannot freely access the RAM 230 in the unit display period.

The present invention therefore seeks to provide an image memory control apparatus in which a CPU can freely access an image memory.

An image memory control apparatus according to one aspect of the present invention includes a display address generator for generating addresses of the stored image data, a display address selector for selecting desired image data addresses sequentially in a fixed order during a unit display cyle, a control address generator, e.g., a CPU for generating addresses of the stored control data, an access selector for combining the image data addresses and the control data address and a controller for controlling the access selector, wherein the controller includes a circuit means for shifting the control of the access selector to immediately access the stored control data in response to an access requesting signal.

In such apparatus according to the present invention, the control data address is freely shifted in the unit display cycle in response to an access request signal. Thus, the control operation conducted by the CPU for the image memory control apparatus is improved.

For a better understanding of the present invention and many of the attendant advantages thereof, reference will now be made,by way of example, to the accompanying drawings, wherein:

Fig. 1 is a block diagram showing an image memory control apparatus know to the applicant.

Fig. 2 is a timing chart explaining the operation of the apparatus of Fig. 1;

Fig. 3 is a block diagram showing an embodiment of an image memory control apparatus according to the present invention;

Fig. 4 is a timing chart illustrating the operation of the image memory control apparatus of Fig. 3; and

Figs. 5A to 5E are timimg charts illustrating a shift operation of the CPU period in the image memory control apparatus of Fig. 3.

The present invention will be described in detail with reference to Fig. 3, Fig, 4 and Figs. 5A through 5E. Throughout the drawings, reference numerals or letters used in Figs. 1 and 2 will be used to designate like or equivalent elements for simplicity of explanation.

Referring now to Figure 3, an embodiment of the image memory control apparatus according to the present invention will be described in detail.

In Fig. 3, the image memory control apparatus according to the present invention comprises a CPU 100, a CPU timing generator 110 and an image memory controller 200. The image memory controller 200 comprises an address generator 210, a display timing generator 212, an address selector 211, an access selector 220, a RAM 230, a data buffer 240, a display driver 250 and a CPU period controller 214. The CPU period controller 214 includes a 2-bit counter 214a and a D type flip flop

214b.

Thus, the image memory control apparatus of Fig. 3 has almost the same elements as the conventional apparatus of Fig. 1. However, the image memory control apparatus of Fig. 3 is improved from the apparatus of Fig. 1 in that it includes the CPU period controller 214 instead of the address selector controller 213.

The improvement of the image memory control apparatus shown in Fig. 3 will be described in detail. In Fig. 3, to the access selector 220 is applied an access control signal S1 from the CPU timing generator 110. The access control signal S1 is also applied to the CPU period controller 214. That is, the access control signal S1 is input to both an enable terminal CKE of the 2-bit counter 214a and a clock terminal CK of the flip flop 214b. The display timing generator 212 supplies a clock signal S3 to a clock terminal CK of the 2-bit counter 214a. The display timing generator 212 also supplies a clear signal S4 to both a clear terminal CL of the 2-bit counter 214a and a preset terminal PR of the flip flop 214b. The flip flop 214b supplies a CPU enable signal S5 to an enable terminal CPU EN of the CPU timing generator 110. The CPU enable signal S5 is output from the output terminal Q of the flip flop 214b, while the data input terminal D of the flip flop 214b is coupled to a reference potential source, e.g., a ground circuit.

When an access request signal 140 is supplied to the CPU timing generator 110 from the CPU 100, the access control signal S1, as shown in Graph 4d In Fig. 4, is generated on a first output terminal K1 of the CPU timing generator 110. The access control signal S1 is used for selecting the display addresses DAa, DAb, DAc and DAd on the first input terminal J1 or the control address CA on the second input terminal J2. Further the access control signal S1 is supplied to the clock terminal CK of the flip flop 214b and the clock enable terminal CKE of the 2-bit counter 214a. The data access signal S2 is output from a second output terminal K2 of the CPU timing generator 110, and used to set the gate of the data buffer 240 open.

The 2-bit counter 214a carries out a count-up operation at the rise of the clock signal S3 generated from the display timing generator 212, as shown in Graph 4A of Fig. 4. The count of the 2-bit counter 214a is cleared to the logic state "00" by a clear signal CL, as shown in Graph 4E of Fig. 4. Then, the 2-bit counter 214a starts the counts, i.e., the logic states "00", "01", "10" and "11", in turn.

However, the 2-bit counter 214a receives the access control signal S1 at its clock enable terminal CKE. The count-up operation of the 2-bit counter 214a is interrupted when the access control signal S1 rises to the "1" logic state. The location of the "1" logic state of the access control signal S1 is freely and directly set in response to the access requesting signal 140 applied to the CPU timing generator 110 from the CPU 100 (while, the location of the "1" logic state at the conventional apparatus is fixed in the access control signal S1, see Graph 2D in Fig. 2). Thus, the count-up operation of the 2-bit counter 214a is interrupted immediately after the access request signal 140 has been applied to the CPU timing generator 110 from the CPU 100.

The flip flop 214b generates the CPU enable signal S5, as described above. The CPU enable signal S5 is applied to the enable terminal EN of the CPU timing generator 110. When the access request signal 140 is supplied from the CPU 100 during the time when the CPU enable signal S5 is also at the "1" logic state, the CPU timing generator 110 switches the access control signal S1 to the "1" logic state. Thus, the access control signal S1 at a "1" logic state causes the access selector 220 to select the control address CA on the second input terminal K2, as shown in Graph 4D of Fig. 4. At this time, the CPU timing generator 110 outputs the data access signal S2. The data access signal S2 sets the gate of the buffer 240 open, and makes the access to the control data stored in the RAM 230 possible.

The D type flip flop 214b is clocked by the trailing end of the "1" logic state of the access control signal S1. The D type flip flop 214b operates to transmit the input level on its data input terminal D to its output terminal Q, as usual. In the apparatus of Fig. 3, the data input terminal D is coupled to the ground circuit. Thus, the "0" logic state is basically introduced on the output terminal Q of the flip flop 214b when the access control signal S1 falls to the "0" logic state. However, the flip flop 214b is given the clear signal S4, as shown in Graph 4E, to its preset terminal PR from the display timing generator 212. This clear signal S4 of the "1" logic state presets the flip flop 214b so that the output terminal Q turns to the "1" logic state. Thus, the Q output of the flip flop 214b, i.e., the CPU enable signal S5, as shown in Graph 4F in Fig. 4, is formed by the access control signal S1 and the clear signal S4.

As a result, a RAM address, as shown in Graph 4B of Fig. 4, is output from the access selector 220. The RAM address includes the display addresses DAa, DAb, DAc and DAd and the control address CA for every unit display cycle. In the unit display cycle, the location of the control address CA is shifted in response to the access control signal S1, while the count-up operation of the 2-bit counter 214a is interrupted by the access control signal S1. Thus, the logic states of the outputs Q0 and Q1 of the 2-bit counter 214a are maintained for two clock periods, as shown in Graph 4C of Fig. 4, in response to the access control signal S1. Thus, the display address present at the input J1 of the access selector 220, at the instant the CPU period is introduced and connection of the output terminal of the access selector 220 is changed from the first input terminal J1 to the second input terminal J2, is maintained. Accordingly, the four display addresses DAa, DAb, DAc and the DAd are preserved in the correct order in every unit display cycle, in spite of the variation in timing of the CPU period.

In this connection, in the CPU timing generator 110, when there is an access request signal 140 from the CPU 100 , the access control signal S1 is switched to the "1" logic state only when, the CPU enable signal S5 is also in the "1" logic state. Therefore, the CPU access period will be limited to one occurrence in one unit display cycle.

Figs. 5A to 5E show various circumstances wherein the control address CA shifts in response to the access control signal S1, which results in the display addresses DAa, DAb, DAc and the DAd shifting in the unit display cycle. In each of Figs. 5A to 5E, the clock CK and clear signal CL to be output from the display timing generator 212 have been omitted.,

In the above embodiment, the image data display period in the unit display cycle is constituted by four image data periods, but in carrying out the present invention the constitution of this image data display period and CPU period may varied from that of the above described embodiment. Further, the manner of shifting the CPU period in the unit display cycle in correspondence with the access request from the CPU 100 should not be limited to the embodiment described above, in reference to Figs. 3, 4 and 5. In the above embodiment, though RAM 230 is provided for storing image data and control data, any other type of memory, e.g, a ROM (read only memory), can be used instead.

As described above, the present invention can provide an extremely advantageous image memory control apparatus.

While there have been illustrated and described what are at present considered to be preferred embodiments of the present invention, it will be understood by those skilled in the art that various changes and modifications may be made, and equivalents may be substituted for elements thereof without departing from the true scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teaching of the present invention without departing from the central scope thereof. Therefore, the present invention is not to be limited to the particular embodiment disclosed as the best mode contemplated for carrying out the present invention, but the present invention includes all embodiments falling within the scope of the claims.

The foregoing description and the drawings are regarded by the applicant as including a variety of individually inventive concepts, some of which may lie partially or wholly outside the scope of some or all of the following claims. The fact that the applicant has chosen at the time of filing of the present application to restrict the claimed scope of protection in accordance with the following claims is not to be taken as a disclaimer of alternative inventive concepts that are included in the contents of the application and which could be defined by claims differing in scope from the following claims, which different claims may be adopted subsequently during prosecution, for example for the purposes of a divisional application.

Claims

1. An image memory control apparatus containing memory means (230) for storing image data and control data, display address generating means (210) for generating addresses of the stored image data, display address selecting means (211) for selecting desired image data addresses sequentially in a fixed order and control address generating means (100) for generating addresses of the stored control data, access selector means (220) for selecting access of the image data addresses or the control data address, control means (212; 214/110) for controlling the access selector means (220) and means (100) for requesting the access to the stored control data, CHARACTERISED IN THAT
the control means (214/110) includes means for arranging the access selector means (220) immediately to access the stored control data in response to the access requesting means (100).

2. An image memory control apparatus of claim 1 wherein the control data address generated is inserted into the sequential and fixed order of accessed image data addresses selected by the display address selecting means (110) and the sequential accessing of the image data addresses suspended until the control data address has been accessed.

3. An image memory control apparatus of claim 1 wherein the control means (214) includes a flip flop circuit (214b) and a counter circuit (214a).

4. A method for controlling a memory apparatus storing image data and control data, including the steps of generating addresses for the image data stored in the memory, selecting the addresses of the image data in a sequentially fixed order, generating addresses for the control data stored in the memory, combining the image data addresses and the control data address,
CHARACTERIZED IN THAT

the control data address is immediately combined into the sequentially and fixed image data addresses upon receipt of an access request signal.

5. An image memory control apparatus containing memory means (230) for storing image data and control data, display address generating means (210) for generating addresses of the stored image data, display address selecting means (211) for selecting desired image data addresses sequentially in a fixed order and control address generating means (100) for generating addresses of the stored control data, combining means (220) for combining the image data addresses and the control data address, control means (214) for controlling the combining means (220) and means (110) for requesting the access to the stored control data,
CHARACTERISED IN THAT
the control means (214) includes means for shifting the control of the combining means (220) to immediately access the stored control data in response to the access requesting means (110).

6. An image memory control apparatus of claim 1 wherein the control data address generated is immediately inserted into the sequential and fixed order image data addresses selected by the display address selecting means (110).

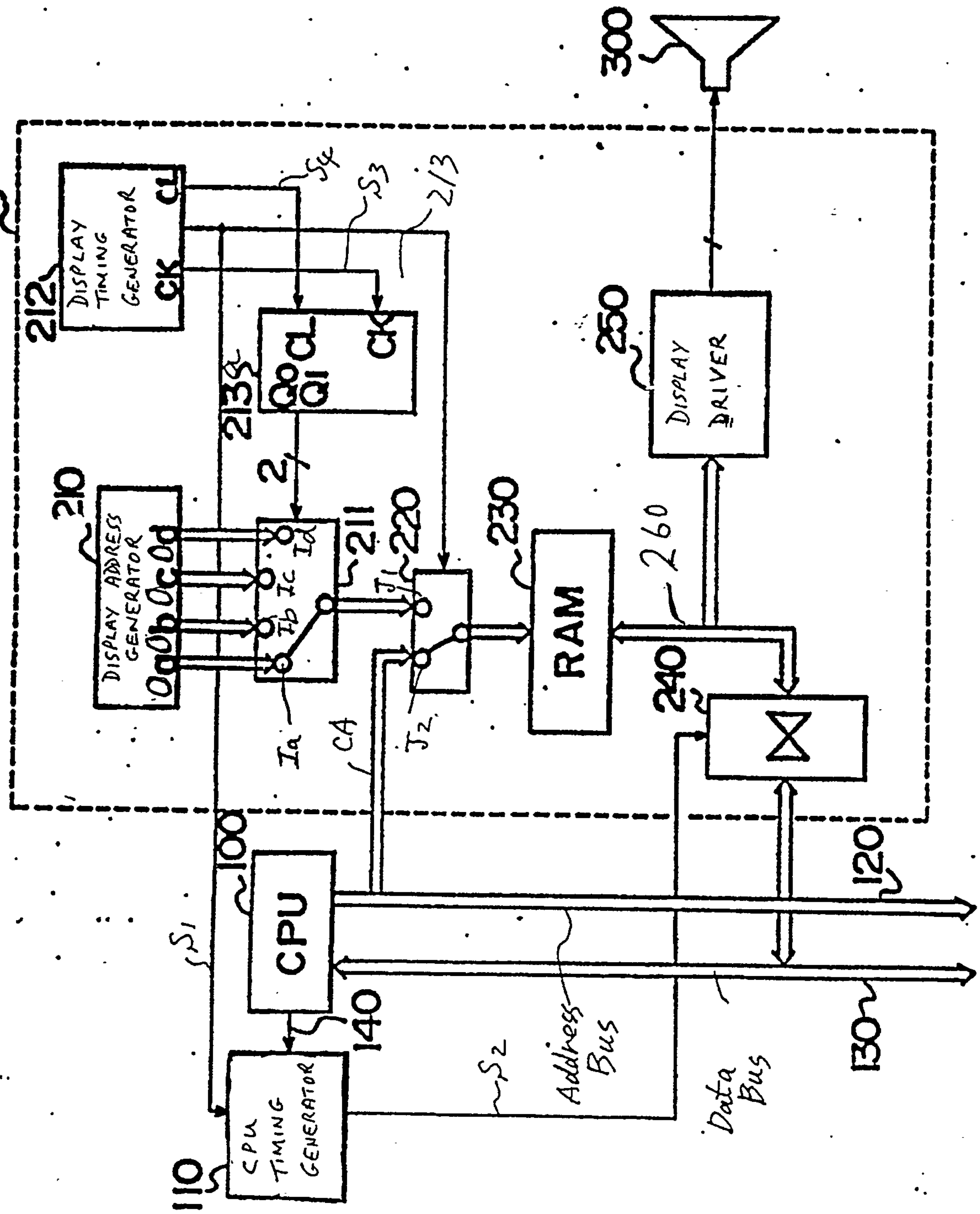
200
212
DISPLAY TIMING GENERATOR
CK
CL
S4
S3
213
Q0
Q1
CL
CK
2
210
DISPLAY ADDRESS GENERATOR
Oa Ob Oc Od
211
Ia Ib Ic Id
220
J1
J2
230
RAM
260
240
250
DISPLAY DRIVER
300
CA
100
CPU
140
110
CPU TIMING GENERATOR
S1
S2
Address Bus
Data Bus
120
130

Fig. 1

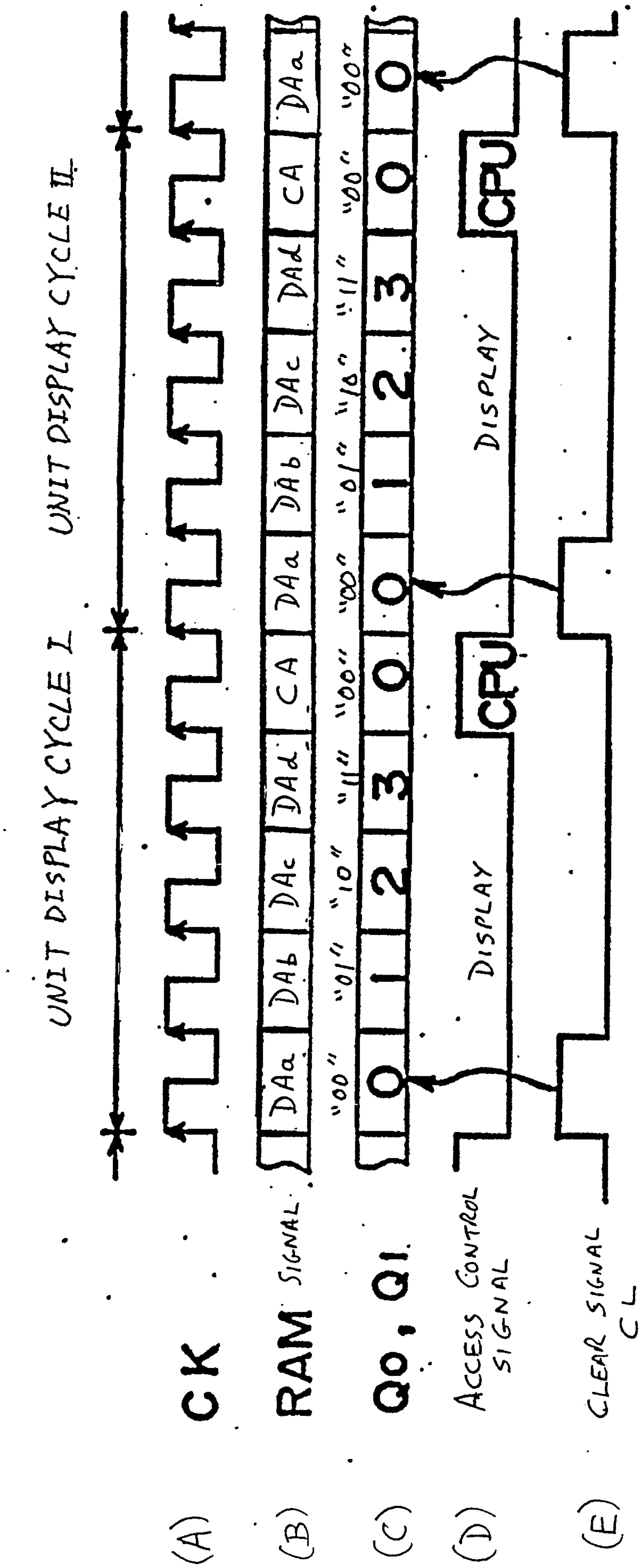
(A) CK
(B) RAM SIGNAL
(C) Q0, Q1
(D) ACCESS CONTROL SIGNAL
(E) CLEAR SIGNAL CL
UNIT DISPLAY CYCLE I
UNIT DISPLAY CYCLE II
DAa DAb DAc DAd CA DAa DAb DAc DAd CA DAa
"00" "01" "10" "11" "00" "00" "01" "10" "11" "00" "00"
0 1 2 3 0 0 1 2 3 0 0
DISPLAY
CPU
DISPLAY
CPU

Fig. 2

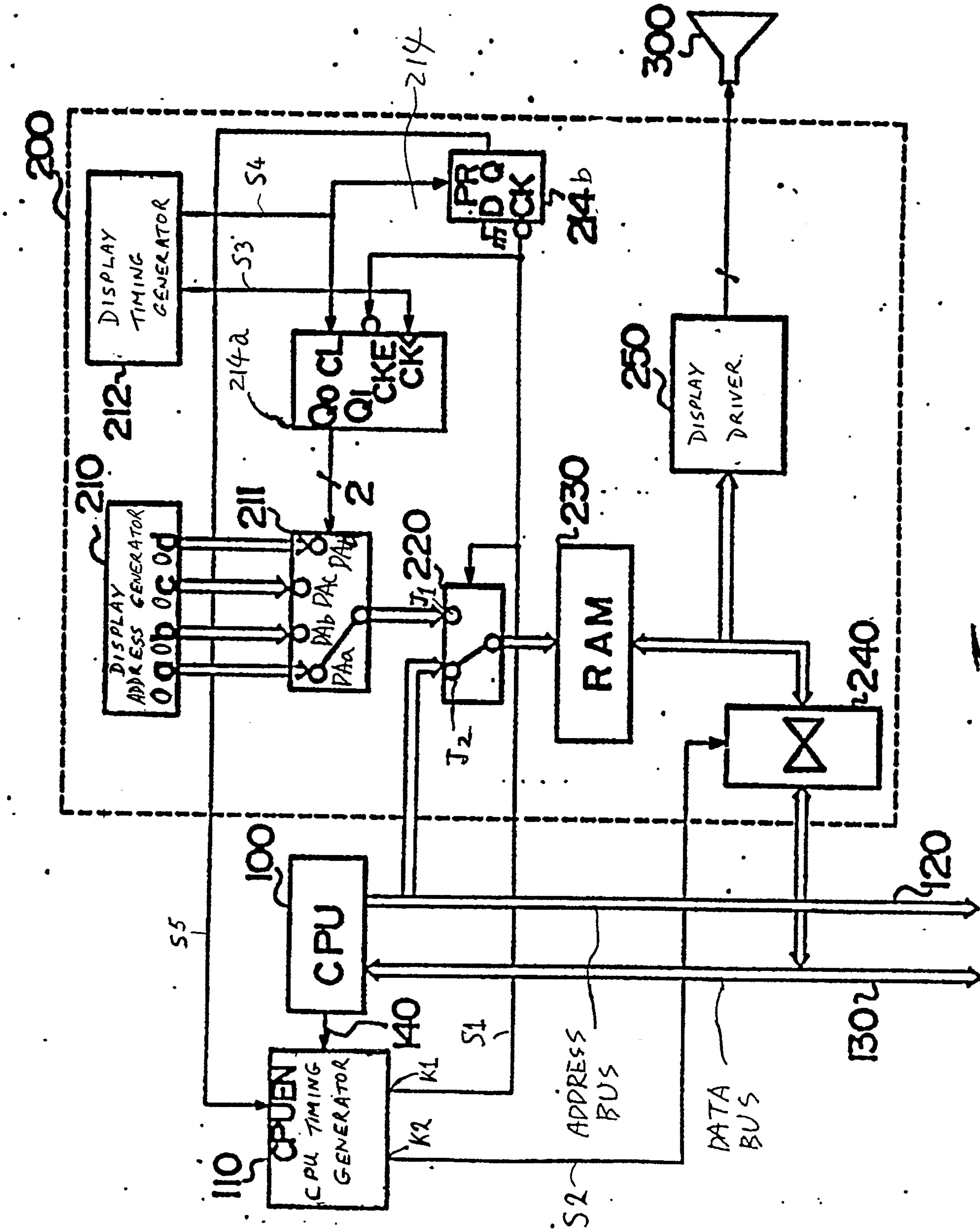
200
210
DISPLAY ADDRESS GENERATOR
0a 0b 0c 0d
211
DAa DAb DAc DAd
212
DISPLAY TIMING GENERATOR
S3
S4
214
214a
Q0 CL
Q1 CKE CK
2
214b
PR D Q
CK
220
J1
J2
230
RAM
240
250
DISPLAY DRIVER
300
100
CPU
110
CPUEN
CPU TIMING GENERATOR
140
K1
K2
S1
S2
S5
ADDRESS BUS
DATA BUS
120
130

Fig. 3

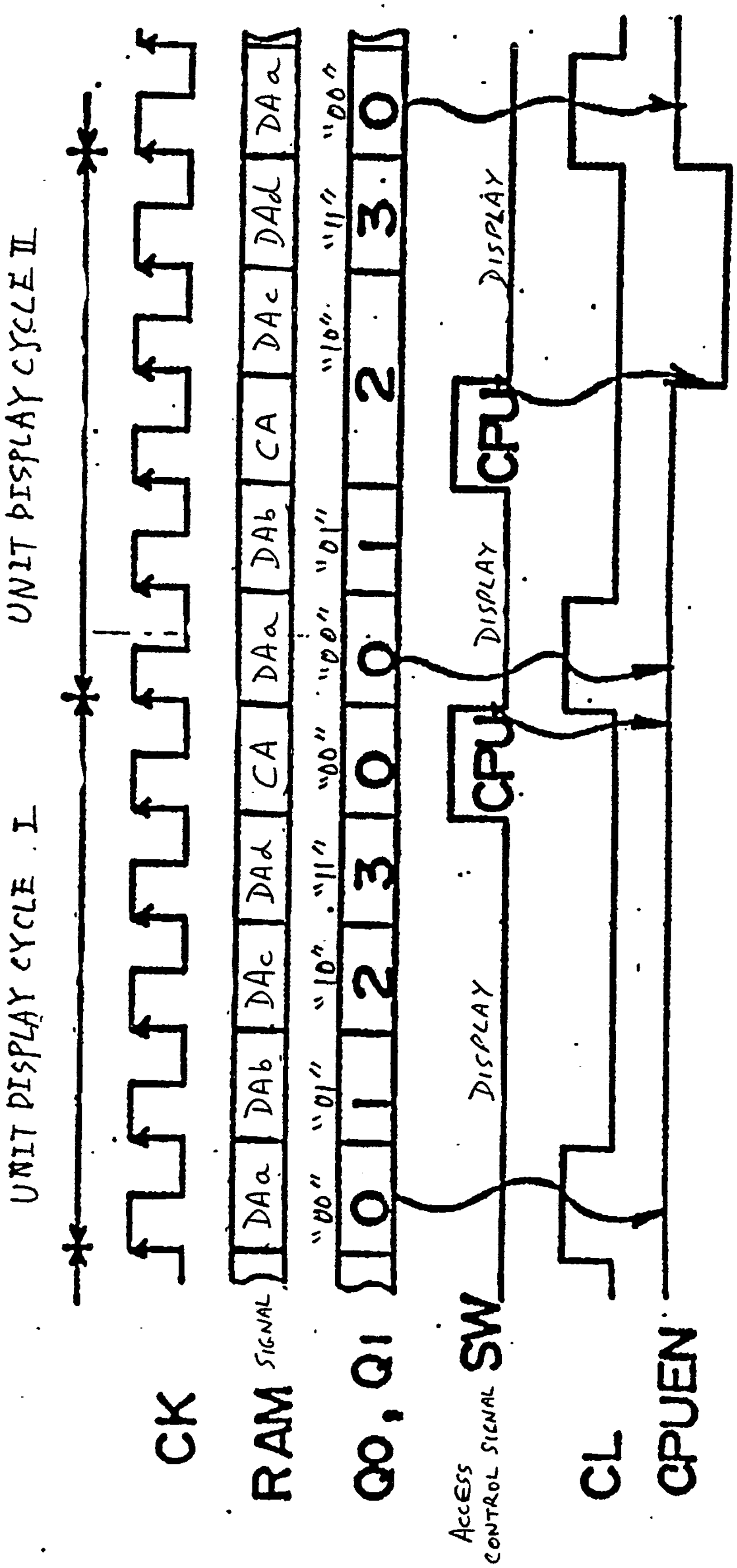
CK
RAM SIGNAL
Q0, Q1
ACCESS CONTROL SIGNAL SW
CL
CPUEN
UNIT DISPLAY CYCLE I
UNIT DISPLAY CYCLE II
DAa DAb DAc DAd CA DAa DAb CA DAc DAd DAa
"00" "01" "10" "11" "00" "00" "01" "10" "11" "00"
0 1 2 3 0 0 1 2 3 0
DISPLAY
CPU
DISPLAY
CPU
DISPLAY

Fig. 4

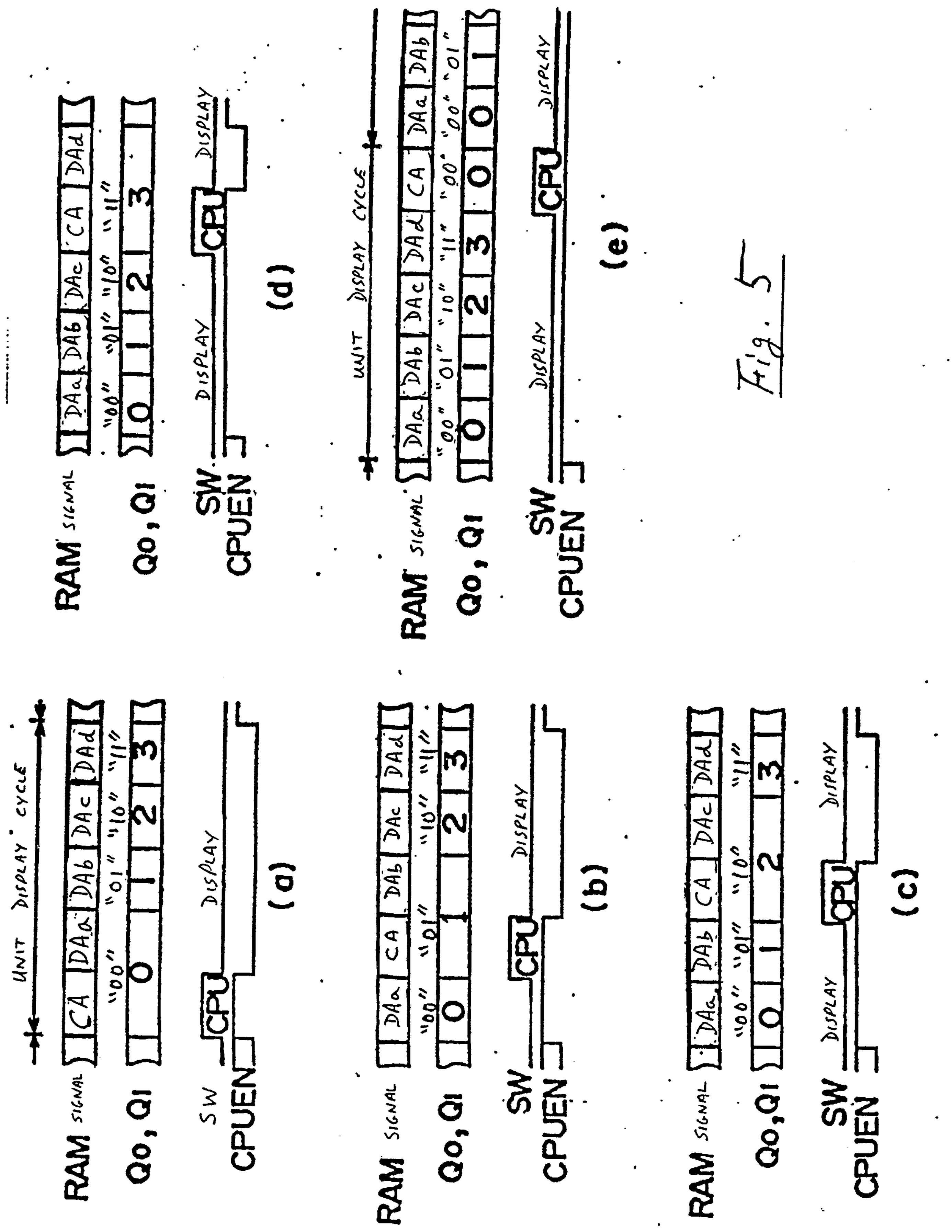
RAM SIGNAL
Qo, Q1
SW
CPUEN
UNIT DISPLAY CYCLE
CA
DAa
DAb
DAc
DAd
"00"
"01"
"10"
"11"
0
1
2
3
CPU
DISPLAY
(a)
(b)
(c)
(d)
(e)

Fig. 5