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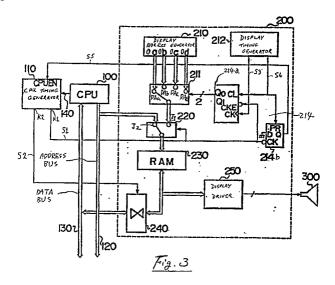
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- (54) Image memory control apparatus.
- The apparatus control apparatus containing a memory device (220) for storing image data and control data. The apparatus includes a display address generator (210) for generating addresses of the stored image data, a display address selector (211) for selecting desired image data addresses sequentially in a fixed order, a control address generator (100) for generating addresses of the stored

control data, an access selector (220) for combining the image data addresses and the control data address and a controller (214) for controlling the access selector (220), wherein the controller (214) includes a circuit (214) for shifting the control of the access selector (220) to immediately access the stored control data in response to an access requesting signal.





EUROPEAN SEARCH REPORT

EP 89 31 2312

DOCUMENTS CONSIDERED TO BE RELEVANT				
Category		h indication, where appropriate, vant passages	Rele to c	
Α	US-A-4 104 624 (H. NAGA * Figure 1; page 2, lines 22-	· · · · · · · · · · · · · · · · · · ·	1-6	G 09 G 1/16
Α	EP-A-0 254 293 (FUJITSU * Figure 3; claim 1 *	LTD)	1-6	
Α	IBM TECHNICAL DISCLOSI July 1985, pages 571-572, f function in a general-purpos * Whole document *	New York, US; "DMA cycle		
Т	US-A-4 845 661 (Y. SHIMA * Figure 2; page 3, lines 30-		1-6	
Т	US-A-4 802 118 (H. TOYO * Figure 7; page 3, lines 61-6 		1-6	
				TECHNICAL FIELDS SEARCHED (Int. C1.5)
				G 09 G
	The present search report has t	een drawn up for all claims		
	Place of search	Date of completion of sea	arch	Examiner
	The Hague	16 May 91		ZENDER J.J.
Y: A: O:	CATEGORY OF CITED DOCL particularly relevant if taken alone particularly relevant if combined wit document of the same catagory technological background non-written disclosure intermediate document	h another	the filing dat D: document cit L: document cit	t document, but published on, or after e ed in the application ed for other reasons he same patent family, corresponding