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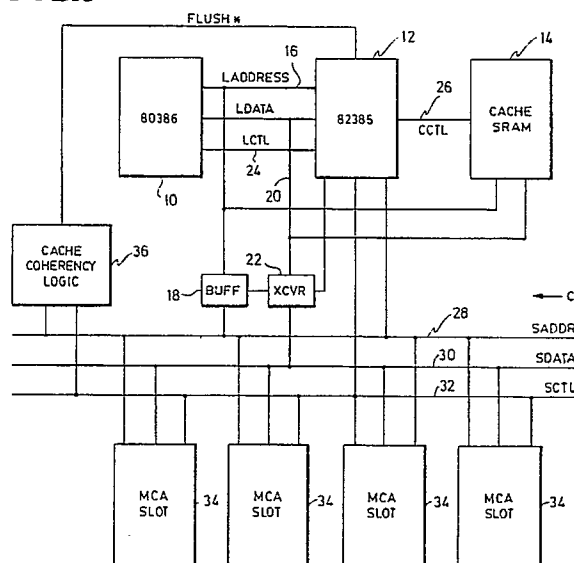
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(54) **Programmable option selection and paged memory cache coherency control.**

(57) A cache flush request circuit for a computer system which flushes (72) the cache controller when a circuit board is being configured (62,64,66, 68) or is responding (68,70) to an input/output write opera-

tion (50) is described. The flush operation can be disabled (56,58) for each circuit board location. A cache flush operation can also be directly requested (72,74,76,78,80).

FIG.1



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EUROPEAN SEARCH REPORT

Application Number

EP 89 31 3158

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	MICROPROCESSORS & MICROSYSTEMS, vol. 12, no. 3, April 1988, pages 147-152; G. LAWS: "Multiprocessing on the Nubus using cache inhibited pages" * Page 150, left-hand column, lines 25-36 * - - -	1	G 06 F 12/08
A	COMPUTER DESIGN, vol. 26, no. 14, August 1987, pages 89-94; W. VAN LOO: "Maximize performance by choosing best memory" * Page 93, right-hand column, lines 19-41; page 94, upper part * - - - - -	1	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			G 06 F 12
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of search 07 June 91	Examiner LEDRUT P.
<div>CATEGORY OF CITED DOCUMENTS</div> <div><div>X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention</div><div>E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons ----- &: member of the same patent family, corresponding document</div></div>			