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(54) I/O bus caching.

(57) A cache for use with input/output devices attached to an input/output bus. Requests for access to system memory by an input/output device pass through the cache. Virtual memory addresses used by the input/output devices are translated into real addresses in the system memory. Virtual memory can be partitioned, with some virtual addresses being mapped to a second memory attached to the input/output bus.

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EUROPEAN SEARCH REPORT

Application Number

EP 89 31 2897

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 052 370 (HITACHI ENGINEERING CO., LTD) * Page 1, lines 1-13; page 11, line 3 - page 12, line 23; claim 1 *	1,6,8	G 06 F 12/08
A		2,5	
A	ELECTRONIC DESIGN, vol. 30, no. 5, March 1982, pages 93-98, Waseca, MN, Denville, NJ, US; J. VANAKEN: "Match cache architecture to the computer system" * page 96, column 1, line 34 - column 2, line 44; figures 1,4-6 *	1,6-8	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 06 F 12/08

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	22 November 90	ADRIAENSSENS M.T.K.P

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

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