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(54) Method and apparatus for detecting and correcting errors in a pipelined computer system.

(57) In a multiprocessor system, an error occurring in any one of the CPUs may have an impact upon the operation of the remaining CPUs, and therefore these errors must be handled quickly. The errors are grouped into two categories: synchronous errors (those that must be corrected immediately to allow continued processing of the current instruction); and asynchronous errors (those errors that do not affect execution of the current instruction and may be handled upon completing execution of the current instruction). Since synchronous errors prevent continued execution of the current instruction, it is preferable that the last stable state conditions of the faulting CPU be restored and the faulting instruction reexecuted. These stable state conditions advantageously occur between the execution of each instruction. However, in a pipelined computer system, it is difficult to identify the beginning and ending of a selected instruction since multiple instructions are in process at the same time. Accordingly, the execution unit is selected to be the point of synchronization between error handling and instruction execution. Once the error is identified as asynchronous or synchronous and the execution unit allows the instruction to complete or rolls back the state conditions to their preinstruction values, error analyzing software examines the condition of the suspect data latches in the CPU. A serial diagnostic link stops the system clock of the CPU and serially loads the CPU data latches into the System Processor Unit for error determination. Thereafter, the CPU system clock is restarted and the CPU resumes execution.

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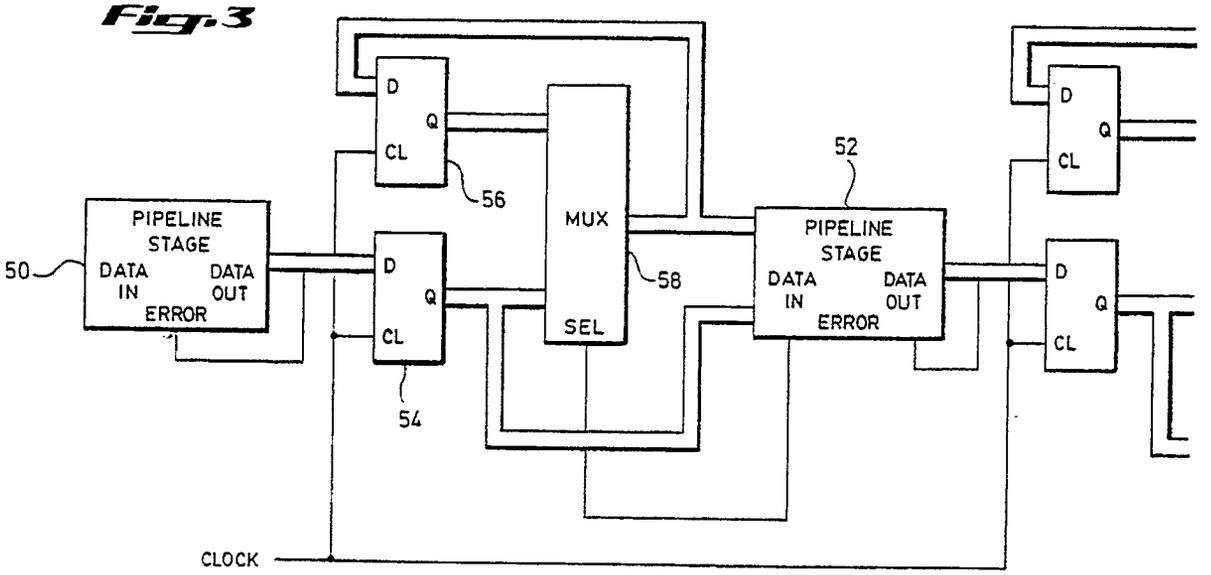
Fig.3


PIPELINE
STAGE
DATA IN
DATA OUT
ERROR
50
D
Q
CL
56
54
MUX
SEL
58
52
PIPELINE
STAGE
DATA IN
DATA OUT
ERROR
CLOCK

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EUROPEAN SEARCH REPORT

Application Number

EP 89 30 9651

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. SC-22, no. 5, October 1987, pages 808-819; P.W. BOSSHART et al.: "A 553K-transistor LISP processor chip" * Page 814, column 1, line 5 - column 2, line 36; page 816, column 2, lines 13-15 *	1,7	G 06 F 11/00 G 06 F 11/14
A	IDEM	4-6,10-13	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 28, no. 2, July 1985, pages 621-624, New York, US; "Error tracing arrangement of a pipelined processor"	1-3,7-9	
Y	EP-A-0 113 232 (FUJITSU LTD) * Abstract *	1,7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
G 06 F

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	22 May 91	CORREMANS G.J.W.

CATEGORY OF CITED DOCUMENTS

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