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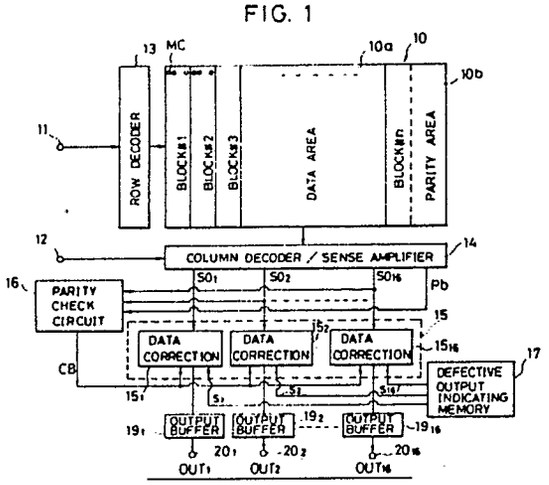
(54) Semiconductor memory device having mask rom structure.

(57) A semiconductor memory device includes a memory cell array (10) having a plurality of memory cells (MC) and formed by a mask ROM, the memory cell array having a data area (10a) in which data (SO_1 -SO_{16}) of n bits (n is an arbitrary number) is stored and a parity area (10b) in which a one-bit parity code (Pb) relating to the data is stored. A control circuit (13, 14) supplies the memory cell array with an address and reads out the data and the one-bit parity code designated by the address. A parity check circuit (16) determines whether or not the data read out from the memory cell array has a bit error and generates correction data (CB) indicating a determination result. A memory (17) stores defective output indicating data (S_1 - S_{16}) indicating one of the n bits of the data having the bit error. A data correction circuit (15) corrects one of the n bits of the data indicated by the defective output indicating data by the correction bit.

FIG. 1



SEMICONDUCTOR MEMORY DEVICE HAVING MASK ROM STRUCTURE

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device having a mask ROM structure, and more particularly to a semiconductor memory device having an error correcting function.

A semiconductor memory device having a mask ROM structure is known. A memory cell array including a plurality of memory cells is configured by mask ROM elements. Information is written into the memory cell array during manufacturing the memory device. Once information is written into the memory cell array, it is impossible to revise the written information. Actually, a memory device has some defective memory cells. Thus, a programmable ROM is incorporated in the memory device. After fabricating the memory device, it is subjected to a test for locating defective memory cells. The address of each detected defective memory cell is written into the programmable ROM. That is, the defective memory cells are replaced by memory cells of the programmable ROM. When the address of a defective memory cell is designated, the corresponding memory cell of the programmable ROM is accessed and information stored therein is read out from the programmable ROM.

However, memory cells of the programmable ROM are larger than those of the mask ROM. For this reason, a large area on a chip must be provided for the programmable ROM. This decreases the integration density of the memory device. Further, it takes an extremely long time to write address information and data on defective memory cells into the programmable ROM.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved semiconductor memory device having a mask ROM structure in which the aforementioned disadvantages are got rid of.

A more specific object of the present invention is to provide a semiconductor memory device having a mask ROM structure in which a reduced area of the programmable ROM on the chip is provided and it takes a reduced time to write information indicating the positions and data of defective memory cells into the programmable ROM.

The above objects of the present invention are achieved by a semiconductor memory device comprising a memory cell array having a plurality of memory cells and formed by a mask ROM, the memory cell array having a data area in which data of n bits (n is an arbitrary number) is stored and a parity area in which a one-bit parity code relating to the data is stored; control means, coupled to the memory cell array, for supplying the memory cell array with an address and reading out the data and the one-bit parity code designated by the address; parity check means, coupled to the memory cell array, for determining whether or not the data read out from the memory cell array has a bit error and for generating correction data indicating a determination result; memory means for storing defective output indicating data indicating one of the n bits of the data having the bit error; and data correcting means, coupled to the memory cell array, the parity check means and the memory means, for correcting one of the n bits of the data indicated by the defective output indicating data by the correction bit.

The above-mentioned objects of the present invention are achieved by a semiconductor memory device comprising a memory cell array having a plurality of memory cells and formed by a mask ROM, the memory cell array having a data area in which data of n bits (n is an arbitrary number) is stored and a parity area in which a one-bit parity code relating to the data is stored, the data area being divided into blocks each divided into m sub-blocks (m is an arbitrary number); control means, coupled to the memory cell array, for supplying the memory cell array with an address including information indicating one of the m sub-blocks and reading out the data and the one-bit parity code designated by the address; parity check means, coupled to the memory cell array, for determining whether or not the data read out from the memory cell array has a bit error and for generating correction data indicating a determination result; memory means for storing defective output indicating data indicating one of the m sub-blocks of each of the blocks relating to the bit error; and data correcting means, coupled to the memory cell array, the parity check means and the memory means, for correcting, by the correction bit supplied from the parity check means, one of the n bits of the data relating to the one of the m sub-blocks indicated by the defective output indicating data supplied from the memory means.

Further objects, features and advantages of the present invention will become apparent from the following detailed description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1 is a block diagram of a semiconductor memory device according to a first preferred embodiment of the present invention;

FIG.2 is a circuit diagram of a parity check circuit shown in FIG.1;

FIG.3 is a circuit diagram of a defective output indicating memory shown in FIG.1;

FIG.4 is a circuit diagram of each data correction circuit shown in FIG.1;

FIG.5 is a block diagram of a second preferred embodiment of the present invention;

FIG.6 is a diagram illustrating one block which is divided into four sub-blocks;

FIG.7 is a circuit diagram of a defective output indicating memory shown in FIG.5;

FIG.8 is a circuit diagram of an address decoder shown in FIG.7;

FIG.9 is a circuit diagram of a decoder provided in each logic circuit shown in FIG.7; and

FIG.10 is a circuit diagram of an alternative configuration of the defective output indicating memory shown in FIG.3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG.1, a semiconductor memory device includes a memory cell array 10 formed by a mask ROM. The memory cell array 10 is divided into a data area 10a and a parity area 10b. In the data area 10a, each row is divided into n blocks (n is an arbitrary number). For example, each row is divided into 16 blocks. Each block stores data composed of a predetermined number of bits, for example, 16 bits. In this case, each block has 16 memory cells MC. The parity area 10b stores, for each row, an even (or odd) number parity bit provided for each data of n bits, each of which relates to the respective block. Thus, n even (or odd) number parity bits are stored in the parity area 10b for each row. In the following description, each row of the data array 10a is divided into 16 blocks, each of which stores 16 bits for each row.

A row address is input to a row decoder 13 through a terminal 11, and a column address is input to a column decoder/sense amplifier 14 through a terminal 14. The row decoder 13 decodes the row address and selects one of a plurality of word lines (rows). When a decoded row address is supplied to the memory cell array 10, data and the parity bits relating to the designated row are read out therefrom and supplied to the column decoder/sense amplifier 14. The column decoder/sense amplifier 14 decodes the column address and selects data of 16 bits and a corresponding one-bit parity code relating to a decoded column address among from the data and one-bit parity codes read out from the memory cell array 10. The 16 data bits selected by the column decoder/sense amplifier 14 are supplied to a data correction block 15 and a parity check circuit 16. At the same time, the one-bit parity code relating to the selected data equal to 16 bits is supplied to the parity check circuit 16. The data correction block 15 is made up of 16 data correction circuits 15_1, 15_2, ..., 15_{16}.

FIG.2 is a circuit diagram of the parity check circuit 16. As is shown, the parity check circuit 16 is made up of a parity generator 16a and an exclusive-OR gate (XOR gate) 16b. The parity generator 16a receives the selected 16-bit data labeled SO_1 , SO_2, ..., SO_{16} and derives a one-bit parity output Pa. The XOR gate 16b receives the one-bit parity output Pa and the one-bit parity code labeled Pb supplied from the parity area 10b through the column decoder/sense amplifier 14, and generates a correction bit CB. When a parity error is detected, the correction bit CB is '1'. On the other hand, when no parity error is detected, the correction bit CB is '0' The correction bit CB is supplied to the data correction circuits 15_1 15_{16}.

A defective output indicating memory 17 formed by a programmable ROM such as a fuse ROM stores address information for each 16-bit data. Address information indicates which one of the 16 bits forming a 16-bit data is defective if the 16-bit data has a one-bit error. The memory device is tested after it is manufactured. In test, it is determined whether each memory cell of the data area 10a generates a bit error.

FIG.3 is a circuit diagram of the defective output indicating memory 17. As is illustrated, the defective output indicating memory 17 has 16 transistors Tr_1, Tr_2, Tr_3, ..., Tr_{16} and 16 fuses F_1, F_2, F_3, ..., F_{16} for each 16-bit data. Select data S_1, S_2, S_3, ..., S_{16} are drawn from the nodes of the transistors Tr_1 , Tr_2, Tr_3, ..., Tr_{16} and the fuses F_1, F_2, F_3, ..., F_{16}, respectively. When it is determined that one-bit data (memory cell) corresponding to the fuse F_3 for example, generates a bit error, the fuse F_3 is broken, and the other fuses relating to data bits having no error are held as they are. In this case, the select data S_3 is switched to a high level (Vcc; a positive power source voltage), and the other select data are maintained at a low level (ground level). The select data S_1- S_{16} are supplied to the data correction circuits 15_1- 15_{16}, respectively.

FIG.4 is a circuit diagram of the data correction circuit 15_1. Each of the data correction circuits 15_2 - 15_{16} has the same structure as the data correction circuit 15_1. The correction bit CB from the parity check circuit 16 is supplied to an XOR gate 31 through a terminal 30. The data bit SO_1 from the column

decoder sense amplifier 14 is supplied to the XOR gate 31 and a transmission gate 33 through a terminal 32. The XOR gate 31 inverts the data bit when the correction bit CB is '1', and passes the data bit SO_1 as it is when the correction bit CB is '0'. The output from the XOR gate 31 is supplied to a transmission gate 34. Each of the transmission gates 33 and 34 is supplied with the select data S_1 through a terminal 35 and inverted data thereof formed through an inverter 36. When the select data S_1 is '0', the transmission gate 33 conducts. On the other hand, when the select data S_1 is '1', the transmission gate 34 conducts. The output from each of the transmission gates 33 and 34 passes through a terminal 37 and is applied, as an output OUT_1, to an output buffer 19_1 (FIG.1).

Table 1 represents the operation of the data correction circuit 15_1. Each of the other data correction circuits 15_2 - 15_{16} operates in the same way as the data correction circuit 15_1.

Table 1

S_1	CB	SO_1	OUT_1
0	-	1	1
0	-	0	0
1	0	1	1
1	0	0	0
1	1	1	0
1	1	0	1

By the above-mentioned manner, one of the 16 data bits relating to a defective memory cell in the data area 10a (FIG.1) is corrected by a corresponding one of the data correction circuits 15_1 - 15_{16}. The outputs from the data correction circuits 15_1 - 15_{16} are amplified by the output buffers 19_1 - 19_{16} and then output through terminals 20_1 - 20_{16}, respectively.

A description is given of a second embodiment of the present invention with reference to FIG.5, in which those parts which are the same as those shown in FIG.1 are given the same reference numerals. As is shown in FIG.6, each block #1, #2, ..., #16 is divided into m blocks (m is an arbitrary integer), four sub-blocks in the illustrated case. One of the four sub-blocks is designated by two high-order bits of the column address applied to the terminal 12. The defective output indicating memory 17 shown in FIG.1 is replaced by a defective output indicating memory 40 having a terminal 18.

FIG.7 is a circuit diagram of the defective output indicating memory 40. As is shown, the detective output indicating memory 40 is made up of a logic circuit 47, a programmable ROM 48 such as a fuse ROM, and an address decoder 49. The aforementioned two high-order bits of the column address labeled A1 and A2 are applied to the address decoder 49, which outputs a decoded signal consisting of four bits. The fuse ROM 48 is divided into 16 circuits 48_1, 48_2, ..., 48_{16}. The logic circuit 47 is divided into 16 sections 47_1, 47_2, ..., 47_{16}. The circuits 48_1, 48_2, ..., 48_{16} of the fuse ROM 48 are provided for the sections 47_1, 47_2, ..., 47_{16} of the logic circuit 47, respectively. The circuit 48_1 generates a control signal C_1 and a pair of sub-block designation signals S_{11} and S_{12}. The control signal C_1 indicates whether or not the corresponding output from the data area 10a of the memory cell array 10 through the column decoder/sense amplifier 14 (FIG.6) should be corrected. The pair of sub-block designation signals S_{11} and S_{12} indicates one of the four sub-blocks which has a defective memory cell to be corrected. Each of the other circuits 48_2 -48_{16} generates a control signal such as C_2 and a pair of sub-block designation signals such as S_{21} and S_{22} in the same way as the circuit 48_1.

The control signal C_1 and the pair of sub-block designation signals S_{11} and S_{12} are supplied to a decoder 50 of the section 47_1 of the logic circuit 47. The section 47_1 decodes the input signals and generates four decoded signals. The section 47_1 of the logic circuit 47 includes NOR gates 51a, 51b, 51c and 51d, and an OR gate 52. The four decoded signals derived from the decoder 50 are supplied to the respective NOR gates 51a, 51b, 51c and 51d, which are also supplied with the respective signals supplied from the address decoder 49. Four outputs from the NOR gates 51a, 51b, 51c and 51d are input to the OR gate 52, which outputs a one-bit select signal X_1. Each of the sections 47_2 - 47_{16} is configured in the same way as the section 47_1, and outputs a corresponding one-bit select signal. The select signals X_1, X_2, ..., X_{16} are supplied to the data correction circuits 15_1, 15_2, ..., 15_{16}.

The relationship between the signals C_1, S_{11} and S_{12} and one of the sub-blocks to be corrected is shown in Table 2.

Table 2

C_1	S_{12}	S_{11}	Parity correction
L	L	L	first sub-block
L	L	H	second sub-block
L	H	L	third sub-block
L	H	H	fourth sub-block
H	X	X	no correction

FIG.8 is a circuit diagram of the address decoder 49 shown in FIG.7. The address decoder 49 is composed of two inverters 49a and 49b, and four NAND gates 49c, 49d, 49e and 49f. Two inputs A and B are decoded and four outputs X0, X1, X2 and X3 are generated.

FIG.9 is a circuit diagram of each decoder 50 shown in FIG.7. The decoder 50 is composed of three inverters 50a, 50b and 50C, and four NAND gates 50d, 50e, 50f and 50g. Three inputs G, A and B corresponding to the aforementioned control signal such as C_1 and sub-block designation signals such as S_{11} and S_{12} are decoded and four outputs X0, X1, X2 and X3 are generated. The fuse ROM 48 is configured by transistors and fuses in the same manner as the aforementioned arrangement shown in FIG.3.

Turning to FIG.7, when the two high-order bits A1 and A2 of the column address indicates the first block and the decoder of the section 47_1 of the logic circuit 47 indicates that the first block is to be corrected, for example, the OR gate 52 outputs the select signal X_1 maintained at the high level ('1'). It is noted that two bits in the same sub-block are defective, it is impossible to correct those bits.

According to the present invention, it is possible to correct one-bit data only by storing one-bit address information on a defective memory cell in the programmable ROM. Thus, a large-capacity programmable ROM is unnecessary. As a result, it is possible to suppress an increase of the chip area and reduce the time it takes to write address information into the programmable ROM.

An alternative cofiguration of the defective output indicating memory 17 shown in FIG.3 is illustrated in FIG.10. The alternative configuration includes four transistors Tr_1 - Tr_4, four associated fuses F_1 - F_4 and a decoder circuit 50. The select signals S_1' - S_4' are supplied to the decoder circuit 50, which decodes the select signals S_1' - S_4' and derives the 16 select signals S_1 -S_{16} therefrom.

The present invention is not limited to the aforementioned embodiments, and variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A semiconductor memory device characterized by comprising:

a memory cell array (10) having a plurality of memory cells (MC) and formed by a mask ROM, said memory cell array having a data area (10a) in which data (SO_1 - SO_{16}) of n bits (n is an arbitrary number) is stored and a parity area (10b) in which a one-bit parity code (Pb) relating to said data is stored;

control means (13, 14), coupled to said memory cell array, for supplying said memory cell array with an address and reading out said data and said one-bit parity code designated by said address;

parity check means (16), coupled to said memory cell array, for determining whether or not said data read out from said memory cell array has a bit error and for generating correction data (CB) indicating a determination result;

memory means (17) for storing defective output indicating data (S_1 - S_{16}) indicating one of the n bits of said data having said bit error; and

data correcting means (15), coupled to said memory cell array, said parity check means and said memory means, for correcting one of the n bits of said data indicated by said defective output indicating data by said correction bit.

2. A semiconductor memory device as claimed in claim 1, characterized in that said data correcting means (15) comprises a correction circuit (15_1 -15_{16}) provided for each of the n bits of said data, and in that said correction circuit includes:

an exclusive-OR gate (31) having a first input terminal supplied with said correction data, a second input terminal supplied with a corresponding one of the n bits of said data, and an output terminal through which an output signal of said exclusive-OR gate is drawn; and

selecting means (33, 34, 35) for selecting one of said output signal from said exclusive-OR gate and said corresponding one of the n bits of said data in accordance with said defective output indicating data from said memory means.

3. A semiconductor memory device as claimed in claim 2, characterized in that said defective output indicating data has n bits provided for the respective n bits of said data, and a corresponding one of the n bits of said defective output indicating data is supplied to said selecting means.

4. A semiconductor memory device as claimed in any of claims 1 to 3, characterized in that said memory means (17) comprises n programmable memory elements (Tr_1 - Tr_{16}, F_1 - F_{16}) which are provided for said data of n bits and store said defective output indicating data relating to the respective n bits of said data.

5. A semiconductor memory device as claimed in claim 4, characterized in that each of said programmable memory elements (Tr_1 Tr_{16}, F_1 -F_{16}) comprises a fuses ROM element.

6. A semiconductor memory device as claimed in any of claims 1 to 5, characterized in that said data area of said memory cell array (10) is divided into n blocks and said data of n bits is formed by one-bit data read out from each of said n blocks.

7. A semiconductor memory device as claimed in any of claims 1 to 6, characterized in that said parity check means (16) comprises:

a parity generator (16a) which receives said data of n bits and generates output parity data (Pa); and

an exclusive-OR gate (16b) having a first input terminal supplied with said output parity code (Pa), a second input terminal supplied with said one-bit parity code (Pb) read out from said memory cell array, and an output terminal through which said correction data (CB) is output to said data correcting means.

8. A semiconductor memory device as claimed in any of claims 1 to 7, said memory means (17) comprises:

a predetermined number of programmable memory elements (Tr_1 - Tr_4, F_1 - F_4) less than the number n and storing information relating to said defective output indicating data; and

decoder means (50), coupled to said programmable memory elements, for decoding said information stored in said programmable memory elements and for generating said defective output indicating data of n bits.

9. A semiconductor memory device as claimed in any of claims 3 to 8, characterized in that said selecting means (33, 34, 35) selects said output signal from said exclusive-OR gate (31) when said corresponding one of the n bits of said defective output indicating data indicates said bit error.

10. A semiconductor memory device as claimed in any of claims 1 to 9, characterized in that said one-bit parity code stored in the parity area (10a) of said memory cell array (10) is an even or odd number parity bit for said data of n bits.

11. A semiconductor memory device characterized by comprising:

a memory cell array (10) having a plurality of memory cells (MC) and formed by a mask ROM, said memory cell array having a data area (10a) in which data (SO_1 - SO_{16}) of n bits (n is an arbitrary number) is stored and a parity area (10b) in which a one-bit parity code (Pb) relating to said data is stored, said data area being divided into blocks each divided into m sub-blocks (m is an arbitrary number);

control means (13, 14), coupled to said memory cell array, for supplying said memory cell array with an address including address information (A1, A2) indicating one of said m sub-blocks and reading out said data and said one-bit parity data designated by said address;

parity check means (16), coupled to said memory cell array, for determining whether or not said data read out from said memory cell array has a bit error and for generating correction data indicating a determination result;

memory means (40) for storing defective output indicating data (X1 - X16) indicating one of said m sub-blocks of each of said blocks relating to said bit error; and

data correcting means (15), coupled to said memory cell array, said parity check means and said memory means, for correcting, by said correction bit supplied from said parity check means, one of the n bits of said data relating to said one of the m sub-blocks indicated by said defective output indicating data supplied from said memory means.

12. A semiconductor memory device as claimed in claim 11, characterized in that said memory means (40) comprises:

programmable memory means (48, 48_1 -48_{16}), provided for each of said n bits of said data, for storing first information (C_1) indicating whether or not a corresponding one of the n bits of said data should be corrected and second information (S_{11}, S_{12}) designating one of said m sub-blocks relating to a corresponding one of said blocks;

address decoder means (49) for deriving a decoded sub-block address indicating one of said m sub-blocks from said address; and

logic means (47), coupled to said programmable memory means and said address decoder means, for deriving said defective output indicating data (X1 - X16) indicating one of said m sub-blocks of each of said blocks relating to said bit error from said first and second information and said decoded sub-block address.

13. A semiconductor memory device as claimed in claim 12, characterized in that said logic means (47_1 - 47_{16}) provided in said memory means comprises:

decoder means for decoding said first and second information (C_1, S_{11}, S_{12}) supplied from said programmable memory means and generating a decoded output; and

gate means (51a - 51d, 52), coupled to said decoder means, for deriving said defective output indicating data (Pb) from said decoded sub-block address supplied from said address decoder means (49) and said decoded output from said decoder means of said logic means (47_1 - 47_{16}).

14. A semiconductor memory device as claimed in any of claims 11 to 13, characterized in that said data correcting means (15) comprises a correction circuit (15_1 - 15_{16}) provided for each of the n bits of said data (SO_1- SO_{16}), and in that said correction circuit includes:

an exclusive-OR gate (31) having a first input terminal supplied with said correction data, a second input terminal supplied with a corresponding one of the n bits of said data, and an output terminal through which an output signal of said exclusive-OR gate is drawn; and

selecting means (33, 34, 35) for selecting one of said output signal from said exclusive-OR gate and said corresponding one of the n bits of said data in accordance with said defective output indicating data (X1 - X16) from said memory means (40).

15. A semiconductor memory device as claimed in claim 14, characterized in that said defective output indicating data (X1 - X16) has n bits provided for the respective n bits of said data (SO_1 -SO_{16}), and a corresponding one of the n bits of said defective output indicating data is supplied to said selecting means (33, 34, 35).

16. A semiconductor memory device as claimed in any of claims 11 to 15, characterized in that said parity check means (16) comprises:

a parity generator (16a) which receives said data of n bits and generates output parity data (Pa); and

an exclusive-OR gate (16b) having a first input terminal supplied with said output parity data, a second input terminal supplied with said one-bit parity code (Pb) read out from said memory cell array (10), and an output terminal through which said correction data (CB) is output to said data correcting means.

17. A semiconductor memory device as claimed in any of claims 11 to 16, characterized in that said programmable memory means (48) includes fuse ROM elements.

FIG. 1

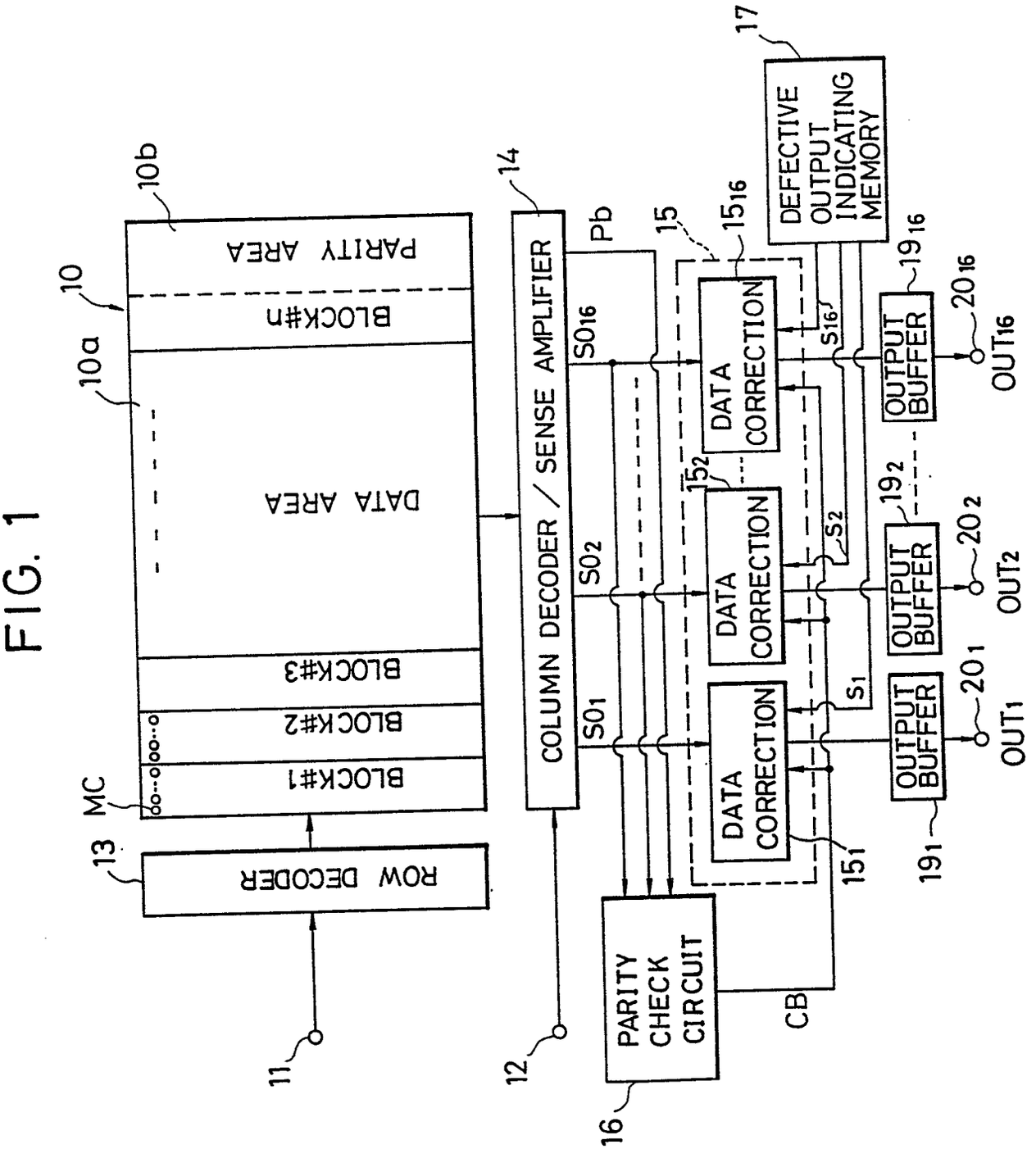

10
10a
10b
DATA AREA
BLOCK#1
BLOCK#2
BLOCK#3
BLOCK#n
PARITY AREA
MC
13
ROW DECODER
11
12
14
COLUMN DECODER / SENSE AMPLIFIER
Pb
SO1
SO2
SO16
15
151
152
1516
DATA CORRECTION
DATA CORRECTION
DATA CORRECTION
S1
S2
S16
16
PARITY CHECK CIRCUIT
CB
17
DEFECTIVE OUTPUT INDICATING MEMORY
191
192
1916
OUTPUT BUFFER
OUTPUT BUFFER
OUTPUT BUFFER
201
202
2016
OUT1
OUT2
OUT16

FIG. 2

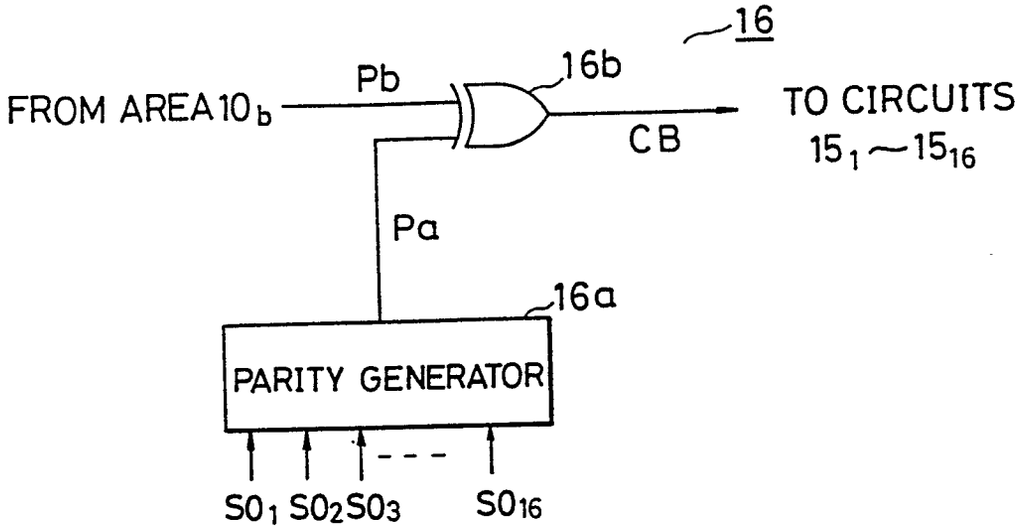


FIG. 3

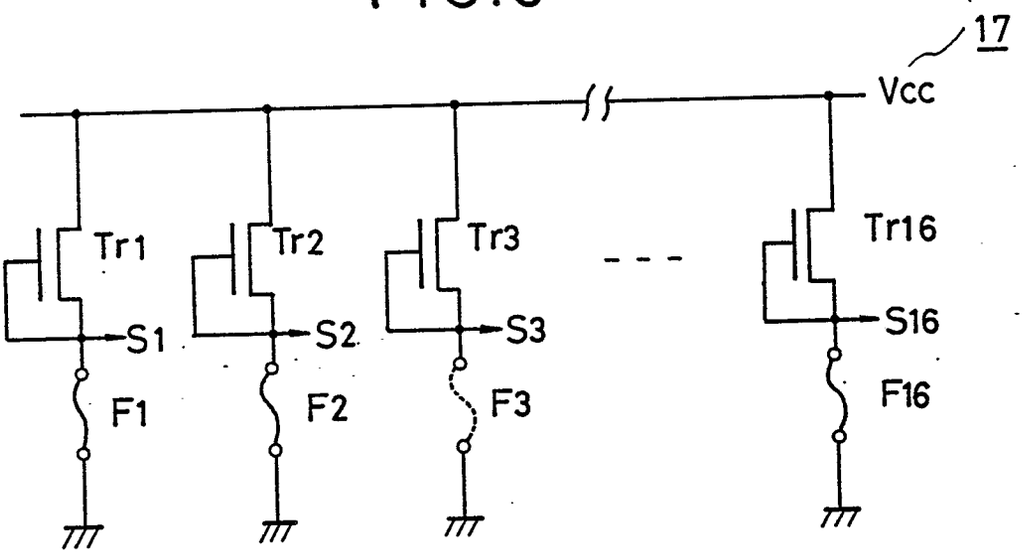


FIG. 4

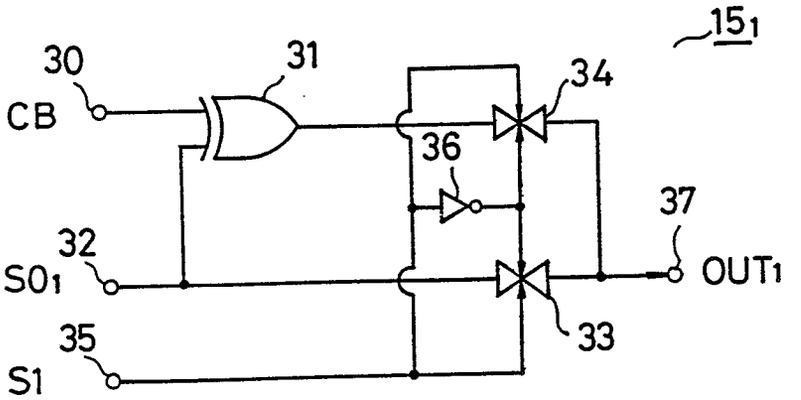


FIG. 5

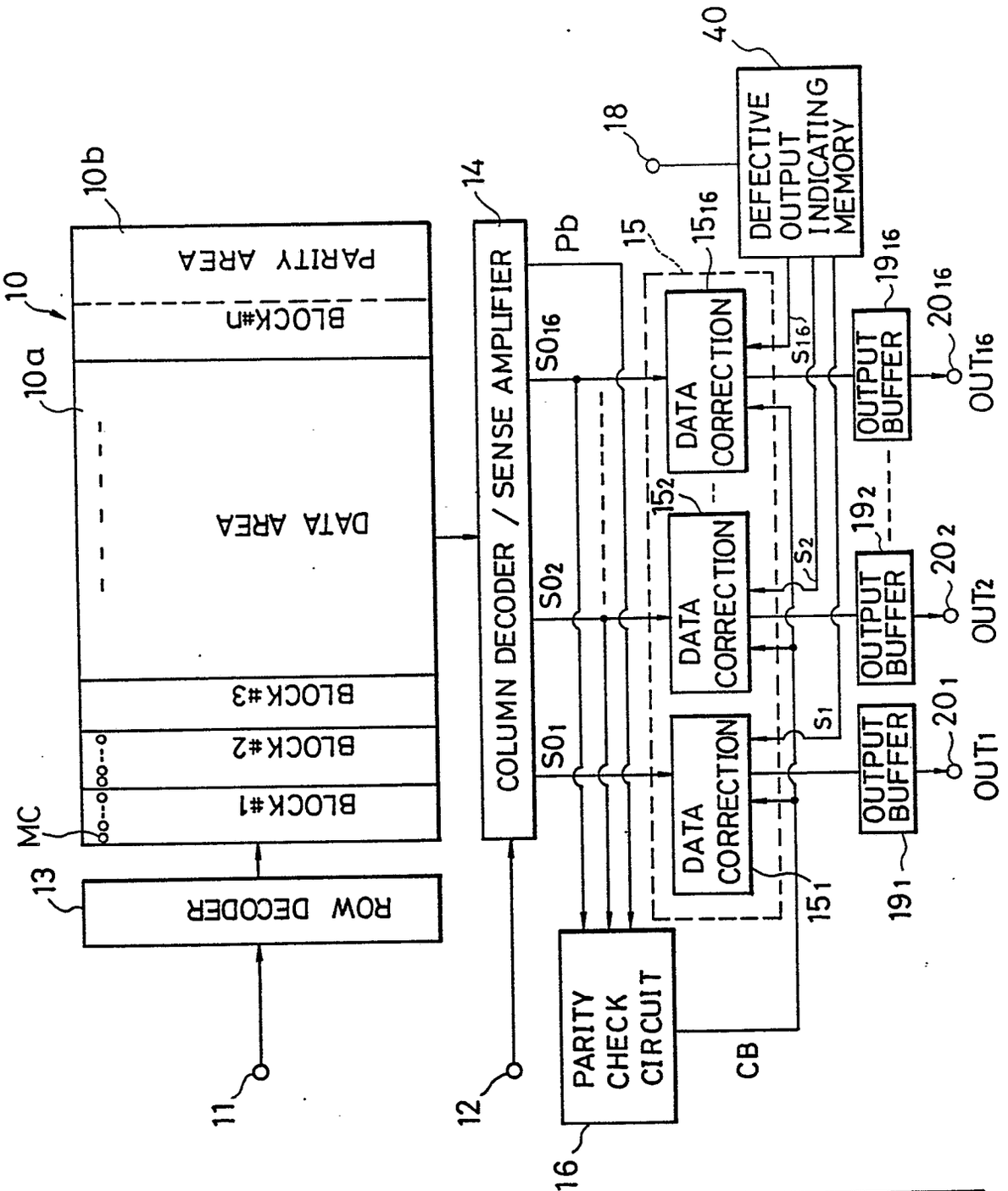


FIG. 6

4TH SUB-BLOCK
3RD SUB-BLOCK
2ND SUB-BLOCK
1ST SUB-BLOCK

FIG. 7

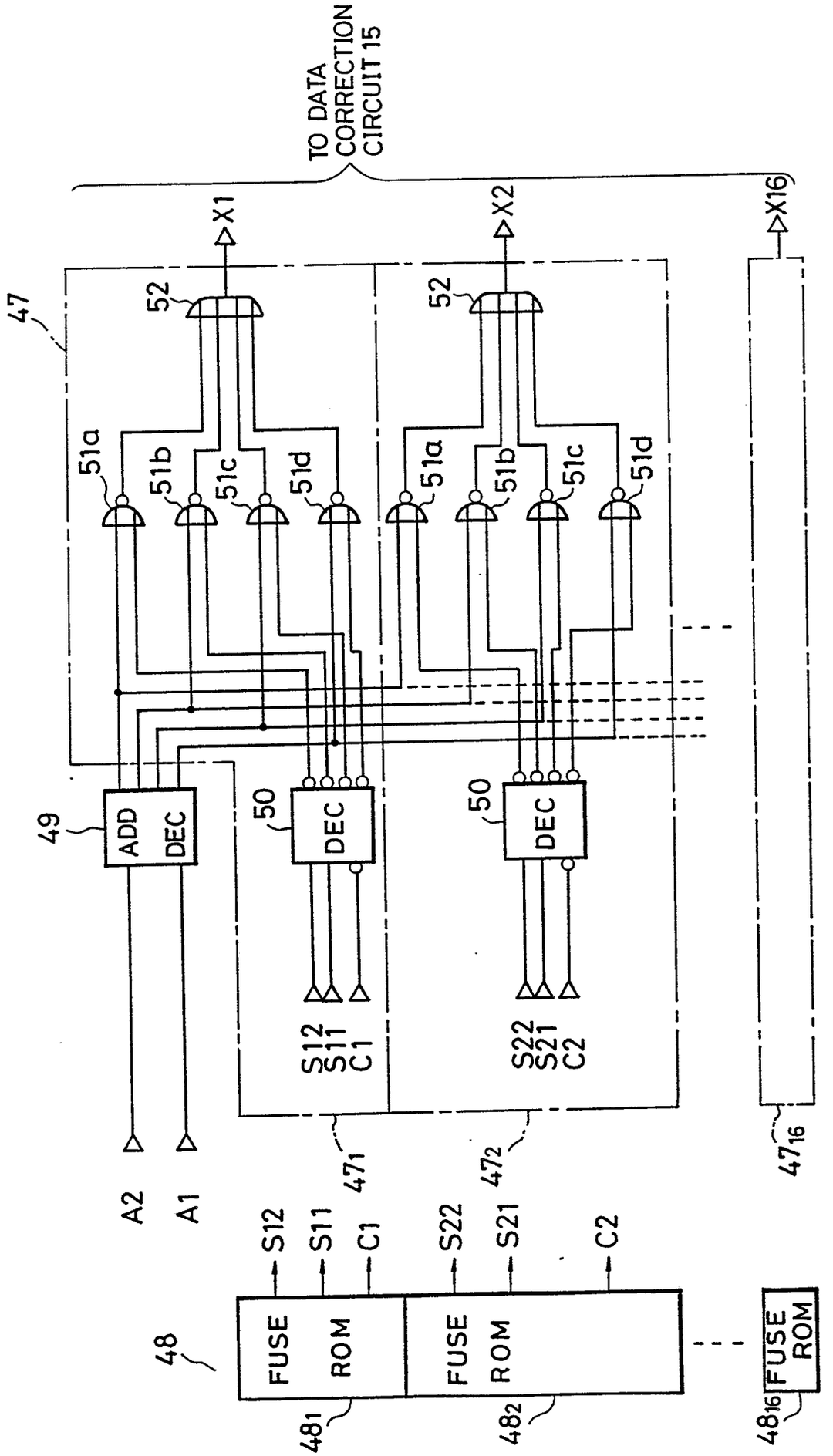

40
TO DATA CORRECTION CIRCUIT 15
X1
X2
X16
47
52
51a
51b
51c
51d
49
ADD
DEC
50
DEC
S12
S11
C1
S22
S21
C2
47_1
47_2
47_{16}
A2
A1
48
FUSE ROM
48_1
48_2
48_{16}

FIG. 8

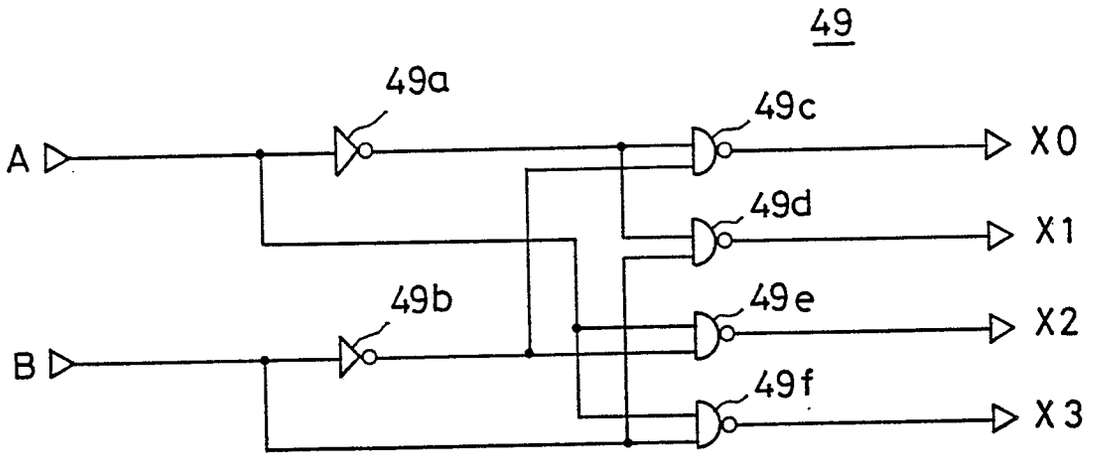

49
49a
49b
49c
49d
49e
49f
A
B
X0
X1
X2
X3

FIG. 9

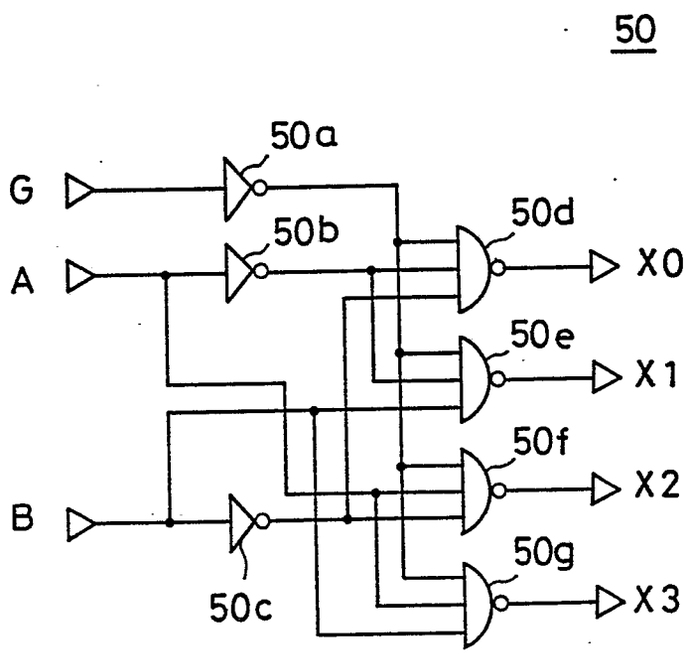
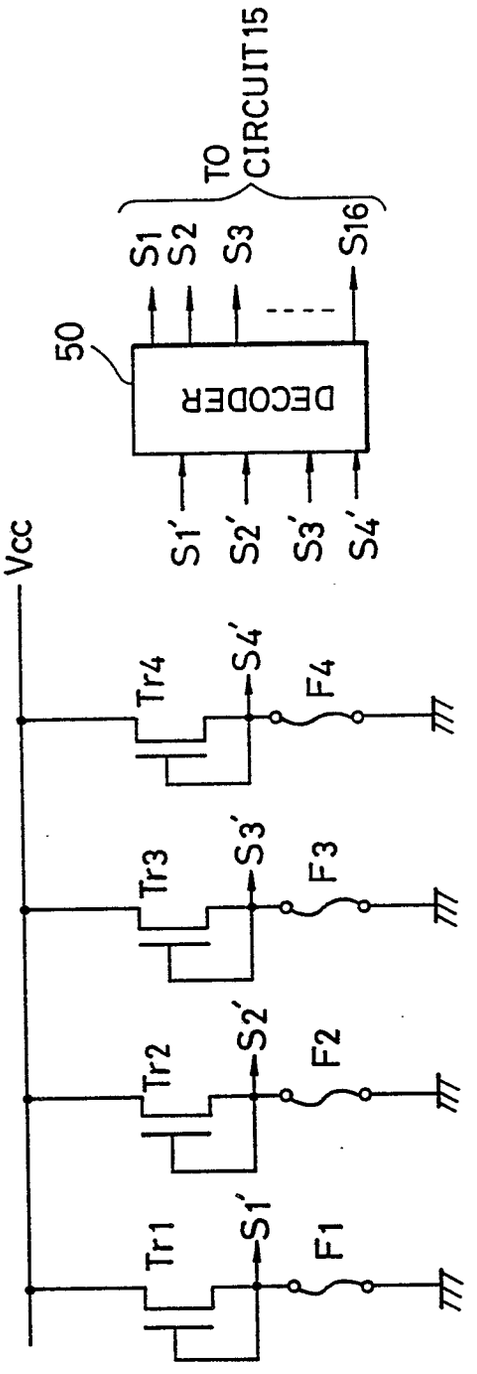

50
50a
50b
50c
50d
50e
50f
50g
G
A
B
X0
X1
X2
X3

FIG. 10


TO CIRCUIT 15
S1
S2
S3
S16
50
DECODER
S1'
S2'
S3'
S4'
Vcc
Tr4
S4'
F4
Tr3
S3'
F3
Tr2
S2'
F2
Tr1
S1'
F1

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 90300881.1

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl 5)
X	US - A - 4 780 875 (HITACHI) * Abstract; column 1, lines 5-49; column 1, line 60 - column 2, line 24; claims 1,3; fig. 1 *	1,11	G 11 C 11/34 G 11 C 17/10 G 06 F 11/10

TECHNICAL FIELDS SEARCHED (Int Cl 5)

G 11 C
G 06 F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	29-05-1990	GRÖSSING

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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