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(54) **Semiconductor device and method of manufacturing the same**

Halbleiteranordnung und Verfahren zu seiner Herstellung

Dispositif à semi-conducteur et son procédé de fabrication

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Description

BACKGROUND OF THE INVENTION

[0001] This invention relates to a semiconductor device and a method of manufacturing the same, and more particularly to a semiconductor device including a plurality of logic elements and memory elements formed on the same substrate, and a method of manufacturing such a semiconductor device.

[0002] Document D1 (GB-A-2 080 024) discloses a semiconductor device including a plurality of peripheral circuit elements and memory elements formed on the same substrate, comprising a region where said peripheral elements are formed, including a first field inversion preventive layer having a first impurity concentration below a first field oxide film for isolating said peripheral circuit elements, and a region where said memory elements are formed, including a second field inversion preventive layer below a second field oxide film for isolating said memory elements and having a second impurity concentration higher than said first impurity concentration.

[0003] Document D2 (US-A-4 637 128) discloses a semiconductor device only including a plurality of memory elements formed on a substrate having flat element regions and inclined portions formed by anisotropic etching and an oxidation retardant film. Below a field oxide film there is provided a field inversion preventive layer including a first impurity portion in all the flat element region not adjoining an active region of said memory elements, and a second impurity portion having an impurity concentration lower than that of said first impurity portion only at the inclined portions and adjoining an active region of said memory elements.

[0004] Semiconductor devices including logic elements and memory elements formed on the same substrate have been conventionally proposed.

[0005] In such conventional semiconductor devices, different problems exist depending upon whether memory elements to be formed on the same substrate as that on which logic elements are formed are of SRAM or DRAM structure, or EPROM or EEPROM structure, respectively.

[0006] Initially, where the memory element is SRAM or DRAM structure, since a memory capacity more than a predetermined value (e.g., 256 k bits) is generally required as the memory capacity, it is necessary to allow the element isolation width by the field oxide film to be more fine than in the case of the logic element. To realize this, the impurity concentration of the field inversion preventive layer must be higher than that in the case of forming only logic elements in order to prevent a punch-through. Thus, a field inversion preventive layer having a high concentration will be also formed on the logic element side.

[0007] However, when such a field inversion preventive layer having a high concentration is formed on the logic element side in this way, a large electric capacitor is formed between element formation region and the field inversion preventive layer adjacent to each other resulting in the problem that the operating oposed on the logic element side is retarded.

[0008] On the other hand, also in the case where the memory element is of EPROM or EEPROM structure, a memory capacity more than a predetermined value is similarly required. For this reason, the impurity concentration of the field inversion preventive layer must be higher than that in the case of forming only logic elements on the substrate. However, since a junction withstand voltage capable of withstanding a high program voltage is required at the same time, it is necessary to lower the impurity concentration of the portion adjoining the device formation region of the field inversion preventive layer. Accordingly, the impurity concentration of the field inversion preventive layer in this case must be lower than that in the case of forming only logic elements on the substrate at the portion adjoining the device formation region, and must be higher than that in the same case as above at the central portion which does not adjoin the device formation region. However, since both field inversion preventive layers have been conventionally formed at the same time as described above, there is a problem that such layers having different concentrations are unable to be formed.

SUMMARY OF THE INVENTION

[0009] Accordingly, an object of the invention is to provide a semiconductor device capable of satisfying charcteristics required for respective logic and memory elements of a semiconductor device on which logic elements and memory elements are formed at the same time, and a method of manufacturing such a semiconductor device.

[0010] This object is solved by a semiconductor device according to claim 1 and a method according to claim 2. Further advantageous embodiments and improvements of the invention are listed in the dependent claims.

[0011] In other word, a semiconductor device according to an aspect of this invention is directed to a semiconductor device in which memory elements and logic elements are formed on the same substrate, wherein the semiconductor device is formed so that a concentration of the field inversion preventive layer below the field oxide film within the region where memory elements are formed is partially higher and partially lower than a concentration of the field inversion preventive layer below the field oxide film within the region where logic elements are formed.

[0012] For the method of manufacturing a semiconductor device according to an aspect of this invention, which realizes the above-mentioned structur, there is a method of allowing the concentrations of field inversion preventive layers within the memory element region and

within the logic element region to be differently changed, respectively, and a method of first forming field inversion preventive layers within the both regions so that they have a low concentration and implementing ion-implantation only to the memory element region for a second time under the state where the logic element region is covered with resist, to thus provide an inversion preventive layer of high concentration.

[0013] The portion close to memory elements of the inversion preventive layer on the memory element side is allowed to have a concentration lower than that of the inversion preventive layer on the logic element side and the central portion away from the memory elements is allowed to have a concentration higher than that of the inversion preventive layer on the logic element side. This is performed by varying a mask for ion-implantation at two stages.

[0014] Since the first field inversion preventive layer formed below the first field oxide film for isolating logic elements has a first relatively low impurity concentration, the electric capacitor formed between the first field inversion preventive layer and the logic element formation region is small, resulting in no possibility that the operating speed is lowered. On the other hand, since the second field inversion preventive layer formed below the second field oxide film for isolating memory elements has a second impurity concentration higher than the first impurity concentration, punch-through is also prevented in the case where the device solution width of the field oxide film becomes narrow for the purpose of miniaturization.

[0015] Furthermore, since the impurity concentration of the portion adjoining the logic element formation region of the second field inversion preventive layer is a third impurity concentration lower than the first impurity concentration, and the portion which does not adjoin the logic element formation region thereof is a second impurity concentration higher than the first impurity concentration, concentration of an electric field between the device formation region and the second field inversion preventive layer is prevented, resulting in an increased junction withstand voltage. In addition, since the impurity concentration is high in the portion which does not adjoin the memory element formation region, the field inversion voltage increases.

[0016] Accordingly, the device and the method according to this invention are effective in carrying out descaling and increasing withstand voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] In the accompanying drawings:

FIGS. 1A to 1F are device cross sections showing a sequence of process steps of a method of manufacturing a semiconductor device according to a first example leading to this invention, respectively,

FIGS. 2A to 2F are device cross sections showing a sequence of process steps of a method of manufacturing a semiconductor device according to a second example leading to this invention, respectively,

FIGS. 3A to 3F are device cross sections showing a sequence of process steps of a method of manufacturing a semiconductor device according to a third example leading to this invention, respectively,

FIG. 4 is a device cross section showing a process steps of a method of manufacturing a semiconductor device according to a further example leading to this invention,

FIG. 5 is a device cross section showing a process step of a method of manufacturing a semiconductor device according to a further different example leading to this invention,

FIGS. 6A to 6F are device cross sections showing a sequence of process steps of a method of manufacturing a semiconductor device according to a preferred embodiment of this invention, respectively,

FIG. 7 is an explanatory view showing the relationship between the device isolation width and the punch-through voltage in the semiconductor device of this invention,

FIG. 8 is an explanatory view showing the relationship between the impurity concentration and the field inversion voltage of the memory element in the semiconductor device of this invention, and

FIG. 9 is an explanatory view showing the relationship between the impurity concentration and the junction withstand voltage in the semiconductor device of this invention.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Initially, a first example for forming a SRAM as a memory element on the same substrate as that for the CPU as a logic element will be described. FIGS. 1A to 1F are device cross sections showing a sequence of process steps in this case, respectively.

[0019] After a p-type well 101 is formed in an n-type semiconductor substrate 100, the surface of the substrate is thermally oxidized at a temperature of 900°C to form an oxide film 102 having a thickness of 500Å then form a silicon nitride film 103 by CVD process on the surface thereof (FIG. 1A). A resist 104 is then formed on the entire surface. The device structure thus obtained is subjected to an exposure process. Then, patterning is implemented to the resist portion only on the logic element side. A photolithographic process using the patterned resist as an etching mask is used to implement patterning to the silicon nitride film 103 portion only on the logic element side. Thus, there is formed a silicon nitride film 103a the portion thereof where a field inversion preventive layer is to be formed being removed. It is to be noted that on the memory element side, since the entire surface is covered with the resist 104, no etch-

ing process is carried out in effect. Then, boron (B) ions are implanted at a dose of $3x10^{13}$ atoms/cm^2 using the silicon nitride film 103a and the resist 104a on the logic element side and the silicon nitride film 103 side and the resist 104 on the memory element as masks (FIG. 1B) to form a field inversion preventive layer 105a only in the logic element side (FIG. 1C).

[0020] A field inversion preventive layer is then formed on the memory element side. To realize this, the resist films 104a and 104 are removed once to coat a resist on the entire surface for a second time. The portion on the logic element side is allowed to be covered with a resist 104c. The silicon nitride film 103 is subjected to patterning using a photolithographic process on the memory element side. Thus, there is formed a silicon nitride film 103b the portion thereof where the field inversion preventive layer is to be formed, being removed. Ion-implantation of boron (B) is carried out at a dose of $7x10^{13}$ atoms/cm^2 using the silicon nitride film 103b and the resist 104b on the memory element side, and the silicon nitride film 103a element side and the resist 104c on the logic as masks (FIG. 1C). Thus, a field inversion preventive layer 105b is formed only in the memory element side.

[0021] After the resist films 104b and 104c are removed, oxidation is carried out in the atmosphere of oxidation. Thus, field oxide films 106 having a thickness of 4000 to 6000Å are formed within both the device isolation region on the logic element side and that on the memory element side (FIG. 1D).

[0022] The silicon nitride films 103b and 103a are then removed (FIG. 1E). The entire surface is thermally oxidized to form an oxide film to deposit thereon polysilicon by CVD process. Then both films are subjected to patterning so that only the gate electrode formation region is left to form gate electrodes 108 of polysilicon and an interconnection 110 (FIG. 1F). At times subsequent thereto, an SRAM is formed within the device formation region on the memory element side and logic elements are formed within the device formation region on the logic element side.

[0023] It is to be noted that since the field inversion preventive layer at the boundary portion between the device formation region on the logic element side and that on the memory element side is such that the width of the field oxide film 106 is ordinarily broad, there is no possibility that punch-through may take place. Thus, this field inversion preventive layer may be formed in conformity with the concentration on either side. Alternatively, a method may be employed in which the half on the logic element side of the field inversion preventive layer is formed so that it has a low concentration and the half on the memory element side thereof is formed so that it has a high concentration.

[0024] As stated above, the field inversion preventive layer on the logic element side and that on the memory element side may be formed in a manner that they have impurity concentrations different from each other. Thus, the field inversion preventive layer on the logic element side is formed so that it has a relatively low impurity concentration, thus preventing an unnecessary electric capacitor from being added to the boundary portion with the device formation region. As a result, lowering of the operating speed can be prevented. On the other hand, as seen from FIG. 7 showing the relationship between the device isolation width and the punch-through voltage, the field inversion preventive layer on the memory element side is formed so that it has an impurity concentration higher than that of the logic element, whereby a high punch-through voltage can be provided and the memory integration can be increased even in the case where a field oxide film narrow in width is formed for the purpose of descaling.

[0025] A second example for forming a SRAM on the same substrate as that for CPU in the same manner as in the first example will now be described. FIGS. 2A to 2F are device cross sections showing a sequence of process steps in this case, respectively.

[0026] This example differs from the first example in the order in which impurity ions are implanted into the region on the logic element side and that on the memory element side, respectively.

[0027] An oxidation film 202 and a silicon nitride film 203 are formed on a substrate 200 (FIG. 2A). Patterning is then implemented to the nitride film 203 using the photolithographic process to form a silicon nitride film 203a the portion thereof where a field inversion preventive layer only on the memory element side is to be formed being removed. Using the silicon nitride film 203a on the memory element side, the silicon nitride film 203 on the logic element side, and resists 204a and 204 formed upon these films as masks, boron (B) ions are implanted at a dose of $7x10^{13}$ atoms/cm^2 (FIG. 2B) to form a field inversion preventive layer 205b only on the memory element side (FIG. 2C).

[0028] Then, the resist films 204a and 204 are once removed to coat a resist on the entire surface for a second time. The silicon nitride film 203 is subjected to patterning using the photolithographic process to form a silicon nitride film 203b the portion thereof where a field inversion preventive layer on the logic element side is to be formed, being removed. Using the silicon nitride film 203b, the silicon nitride film 203a on the logic element side, and resists 204b and 204c on these films as a mask, boron (B) ions are implanted at a dose of $3x10^{13}$ atoms/cm^2 (FIG. 2C) to form a field inversion preventive layer 205a on only on the logic element side.

[0029] In a manner similar to the above at subsequent times, after the resist films 204b and 204c are removed, oxidation is carried out in the atmosphere of oxidation to thereby form a field oxide film 206 having a thickness of 4000 to 6000Å within both the device isolation region on the logic element side and that on the memory element side (FIG. 2D).

[0030] After the silicon nitride films 203b and 203a are removed in the same manner as in the first embodiment

(FIG. 2E), a SRAM is formed within the device formation region on the memory element side and a CPU is formed within that on the logic element side.

[0031] FIGS. 3A to 3F are device cross sections showing a sequence of process steps according to a third example, respectively. This example is characterized in that ion-implantation is first implemented at a low dose to the regions forming the both field inversion preventive layers thereafter to implement an ion-implantation at a higher dose only to the region on the memory element side for a second time.

[0032] An oxidation film 302 and a silicon nitride film 303 are formed on the surface of a semiconductor substrate 300 (FIG. 3A). The silicon nitride film 303 on the memory element side and that on the logic element side are subjected to patterning using the photolithographic process to form a silicon nitride film 303a portion thereof where a field inversion preventive layer is to be formed, being removed. Using the silicon nitride film 303a and resist film 304 as a mask, boron (B) ions are implanted at a dose of $3x10^{13}$ atoms/cm^2 (FIG. 3B). Field inversion preventive layers 305a and 305b are formed within the field oxidation formation region on the logic element side and that on the memory element side so that they have the same impurity concentration, respectively.

[0033] The resist film 304 is then removed once to coat a resist on the entire surface for a second time. The resist film thus coated is subjected to patterning by the same pattern as above on only the memory element side to form a resist film 304a the portion thereof where a field inversion preventive layer is to be formed, being removed. Using the resist film 304a and the silicon nitride film 303a as a mask, boron (B) ions are implanted at a dose of $4x10^{13}$ atoms/cm^2 (FIG. 3C), thus allowing only the field inversion preventive layer 305b on the memory element side to have a high impurity concentration.

[0034] At times subsequent thereto, in the same manner as in the first and second examples, a field oxidation film 306 having a thickness of 4000 to 6000A is formed within the device isolation region (FIG. 3D). After the silicon nitride film 303a is removed (FIG. 3E), a SRAM is formed on the memory element side and a CPU is formed on the logic element side (FIG. 3F).

[0035] FIG. 4 shows a cross sectional view in the case where a DRAM as the memory element is formed on the same substrate as that for CPU wherein a diffused layer for an n-type capacitor is formed within a DRAM formation region. By using any one of the methods of the above-described first to third examples it is possible to form a field inversion preventive layer 405a having a low impurity concentration on the logic element side, and to form a field inversion preventive layer 405b having a high impurity concentration on the memory element side.

[0036] FIG. 5 shows an example where a DRAM as the memory element is formed in the same manner as in the case of FIG. 4. This example differs from the example of FIG. 4 only in that not only a field inversion preventive layer 505a but also a trench buried polysilicon 513 are formed below a field oxide film 506a on the memory element side. Also in this case, by using any one of the methods of the above-described first to third examples, it is possible to form a field inversion preventive layer 505a having a low impurity concentration on the logic element side, and to form a field inversion preventive layer 505b having a high impurity concentration on the memory element side.

[0037] A preferred embodiment for forming an EEPROM as the memory element simultaneously with formation of a CPU will now be described. In this case, unlike the first to third examples, the field inversion preventive layer on the memory element side is formed in a manner that a portion adjoining the device formation region and a portion which does not adjoin it have impurity concentrations different from each other.

[0038] FIGS. 6A to 6F are device cross sections showing a sequence of process steps in this case, respectively. In this embodiment, a p-type well 601 is formed only on the logic element side of a p-type semiconductor substrate 600. This is because logic elements are formed in the state of the semiconductor substrate 600 having a low concentration impurity in order to eliminate a voltage drop. Other process steps will be implemented in the same manner as in the first to third examples. Namely, the surface of the substrate 600 is thermally oxidized at a temperature of 900 degrees to form an oxide film 602 having a thickness of 500Å to form a silicon nitride film 603 by CVD process on the surface of the oxide film 602 (FIG. 6A).

[0039] Then, silicon nitride film 603 on the memory element side and that on the logic element side are subjected to patterning by using the photolithographic process to form a silicon nitride film 603a from which the portion where a field inversion preventive layer is to be formed is removed. Then, a resist film 604 is formed only on the memory element side.

[0040] Subsequently, using the resist film 604 and the silicon nitride film 603a as a mask, boron (B) ions are implanted at a dose of $3x10^{13}$ atoms/cm^2 to form a field inversion preventive layer 605a on the logic element side (FIG. 6B).

[0041] The resist film 604 is then removed once to form a resist film 604a only on the logic element side.

[0042] Using the resist film 604a and the silicon nitride film 603a as a mask, boron (B) ions are implanted at a dose of $1.5x10^{13}$ atoms/cm^2 (FIG. 6C) to first form a field inversion preventive layer 605b having a low impurity concentration on the memory element side.

[0043] After the resist film 604a is removed, a resist is coated on the entire surface. Then, patterning is implemented so that the resist portion only on the central portion which does not adjoin elements of the field inversion preventive layer on the memory element side is removed to form a resist film 604b.

[0044] Using the resist film 604b as a mask, boron (B)

ions are implanted at a dose of $5x10^{13}$ atoms/cm^2 (FIG. 6D) to increase the impurity concentration of the central portion 605c.

[0045] At times subsequent thereto, in the same manner as in the above-described first and second embodiments, a field oxide film 606 having a thickness of 4000 to 6000Å is formed within the device isolation region (FIG. 6E) to remove therefrom the silicon oxide film 603a thereafter to form an EEPROM and a CPU within the device formation region 607 on the memory element side and that on the logic element side, respectively (FIG. 6F).

[0046] As stated above, the semiconductor device is formed in a manner that the field inversion preventive layer on the logic element side and that on the memory element side have impurity concentrations different from each other. In the case of the field inversion preventive layer on the logic element side, this layer is formed so that it has a relatively low concentration impurity to prevent an unnecessary electric capacitor from being formed, thereby making it possible to prevent lowering of the operating speed.

[0047] On the other hand, the field inversion preventive layer on the memory element side can be formed so that the portion adjoining the device formation region and the portion which does not adjoin it have concentrations different from each other. In this instance, the portion which does not adjoin the device formation region is formed so that it has an impurity concentration higher than that in the prior art. As seen from FIG. 8 showing the relationship between the field inversion voltage and the impurity concentration, a higher field inversion voltage can be thus provided. For this reason, even in the case where a high voltage is used, field inversion phenomenon can be prevented and the memory capacity of the memory element can be increased. In addition, by forming the portion adjoining the device formation region so that it has an impurity concentration lower than that of the field inversion preventive layer on the logic element side, the junction withstand voltage can be improved as compared to that of. the prior art as seen from FIG. 9 showing the relationship between the junction withstand voltage and the impurity concentration.

[0048] The above-described examples and embodiment may be modified or altered in various forms.

[0049] For example, in connection with the conductivity type of the semiconductor, conductivity types illustrated in the embodiments may be entirely reversed, respectively. In addition, the sequence of the process steps for implanting boron (B) ions may be different from that illustrated in FIG. 6. Namely, the process step for ion-implantation into the region on the logic element side shown in FIG. 6B and the process step for ion-implantation into the region on the memory element side shown in FIG. 6C may be carried out in reverse order.

[0050] Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A semiconductor device including a plurality of logic elements and memory elements formed on the same semiconductor substrate (600) having a first conductivity type (p), comprising:

a) a region where said logic elements are formed, including a first field inversion preventive layer (605a) having a first impurity concentration and said first conductivity type (p) below a first field oxide film (606) for isolating said logic elements; and

b) a region where said memory elements are formed, including a second field inversion preventive layer (605b) of said first conductivity type (p) and having a second impurity concentration lower than said first impurity concentration below a second field oxide film (606) having a width for isolating active regions (607) of said memory elements;

wherein

c) said second field inversion preventive layer (605b) comprises:

c1) a first impurity part (605c) having a third impurity concentration higher than said first impurity concentration at a substantially central portion of the bottom surface of said second field oxide film (606);

c2) said first impurity part (605c) having a first width sufficient for preventing current from flowing due to inversion under the second field oxide film (606); and

c3) a second impurity part (605b) having said second impurity concentration lower than said first impurity concentration at a majority portion of the bottom surface of said second field oxide film (606),

c4) said second impurity part (605b) having sufficient width from an active region (607) of the memory region to the second impurity part (605c) for preventing punch-through current; and

c5) wherein said first impurity part (605c) does not adjoin active regions (607) of said memory elements and extends deeper into said semiconductor substrate (600) than said second impurity part (605b); and

c6) wherein said second impurity part

(605b) adjoins active regions (607) of said memory elements.

2. A method of manufacturing a semiconductor device including a logic element region and a memory element region formed on the same semiconductor substrate (600) having a first conductivity type (p), comprising the following steps:

a) forming (fig. 6A) an oxide film (602) and an oxidation resistive film (603) on a surface of said semiconductor substrate (600);

b) patterning and removing (fig. 6B) parts of said oxidation resistive film (603)

- to expose a first portion of said oxide film (602) to be used for forming a first field oxide film (606) isolating logic elements in said logic element region; and
- to expose a second portion of said oxide film (602) to be used for forming a second field oxide film (606) for isolating memory elements in said memory element region; and

c) coating (fig. 6B) a first resist film (604) on said exposed second portion of said oxide film (602) and said remaining parts of said oxidation resistive film (603a) on the memory element region only;

d) implanting (fig. 6B) impurity ions (B+) of said first conductivity type (p), by using said first resist film (604) in said memory element region and said remaining parts of said oxidation resistive film in said logic element region as masks, through said first portion of said oxide film (602) into said semiconductor substrate (600, 601) for forming a first field inversion preventive layer (605a) having said first conductivity type (p) and a first impurity concentration close to the surface of said semiconductor substrate (600, 601) at said first portion;

e) removing (fig. 6C) said first resist film (604) from said memory element region and forming a second resist film (604a) on said exposed first portion of said oxide film (602) and said remaining parts of said oxidation resistive film (603a) on the logic element side only;

f) implanting (fig. 6C) impurity ions (B+) of said first conductivity type (p), by using said second resist film (604a) in said logic element region and said remaining parts of said oxidation resistive film (603a) in said memory element region as masks, through said second portions of said oxide film (602) into said semiconductor substrate (600) for forming a second field inversion preventive layer (605b) having said first conductivity type (p) and a second impurity concentration lower than said first impurity concentration close to the surface of said semiconductor substrate (600) at said second portions;

g) removing (fig. 6D) said second resist film (604a) from said logic element side and thereafter coating a third resist film (604b) on said field oxide film (602) at said first and second portions and said remaining parts of said oxidation resistive film (603a) on said logic element and said memory element side and patterning said third resist film (604b) at said memory element side and removing said third resist film (604a) at a third portion positioned at a central portion of said second field inversion preventive layers (605b); and

h1) implanting (fig. 6D) impurity ions (B+) of said first conductivity type (p), by using said third resist film (604a) in said logic element region and in said memory element side as masks, through said third portion into said semiconductor substrate (600, 602; 605b) for forming at said central portion a third region (605c) close to the surface of said semiconductor substrate (600, 602) having a third impurity concentration higher than said first impurity concentration;

h2) wherein in said step h1) said third central region (605c) is formed such that it extends deeper into the semiconductor substrate (600) than the remaining regions (605b) of said second field inversion preventive layer (605b), whereby

i1) said third region (605c) is made to have a first width sufficient for preventing current from flowing due to inversion under said second field oxide film (606); and

i2) said remaining regions (605b) are made to extend over a majority portion of the bottom surface of said second field oxide film and to have sufficient width from an active region (607) of the memory region to said third region (605c) for preventing punch-through current.

3. A device according to claim 1,
characterized in that,
said first field inversion preventive film (605a) in said logic element side is formed in a well (601) hav-

ing said first conductivity type (p).

4. A method according to claim 2, ***characterized in that,*** before step a) a well (601) having said first conductivity type (p) is formed in said semiconductor substrate (600) on said logic element side and said first field inversion preventive film (605a) is formed in said well (601).

5. A method according to claim 2, ***characterized in that,*** after step h) said third resist film (604b) is removed on said logic element side and said memory element side and said oxide film (602) is oxidized (fig. 6E) thus forming said first and second fields oxide films (606) isolating said logic elements in said logic element region and said memory elements in said memory element region.

6. A method according to claim 5, ***characterized in that,*** said remaining parts of said oxidation resistive films (603a) are removed (fig. 6F), the surface is oxidized for forming another oxide film, a polysilicon film is placed thereon and said polysilicon film and said another oxide film are patterned for forming electrode regions of polysilicon and interconnection regions (610).

7. A method according to claim 5, ***characterized in that,*** in active regions (607) in said logic element side and said memory element side a CPU and a EEPROM is formed.

8. A device according to claim 1, ***characterized in that,*** at a boundary portion (fig. 6F) between said region in which logic elements are formed and said region where memory elements are formed said first and second field oxide-films (606; 606) are joined and a field inversion prevention layer at this boundary portion has a concentration of either said first or said second field inversion preventive layers (605a; 605b).

9. A device according to claim 8, ***characterized in that,*** at said boundary portion (fig. 6F) between said region in which logic elements are formed and said region where memory elements are formed the width of said field oxide films (606; 606) is ordinarily broad, such that punch-through between the logic element side and the memory element side is prevented.

Patentansprüche

1. Halbleitereinrichtung mit einer Vielzahl von Logikelementen und Speicherelementen, die auf dem gleichen Halbleitersubstrat (600), das einen ersten Leitfähigkeitstyp (p) aufweist, gebildet sind, umfassend:

a) einen Bereich, wo die Logikelemente gebildet sind, mit einer ersten Feldinversions-Verhinderungsschicht (605a), die eine erste Verunreinigungskonzentration und den ersten Leitfähigkeitstyp (p) aufweist, unter einem ersten Feldoxidfilm (606) zum Isolieren der Logikelemente; und

b) einen Bereich, wo die Speicherelemente gebildet sind, mit einer zweiten Feldinversions-Verhinderungsschicht (605b) des ersten Leitfähigkeitstyps (p) und mit einer zweiten Verunreinigungskonzentration kleiner als die erste Verunreinigungskonzentration unter einem zweiten Feldoxidfilm (606) mit einer Breite zum Isolieren von aktiven Bereichen (607) der Speicherelemente;

wobei

c) die zweite Feldinversions-Verhinderungsschicht (605b) umfasst:

c1) einen ersten Verunreinigungsteil (605c) mit einer dritten Verunreinigungskonzentration höher als die erste Verunreinigungskonzentration an einem im wesentlichen zentralen Abschnitt der Bodenfläche des zweiten Feldoxidfilms (606);

c2) wobei der erste Verunreinigungsteil (605c) eine erste Breite aufweist, die ausreicht, um zu verhindern, dass aufgrund einer Inversion unter dem zweiten Feldoxidfilm (606) ein Strom fließt; und

c3) einen zweiten Verunreinigungsteil (605b), der die zweite Verunreinigungskonzentration kleiner als die erste Verunreinigungskonzentration aufweist an einem Hauptabschnitt der Bodenfläche des zweiten Feldoxidfilms (606) ;

c4) wobei der zweite Verunreinigungsteil (605b) eine ausreichende Breite von einem aktiven Bereich (607) des Speicherbereichs zu dem zweiten Verunreinigungsteil (605c) zum Verhindern eines Durchschlagstroms aufweist; und

c5) wobei der erste Verunreinigungsteil (605c) an aktive Bereiche (607) der Speicherelemente nicht angrenzt und sich tiefer in das Halbleitersubstrat (600) als der zweite Verunreinigungsteil (605b) erstreckt; und

c6) wobei der zweite Verunreinigungsteil (605b) an aktive Bereiche (607) der Speicherelemente angrenzt.

2. Verfahren zum Herstellen einer Halbleitereinrichtung mit einem Logikelementbereich und einem Speicherelementbereich, die auf dem gleichen Halbleitersubstrat (600) gebildet sind, das einen ersten Leitfähigkeitstyp (p) aufweist, umfassend die folgenden Schritte:

a) Bilden (Fig. 6A) eines Oxidfilms (602) und eines oxidationsbeständigen Films (603) auf einer Oberfläche des Halbleitersubstrats (600);

b) Strukturieren und Entfernen (Fig. 6B) von Teilen des oxidationsbeständigen Films (603);

- zum Freilegen eines ersten Abschnitts des Oxidfilms (602), der zum Bilden eines ersten Feldoxidfilms (606) verwendet werden soll, der Logikelemente in dem Logikelementbereich isoliert; und
- zum Freilegen eines zweiten Abschnitts des Oxidfilms (602), der zum Bilden eines zweiten Feldoxidfilms (606) zum Isolieren von Speicherelementen in dem Speicherelementbereich verwendet werden soll; und

c) Aufschichten (Fig. 6B) eines ersten Resistfilms (604) auf den freigelegten zweiten Abschnitt des Oxidfilms (602) und die übrigen Teile des oxidationsbeständigen Films (603a) auf nur dem Speicherelementbereich;

d) Implantieren (Fig. 6B) von Verunreinigungsionen (B+) des ersten Leitfähigkeitstyps (p) durch Verwenden des ersten Resistfilms (604) in dem Speicherelementbereich und den übrigen Teilen des oxidationsbeständigen Films in dem Logikelementbereich als Masken, durch den ersten Abschnitt des Oxidfilms (602) in das Halbleitersubstrat (600, 601) hinein, zum Bilden einer ersten Feldinversions-Verhinderungsschicht (605a), die den ersten Leitfähigkeitstyp (p) und eine erste Verunreinigungskonzentration aufweist, nahe zu der Oberfläche des Halbleitersubstrats (600, 601) an dem ersten Abschnitt;

e) Entfernen (Fig. 6C) des ersten Resistfilms (604) von dem Speicherelementbereich und Bilden eines zweiten Resistfilms (604a) auf dem freigelegten ersten Abschnitt des Oxidfilms (602) und den übrigen Teilen des Oxidationswiderstandsfilms (603a) nur auf der Logikelementseite;

f) Implantieren (Fig. 6C) von Verunreinigungsionen (B+) des ersten Leitfähigkeitstyps (p) durch Verwenden des zweiten Resistfilms (604a) in dem Logikelementbereich und den übrigen Teilen des oxidationsbeständigen Films (603a) in dem Speicherelementbereich als Masken, durch die zweiten Abschnitte des Oxidfilms (602) in das Halbleitersubstrat (600) hinein, zum Bilden einer zweiten Feldinversions-Verhinderungsschicht (605b), die den ersten Leitfähigkeitstyp (p) und eine zweite Verunreinigungskonzentration niedriger als die erste Verunreinigungskonzentration aufweist, in der Nähe der Oberfläche des Halbleitersubstrats (600) an den zweiten Abschnitten;

g) Entfernen (Fig. 6D) des zweiten Resistfilms (604a) von der Logikelementseite und danach Aufbringen eines dritten Resistfilms (604b) auf den Feldoxidfilm (602) an den ersten und zweiten Abschnitten und den übrigen Teilen des Oxidationswiderstandsfilms (603a) auf der Logikelement- und der Speicherelement-Seite und Strukturieren des dritten Resistfilms (604b) auf der Speicherelementseite und Entfernen des dritten Resistfilms (604a) an einem dritten Abschnitt, der an einem zentralen Abschnitt der zweiten Feldinversions-Verhinderungsschichten (605b) positioniert ist; und

h1) Implantieren (Fig. 6D) von Verunreinigungsionen (B+) des ersten Leitfähigkeitstyps (p) durch Verwenden des dritten Resistfilms (604a) in dem Logikelementbereich und der Speicherelementseite als Masken, durch den dritten Abschnitt in das Halbleitersubstrat (600, 602; 605b) hinein, zum Bilden eines dritten Bereichs (605c) in der Nähe der Oberfläche des Halbleitersubstrats (600, 602) mit einer dritten Verunreinigungskonzentration höher als die erste Verunreinigungskonzentration an dem zentralen Abschnitt;

h2) wobei in dem Schritt h1) der dritte zentrale Bereich (605c) so gebildet wird, dass er sich tiefer in das Halbleitersubstrat (600) hinein als die übrigen Bereiche (605b) der zweiten Feldinversions-Verhinderungsschicht (605b) erstreckt;
wobei

i1) der dritte Bereich (605c) gebildet wird, um eine erste Breite aufzuweisen, die ausreicht, um zu verhindern, dass ein Strom aufgrund einer Inversion unter dem zweiten Feldoxidfilm (606) fließt; und

i2) die übrigen Bereiche (605b) gebildet werden, um sich über einen Hauptabschnitt der Bodenfläche des zweiten Feldoxidfilms zu erstrecken und eine ausreichende Breite von einem aktiven Bereich (607) des Speicherbereichs zu dem dritten Bereich (605c) zum Verhindern eines Durchbruchstroms aufweisen.

3. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet, dass** der erste Feldinversionsverhinderungsfilm (605a) in der Logikelementseite in einer Wanne (601) gebildet ist, die den ersten Leitfähigkeitstyp (p) aufweist.

4. Verfahren nach Anspruch 2, **dadurch gekennzeichnet, dass** vor dem Schritt a) eine Wanne (601), die den ersten Leitfähigkeitstyp (p) aufweist, in dem Halbleitersubstrat (600) auf der Logikelementseite gebildet wird und der erste Feldinversionsverhinderungsfilm (605a) in der Wanne (601) gebildet wird.

5. Verfahren nach Anspruch 2, **dadurch gekennzeichnet, dass** nach dem Schritt h) der dritte Resistfilm (604b) auf der Logikelementseite und der Speicherelementseite entfernt wird und der Oxidfilm (602) oxidiert (Fig. 6E) wird, wodurch die ersten und zweiten Feldoxidfilme (606) gebildet werden, die die Logikelemente in dem Logikelementbereich und die Speicherelemente in dem Speicherelementbereich isolieren.

6. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, dass** die übrigen Teile der oxidationsbeständigenFilme (603a) entfernt (Fig. 6F) werden, die Oberfläche zum Bilden eines anderen Oxidfilms oxidiert wird, ein Polysiliziumfilm darauf platziert wird und der Polysiliziumfilm und der andere Oxidfilm zum Bilden von Elektrodenbereichen von Polysilizium- und Zwischenverbindungsbereichen (610) strukturiert werden.

7. Verfahren nach Anspruch 5, **dadurch gekennzeichnet, dass** in aktiven Bereichen (607) in der Logikelementseite und der Speicherelementseite eine CPU und ein EEPROM gebildet wird.

8. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet, dass** an einem Grenzabschnitt (Fig. 6F) zwischen dem Bereich, in dem Logikelemente gebildet sind, und dem Bereich, wo Speicherelemente gebildet sind, die ersten und zweiten Feldoxidfilme (606; 606) verbunden sind und eine Feldinversions-Verhinderungsschicht an diesem Grenzabschnitt eine Konzentration entweder der ersten oder der zweiten Feldinversions-Verhinderungsschicht (605a, 605b) aufweist.

9. Einrichtung nach Anspruch 8, **dadurch gekennzeichnet, dass** an dem Grenzabschnitt (Fig. 6F) zwischen dem Bereich, in dem Logikelemente gebildet sind, und dem Bereich, wo Speicherelemente gebildet sind, die Breite der Feldoxidfilme (606; 606) gewöhnlich breit sind, so dass ein Durchschlag zwischen der Logikelementseite und der Speicherelementseite verhindert wird.

Revendications

1. Dispositif à semiconducteur comportant une pluralité d'éléments logiques et d'éléments de mémoire formés sur le même substrat semiconducteur (600), qui possède un premier type de conductivité (p), comprenant :

   a) une région dans laquelle lesdits éléments logiques sont formés, comportant une première couche d'empêchement d'inversion de champ (605a), qui possède une première concentration en impureté et ledit premier type de conductivité (p), au-dessous d'une première pellicule d'oxyde de champ (606) servant à isoler lesdits éléments logiques ; et
   b) une région dans laquelle lesdits éléments de mémoire sont formés, comportant une deuxième couche d'empêchement d'inversion de champ (605b) dudit premier type de conductivité (p) et possédant une deuxième concentration en impureté inférieure à ladite première concentration en impureté, au-dessous d'une deuxième pellicule d'oxyde de champ (606) ayant une certaine largeur et servant à isoler des régions actives (607) desdits éléments de mémoire ;

   où :

   c) ladite deuxième couche d'empêchement d'inversion de champ (605b) comprend :

      c1) une première partie d'impureté (605c) ayant une troisième concentration en impureté supérieure à ladite première concentration en impureté en une partie sensiblement centrale de la surface inférieure de ladite deuxième pellicule d'oxyde de champ (606) ;
      c2) ladite première partie d'impureté (605c)

ayant une première largeur suffisante pour empêcher qu'un courant ne circule du fait d'une inversion sous la deuxième pellicule d'oxyde de champ (606); et

c3) une deuxième partie d'impureté (605b) ayant ladite deuxième concentration en impureté inférieure à ladite première concentration en impureté en une partie majeure de la surface inférieure de ladite deuxième pellicule d'oxyde de champ (606),

c4) ladite deuxième partie d'impureté (605b) ayant une largeur suffisante, d'une région active (607) de la région de mémoire à la deuxième partie d'impureté (605c), pour empêcher un courant de percement ; et

c5) où ladite première partie d'impureté (605c) n'est pas contiguë à des régions actives (607) desdits éléments de mémoire et s'étend plus profondément dans ledit substrat semiconducteur (600) que ladite deuxième partie d'impuretés (605b) ; et

c6) où ladite deuxième partie d'impureté (605b) est contiguë à des régions actives (607) desdits éléments de mémoire.

2. Procédé de fabrication d'un dispositif à semiconducteur comportant une région d'éléments logiques et une région d'éléments de mémoire formées sur le même substrat semiconducteur (600), qui possède un premier type de conductivité (p) comprenant les opérations suivantes :

a) former (figure 6A) une pellicule d'oxyde (602) et une pellicule résistant à l'oxydation (603) sur une surface dudit substrat semiconducteur (600) ;

b) appliquer un tracé de motif à des parties de ladite pellicule résistant à l'oxydation (603) et retirer ces dernières (figure 6B)

- afin d'exposer une première partie de ladite pellicule d'oxyde (602) destinée à être utilisée pour former une première pellicule d'oxyde de champ (606) isolant des éléments logiques de ladite région d'éléments logiques ; et
- afin d'exposer une deuxième partie de ladite pellicule d'oxyde (602) destinée à être utilisée pour former une deuxième pellicule d'oxyde de champ (606) servant à isoler des éléments de mémoire de ladite région d'éléments de mémoire ; et

c) déposer (figure 6B) une première pellicule d'agent sensible du type réserve, ou résist, (604) sur ladite deuxième partie exposée de ladite pellicule d'oxyde (602) et desdites parties restantes de ladite pellicule résistant à l'oxydation (603a) sur la région d'éléments de mémoire seulement ;

d) implanter (figure 6B) des ions d'impureté (B+) dudit premier type de conductivité (p), en utilisant ladite première pellicule de résist (604) de ladite région d'éléments de mémoire et desdites parties restantes de ladite pellicule résistant à l'oxydation de ladite région d'éléments logiques comme masques, à travers ladite première partie de ladite pellicule d'oxyde (602), dans ledit substrat semiconducteur (600, 601) afin de former une première couche d'empêchement d'inversion de champ (605a), ayant ledit premier type de conductivité (p) et une première concentration en impureté, à proximité de la surface dudit substrat semiconducteur (600, 601) au niveau de ladite première partie ;

e) retirer (figure 6C) de ladite région d'éléments de mémoire ladite première pellicule de résist (604) et former une deuxième pellicule de résist (604a) sur ladite première partie exposée de ladite pellicule d'oxyde (602) et les parties restantes de ladite pellicule résistant à l'oxydation (603a) du côté des éléments logiques seulement ;

f) implanter (figure 6C) des ions d'impureté (B+) dudit premier type de conductivité (p) en utilisant ladite deuxième pellicule de résist (604a) de ladite région d'éléments logiques et lesdites parties restantes de ladite pellicule résistant à l'oxydation (603a) de ladite région d'éléments de mémoire comme masques, à travers lesdites deuxièmes parties de ladite pellicule d'oxyde (602), dans ledit substrat semiconducteur (600) afin de former une deuxième couche d'empêchement d'inversion de champ (605b), ayant ledit premier type de conductivité (p) et une deuxième concentration en impureté inférieure à ladite première concentration en impureté, à proximité de la surface dudit substrat semiconducteur (600) au niveau desdites deuxièmes parties ;

g) retirer (figure 6D) dudit côté des éléments logiques ladite deuxième pellicule de résist (604a) et, après cela, déposer une troisième pellicule de résist (604b) sur ladite pellicule d'oxyde de champ (602) au niveau desdites première et deuxième parties et desdites parties restantes de ladite pellicule résistant à l'oxydation (603a) du côté desdits éléments logiques et desdits éléments de mémoire et appliquer un tracé de motif à ladite troisième pellicule de résist (604b) du côté desdits éléments de mémoire, et retirer ladite troisième pellicule de résist (604a) au niveau d'une troisième partie placée en une partie centrale desdites deuxièmes couches d'empêchement d'inver-

sion de champ (605b) ; et
h1) implanter (figure 6D) des ions d'impureté (B+) dudit premier type de conductivité (p) en utilisant ladite troisième pellicule de résist (604a) de ladite région d'éléments logiques et dudit côté des éléments de mémoire comme masques, à travers ladite troisième partie, dans ledit substrat semiconducteur (600, 602 ; 605b) afin de former, au niveau de ladite partie centrale, une troisième région (605c) à proximité de la surface dudit substrat semiconducteur (600, 602), ayant une troisième concentration en impureté supérieure à ladite première concentration en impureté ;
h2) où, dans l'opération h1), ladite troisième région centrale (605c) est formée de façon qu'elle s'étende plus profondément dans le substrat semiconducteur (600) que les régions restantes (605b) de ladite deuxième couche d'empêchement d'inversion de champ (605b),
de sorte que :

i1) ladite troisième région (605c) est amenée à avoir une première largeur suffisante pour empêcher qu'un courant ne circule du fait de l'inversion sous ladite deuxième pellicule d'oxyde de champ (606) ; et
i2) lesdites régions restantes (605b) sont amenées à s'étendre sur une majeure partie de la surface inférieure de ladite deuxième pellicule d'oxyde de champ et à avoir une largeur suffisante, d'une région active (607) de la région de mémoire à ladite troisième région (605c), afin d'empêcher un courant de percement.

3. Dispositif selon la revendication 1, **caractérisé en ce que** ladite première pellicule d'empêchement d'inversion de champ (605a) du côté desdits éléments logiques est formé dans un puits (601) ayant ledit premier type de conductivité (p).

4. Procédé selon la revendication 2, **caractérisé en ce que**, avant l'opération a), un puits (601) ayant ledit premier type de conductivité (p) est formé dans ledit substrat semiconducteur (600) du côté desdits éléments logiques et ladite première pellicule d'empêchement d'inversion de champ (605a) est formée dans ledit puits (601).

5. Procédé selon la revendication 2, **caractérisé en ce que**, après l'opération h), on retire ladite troisième pellicule de résist (604b) du côté desdits éléments logiques et du côté desdits éléments de mémoire et on oxyde ladite pellicule d'oxyde (602) (figure 6E), de manière à ainsi former lesdites première et deuxième pellicules d'oxyde de champ (606) isolant lesdits éléments logiques de ladite région d'éléments logiques et lesdits éléments de mémoire de ladite région d'éléments de mémoire.

6. Procédé selon la revendication 5, **caractérisé en ce qu'**on retire lesdites parties restantes desdites pellicules résistant à l'oxydation (603a) (figure 6F), on oxyde la surface afin de former une autre pellicule d'oxyde, on place sur celle-ci une pellicule de silicium polycristallin, et on applique un tracé de motif à ladite pellicule de silicium polycristallin et à ladite autre pellicule d'oxyde afin de former des régions d'électrodes de silicium polycristallin et des régions d'interconnexion (610).

7. Procédé selon la revendication 5, **caractérisé en ce que**, dans des régions actives (607) du côté desdits éléments logiques et du côté desdits éléments de mémoire, on forme une unité centrale de traitement, ou CPU, et une mémoire programmable électriquement effaçable, ou EEPROM.

8. Dispositif selon la revendication 1, **caractérisé en ce que**, au niveau d'une partie frontière (figure 6F) entre ladite région dans laquelle sont formés des éléments logiques et ladite région dans laquelle sont formés des éléments de mémoire, lesdites premières et deuxièmes pellicules d'oxyde de champ (606 ; 606) sont contiguës et une couche d'empêchement d'inversion de champ se trouvant au niveau de cette partie frontière possède une concentration de ladite première ou de ladite deuxième couche d'empêchement d'inversion de champ (605a, 605b).

9. Dispositif selon la revendication 8, **caractérisé en ce que**, au niveau de ladite partie frontière (figure 6F) entre ladite région dans laquelle sont formés des éléments logiques et ladite région dans laquelle sont formés des éléments de mémoire, la largeur desdites pellicules d'oxyde de champ (606 ; 606) est ordinairement grande, de sorte qu'un percement entre le côté des éléments logiques et le côté des éléments de mémoire est empêché.

FIG.1A

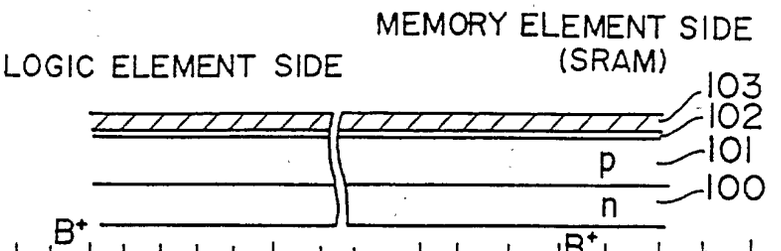


FIG.1B

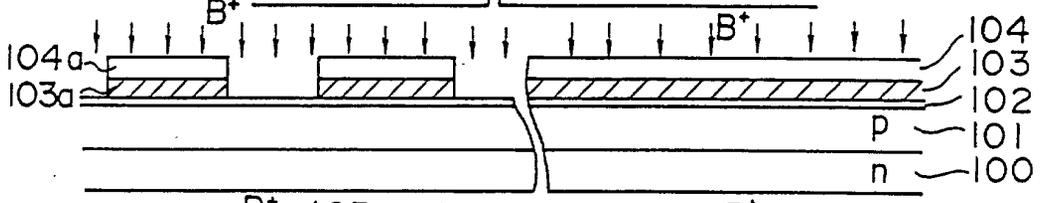


FIG.1C

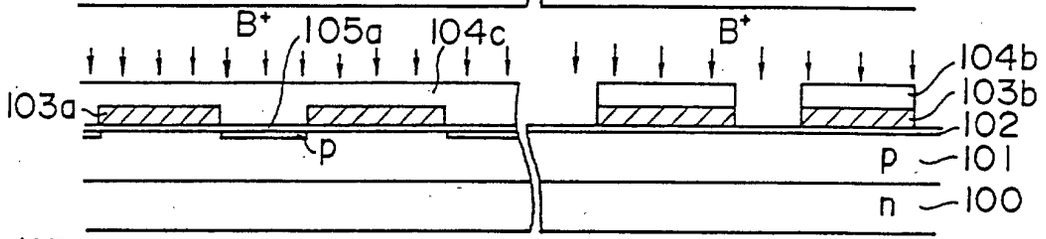


FIG.1D

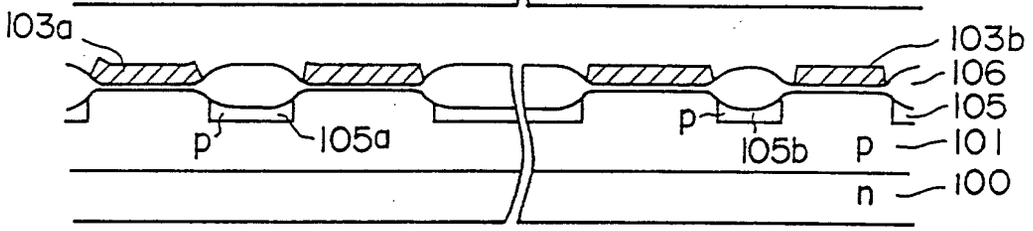


FIG.1E

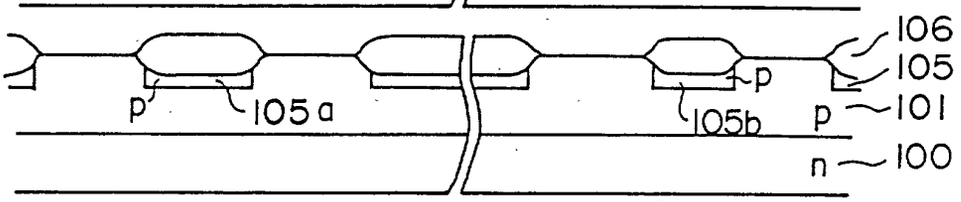


FIG.1F

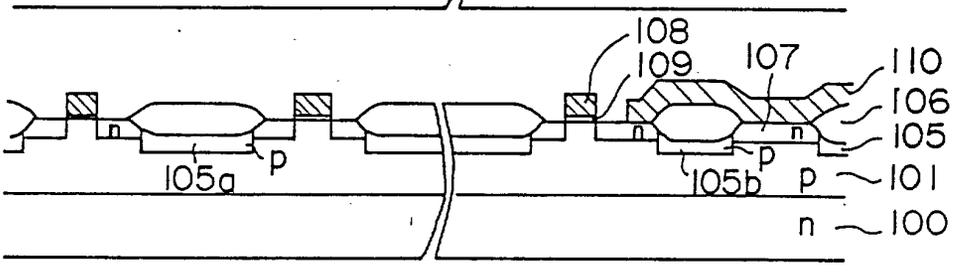


FIG.2A

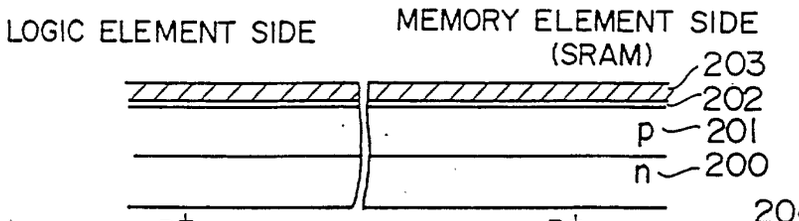


FIG.2B

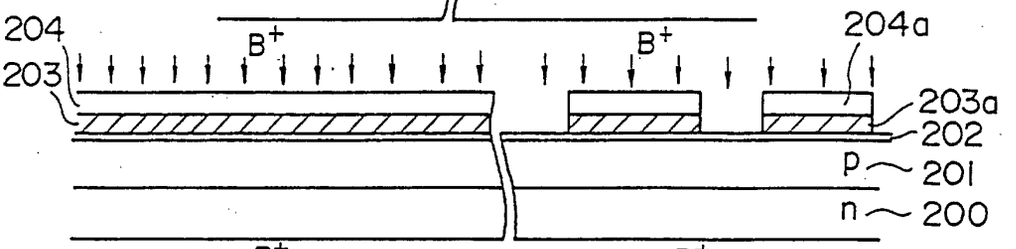


FIG.2C

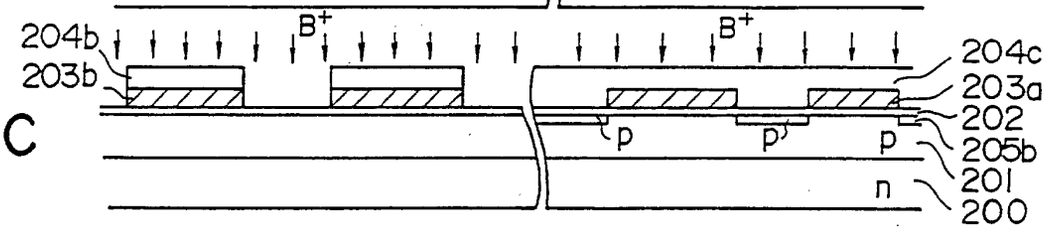


FIG.2D

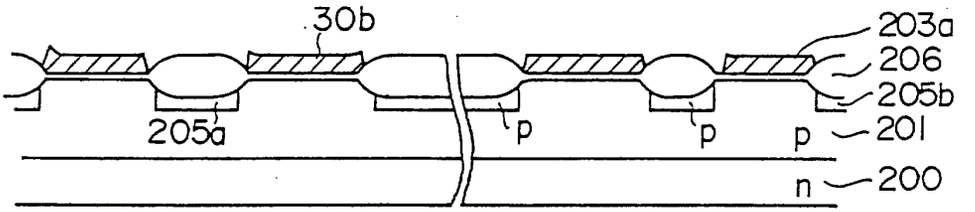


FIG.2E

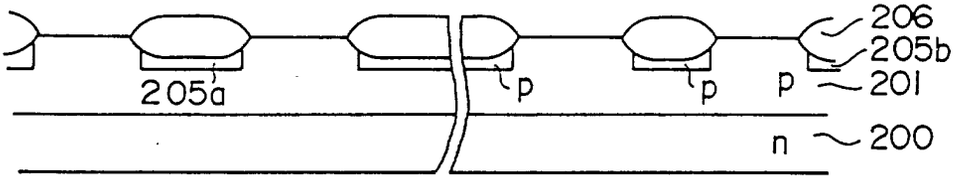


FIG.2F

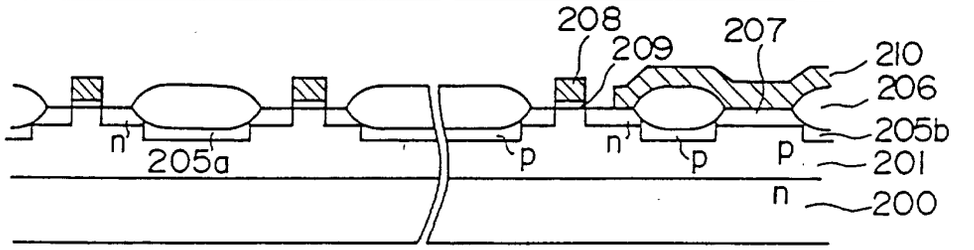


FIG.3A

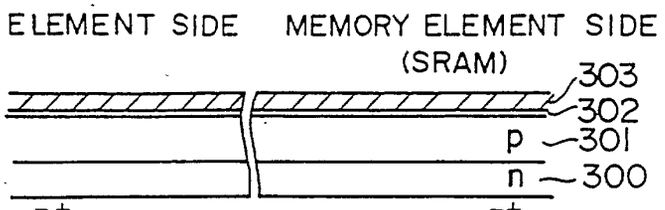


FIG.3B

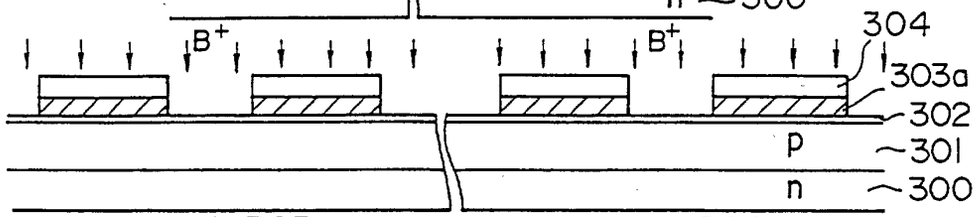


FIG.3C

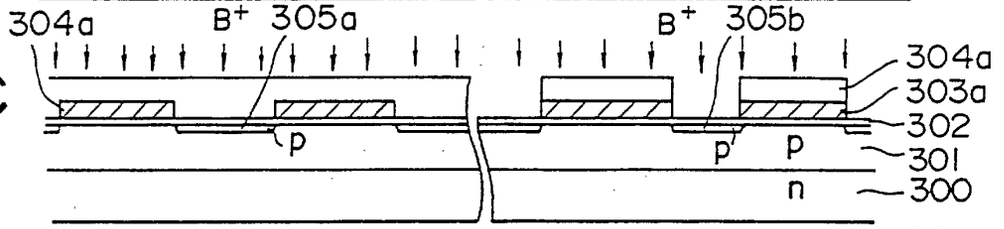


FIG.3D

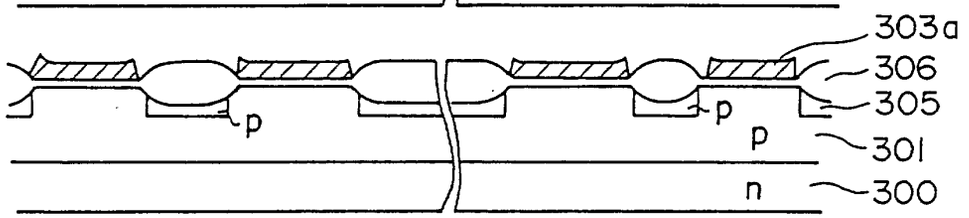


FIG.3E

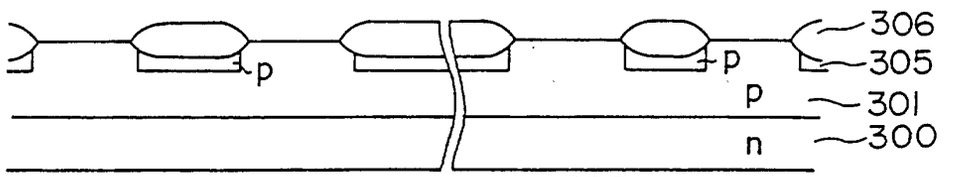
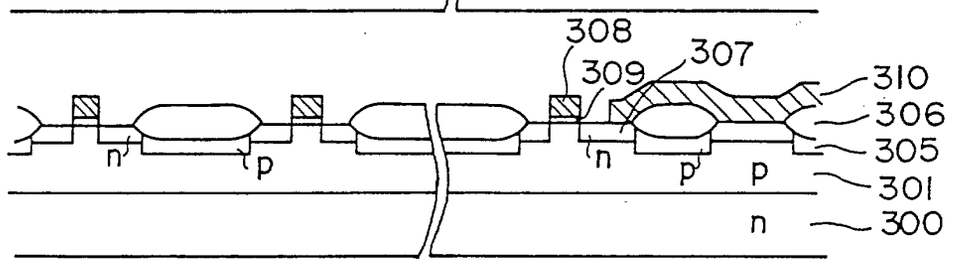


FIG.3F



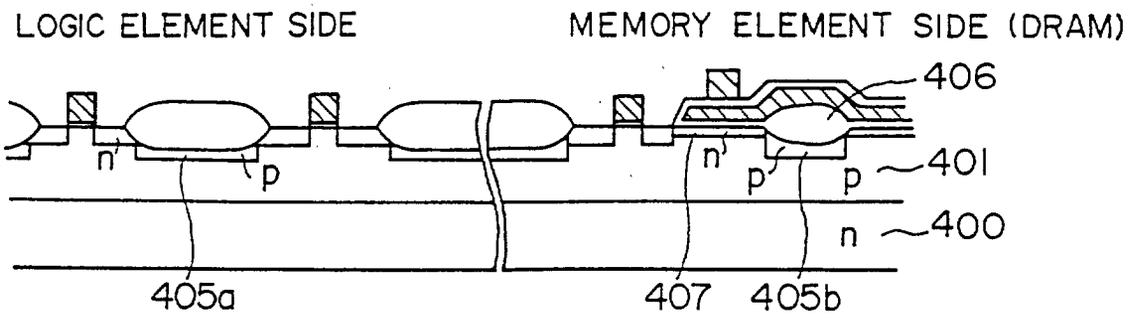

LOGIC ELEMENT SIDE
MEMORY ELEMENT SIDE (DRAM)
406
n'
p
n'
p'
p
401
n
400
405a
407
405b

FIG. 4

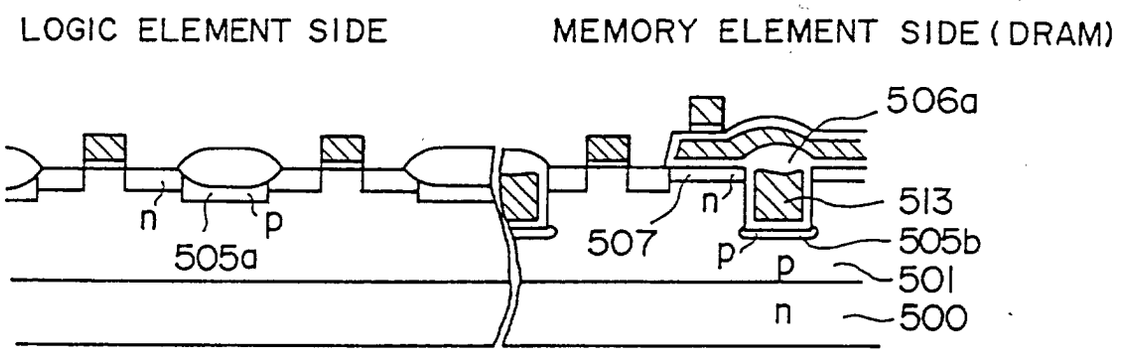

LOGIC ELEMENT SIDE
MEMORY ELEMENT SIDE (DRAM)
506a
n
p
505a
507
n'
513
p'
505b
p
501
n
500

FIG. 5

FIG.6A

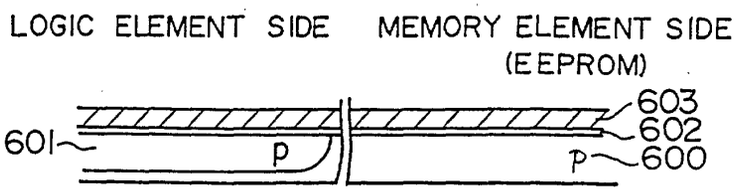


FIG.6B

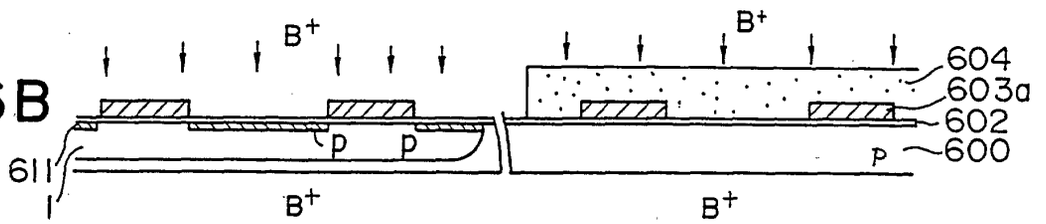


FIG.6C

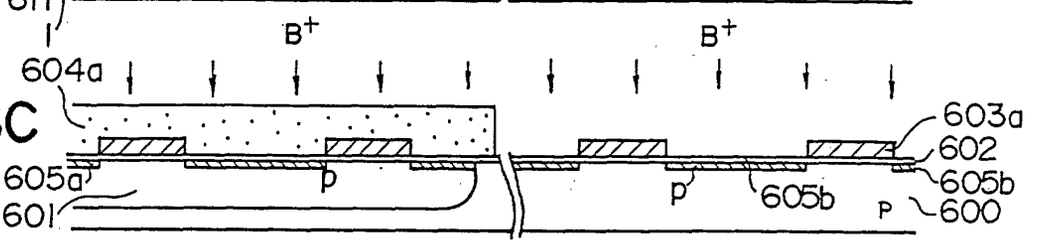


FIG.6D

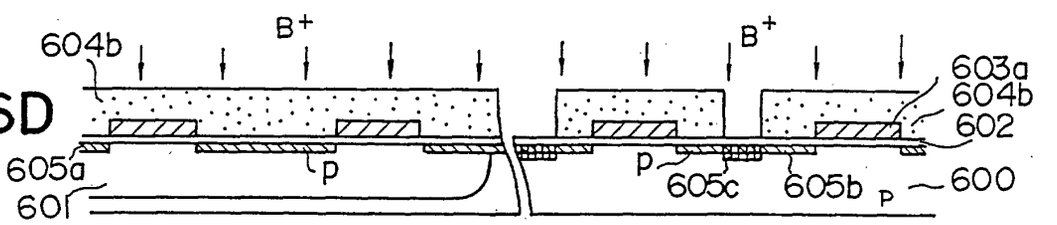


FIG.6E

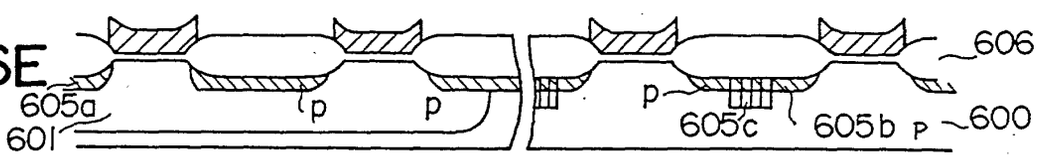
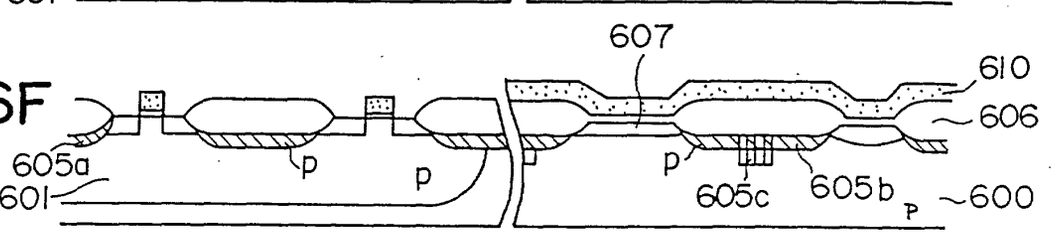


FIG.6F



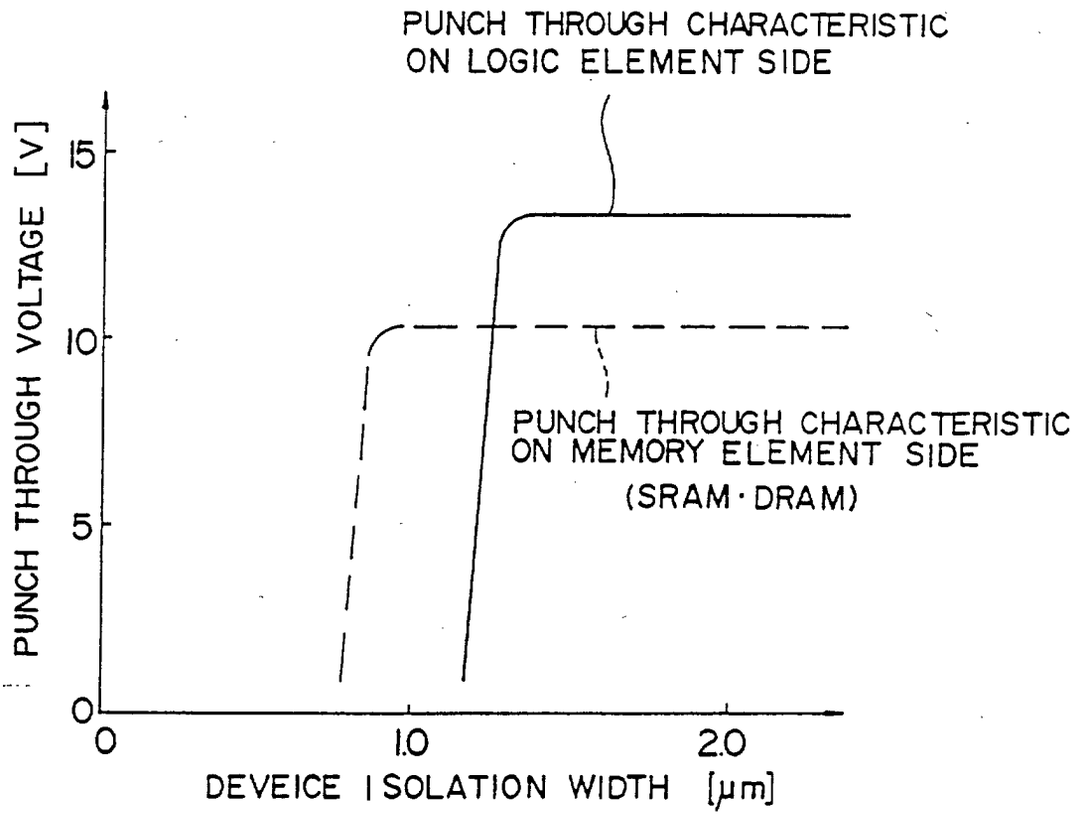

PUNCH THROUGH CHARACTERISTIC
ON LOGIC ELEMENT SIDE
PUNCH THROUGH VOLTAGE [V]
15
10
5
0
PUNCH THROUGH CHARACTERISTIC
ON MEMORY ELEMENT SIDE
(SRAM · DRAM)
0
1.0
2.0
DEVEICE ISOLATION WIDTH [μm]

FIG. 7

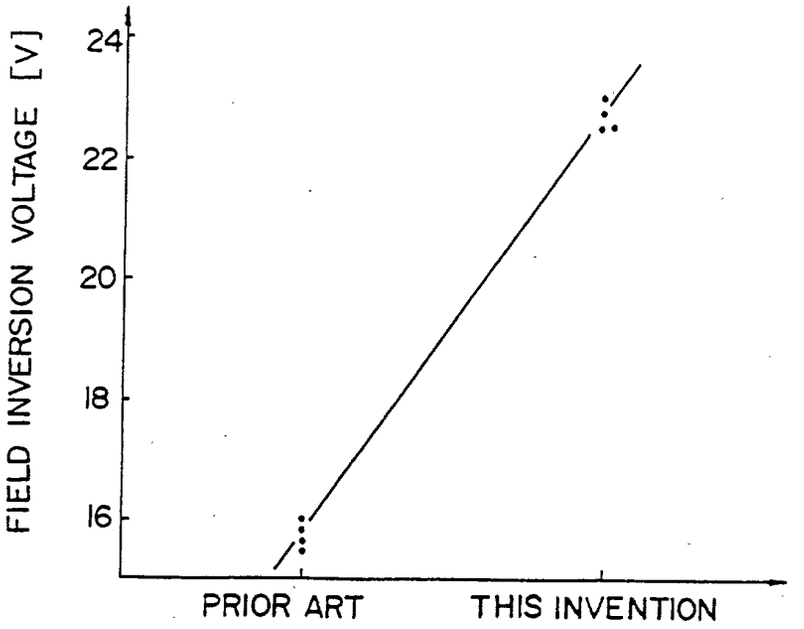

FIELD INVERSION VOLTAGE [V]
24
22
20
18
16
PRIOR ART
THIS INVENTION
IMPURITY CONCENTRATION (FIELD INVERSION
ATOMS / cm3
PREVENTIVE LAYER
605c OF FIG. 6F)

FIG. 8

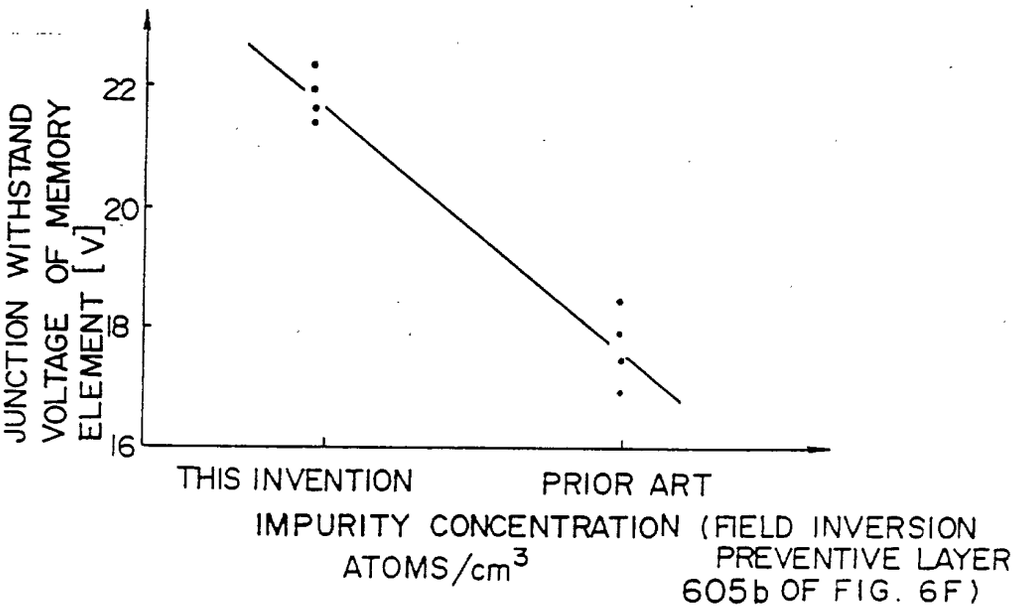

JUNCTION WITHSTAND VOLTAGE OF MEMORY ELEMENT [V]
22
20
18
16
THIS INVENTION
PRIOR ART
IMPURITY CONCENTRATION (FIELD INVERSION
ATOMS/cm3
PREVENTIVE LAYER
605b OF FIG. 6F)

FIG. 9