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(71) Applicant: **SHARP KABUSHIKI KAISHA**
22-22 Nagaike-cho Abeno-ku
Osaka 545(JP)

(72) Inventor: Kanatani, Yoshiharu
1-1896-8, Gakuen-asahi-moto-machi
Nara-shi, Nara-ken(JP)
Inventor: Fukuoka, Hirofumi
2-14-18, Yamanouchi, Sumiyoshi-ku
Osaka-shi, Osaka(JP)

(74) Representative: **Huntingford, David Ian et al**
W.P. THOMPSON & CO. Coopers Building
Church Street
Liverpool L1 3AB(GB)

(54) **A drive circuit for driving an LCD apparatus.**

(57) A drive device for driving a display apparatus having a display unit which includes a plurality of signal electrodes arranged in juxtaposition is disclosed. The drive device comprises: a signal electrode drive circuit for amplitude-modulating an input digital video signal by performing digital-analog conversion, and supplying the resulting analog signal to one of the signal electrodes; a memory for storing the input digital video signal; a pulsewidth conversion circuit for converting the stored digital video signal into a pulse signal, the width of the pulse signal corresponding to the information contained in the stored digital video signal; a pulsewidth-amplitude conversion circuit for converting the pulse signal into an analog signal the amplitude of which corresponds to the pulsewidth of the pulse signal; and an output circuit for supplying a drive signal to one of the signal electrodes, in accordance with the analog signal.

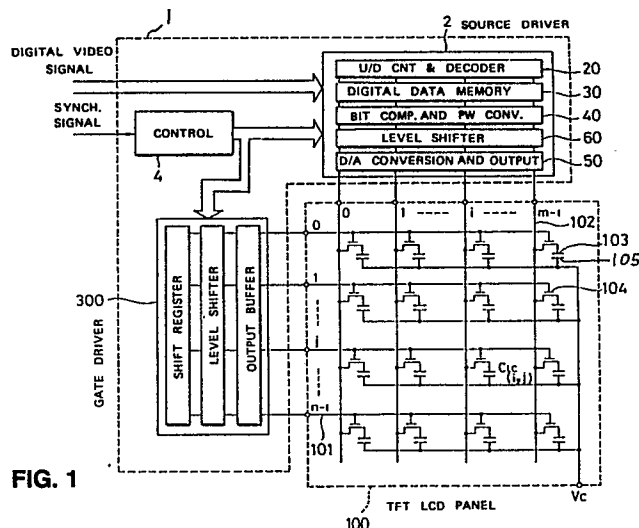


FIG. 1

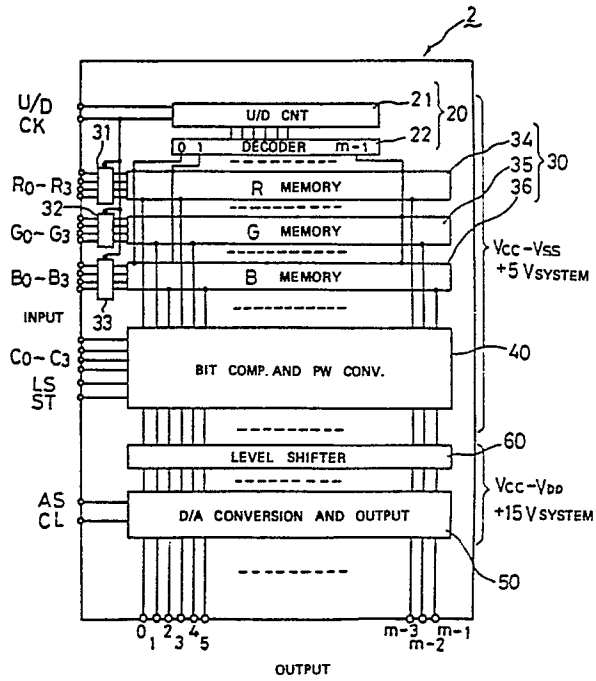


FIG. 2

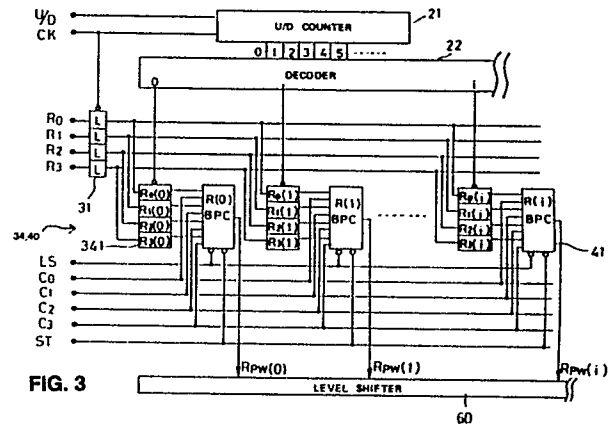


FIG. 3

A DRIVE CIRCUIT FOR DRIVING AN LCD APPARATUS

This invention relates to a drive device for driving a display apparatus and a display apparatus, and more particularly to a drive device for a display apparatus which is capable of gray-scale display by means of amplitude modulation and also to a display apparatus which is capable of gray-scale display by means of amplitude modulation. In this specification, a display apparatus using a matrix-type liquid crystal display unit will be described as a typical example of a display apparatus, but this invention can also be applied to drive circuits for other types of display apparatuses such as electroluminescent (EL) display apparatus and plasma display apparatus, and to such display apparatuses.

Figure 15 shows a matrix liquid crystal display apparatus of the prior art. The matrix liquid crystal display of Figure 15 employs a TFT liquid crystal panel 100 comprising thin-film transistors (TFT) as the switching elements for driving pixel electrodes 103. The TFT liquid crystal panel 100 further comprises n (numbered from 0 to $n-1$) scanning electrodes 101 positioned parallel to each other and m (numbered from 0 to $m-1$) signal electrodes 102 positioned parallel to each other and perpendicularly intersecting the scanning electrodes 101. TFTs 104 for driving the pixel electrodes 103 are located in the vicinity of the intersections of the scanning electrodes 101 and the signal electrodes 102. One horizontal scanning line is composed of m pixel electrodes 103 arranged in a row. Counter electrodes 105 which are respectively opposite to the pixel electrodes 103 are formed. A plurality of counter electrodes are shown in Figure 15, but actually they are consist of one conductive layer formed in common to all of the pixel electrodes 103. A fixed voltage v_c is impressed on the counter electrodes 105.

The TFT liquid crystal panel 100 is driven by a drive device containing a source driver 200 and gate driver 300. The source driver 200 and gate driver 300 are connected to the signal electrodes 102 and the scanning electrodes 101, respectively, of the TFT liquid crystal panel 100. The source driver 200 samples an input analog video signal or video signal, and holds it. The held signal is supplied to the signal electrodes 102. The gate driver 300 outputs scanning pulses to the scanning electrodes 101 in sequence. The timing signal and other signals input to the gate driver 300 and source driver 200 are supplied from a control circuit 400.

With reference to Figure 16, the source driver 200 will be described in more detail. The source driver 200 comprises a shift register 210, sample and hold circuits 220 and output buffers 230. In the shift register 210, shift pulses input from the control circuit 400 are shifted in accordance with the shift clock, and sampling pulses are output sequentially to lines $B_1, B_2, \dots, B_i, \dots, B_m$. In conjunction with this, analog switches $ASW1(1), \dots, ASW1(i), \dots, ASW1(m)$ become closed in sequence, and sampling capacitors 221 are charged in sequence up to the instantaneous amplitude $v(i, j)$ of the input analog video signal. Here, $v(i, j)$ is the instantaneous amplitude of an analog video signal to be written to the pixel electrode 103 corresponding to the intersection of the i th signal electrode and j th scanning electrode of the TFT liquid crystal panel 100. In this way, after video signals of one horizontal scanning period are sampled by the sample and hold circuit 220, an output pulse OE is input, and the video signals are transferred from the sampling capacitors 221 to the holding capacitors 222. The video signal held by the holding capacitors 222 are output to the signal electrodes 102 via the output buffers 230.

Figure 17 diagrammatically shows waveforms of the input and output signals in the source driver 200. In Figure 17, $v(C_{SPL}(i))$, $v(C_H(i))$ and $v_S(i)$ denote the voltage of the i th sampling capacitor 221, the voltage of the i th holding capacitor 222 and the output voltage of the i th output buffer 230, respectively.

The so-called "analog video signal sampling method" drive circuits described above present the following problems (1) to (4) when attempts are made to increase the size or improve the resolution of a display panel such as the above-mentioned TFT liquid crystal panel 100.

(1) In a drive device which samples the amplitude of an analog video signal, the accuracy in the amplitude $v(i, j)$ of a sampled video signal is determined by the time constant established by the on-resistance R_{ON} of the closed analog switch $ASW1(i)$ and the capacitance C_{SPL} of the sampling capacitor 221. Hence, the above-mentioned time constant must be selected so that the frequency band of the video signal is not narrowed by the sampling. More specifically, assuming the frequency at which the signal level drops by 3 dB is expressed as $f(-3 \text{ dB})$ Hz in the frequency characteristic of the input analog video signal, then the condition in the following equation must be satisfied.

0.35

$$\frac{2.2 \times R_{ON} \times C_{SPL}}{f(-3 \text{ dB})}$$

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As the capacity and resolution of display panels (TFT liquid crystal panel 100) are increased, the frequency band becomes wider, which requires faster sampling, so a low R_{ON} and small C_{SPL} are required to satisfy the equation above.

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The charges in the sampling capacitors 221 are distributed to the holding capacitors 222 by the output pulse OE, and the voltage of the holding capacitor 222 of the capacitance C_H becomes as follows.

$$\begin{aligned}
 v(C_H(i)) &= v(i, j) \frac{C_{SPL}(i)}{C_{SPL}(i) + C_H(i)} \\
 &= v(i, j) \frac{1}{1 + \frac{C_H(i)}{C_{SPL}(i)}} \\
 &< v(i, j)
 \end{aligned}$$

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When $C_H(i) \ll C_{SPL}(i)$, therefore, $v(C_H(i))$ is approximately equal to $v(i, j)$. It can be seen that there is a limit to the minimization of the capacitance C_{SPL} in order to minimize amplitude attenuation due to charge distribution from the sampling capacitors 221 to the holding capacitors 222. Further, in order to suppress deterioration or irregularity of the input/output linearity due to dispersion during production in the on-resistance R_{ON} as well as in the capacitance C_{SPL} and C_H , the capacitance C_{SPL} cannot be made very small. As this indicates, there is a limit to the minimization of the capacitance of the sampling capacitors 221, so it is difficult to greatly widen the frequency band of the input video signal. This problem becomes an obstacle to increasing the capacity of a display panel.

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(2) Analog video signals are supplied to the source driver 200 via the bus line as shown in Figure 16, and as the capacity and resolution of a display panel are increased, the frequency band of the video signal becomes wider and the distribution capacity of the bus line increases. This results in the necessity of a wideband amplifier in the circuit supplying video signals, and increases the cost of production.

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(3) When bus lines for supplying multiple analog video signals are arranged in a color display apparatus in which RGB video signals are used, as the capacity and resolution of the display panel are increased, the above-mentioned wideband amplifier is required to have extremely high signal quality in that there can be no phase differences between the multiple video signals and no dispersion in the amplitude characteristics or frequency characteristics.

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(4) Unlike the displaying in a CRT, in drive circuits for matrix display devices, analog video signals are sampled according to a clock signal and displayed in pixels arranged in a matrix. Because delays in the drive device including delays in the bus lines cannot be avoided, it is extremely difficult to accurately establish the sampling position for the analog video signals. Particularly, when displaying on a matrix display apparatus a computer graphic image in which the relationship between video signals and pixel addresses is clearly defined, though in theory it should be possible to perfectly reproduce computer-generated images on the display panel, shift in the image display position, bleeding of the image, etc., due to delays in the drive system and deterioration of the frequency characteristics cannot be avoided in drive circuits using an analog video signal sampling method of the prior art.

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It is an object of the present invention to provide a display apparatus which overcomes the above-discussed and other disadvantages and deficiencies of the prior art.

In accordance with the present invention, there is provided a drive device for driving a display apparatus having a display unit which includes a plurality of signal electrodes arranged in juxtaposition, the

drive device comprising a signal electrode drive means for amplitude-modulating an input digital video signal by performing digital-analog conversion, and for supplying the resulting analog signal to one of said signal electrodes

In a preferred embodiment, the signal electrode drive means comprises a memory means for storing said input digital video signal; a pulsewidth conversion means for converting said digital video signal which is stored in said memory means, into a pulse signal, the width of said pulse signal corresponding to the information contained in said stored digital video signal, a pulsewidth-amplitude conversion means for converting said pulse signal into an analog signal, the amplitude of said analog signal corresponding to the pulsewidth of said pulse signal; and an output circuit for supplying a drive signal to said one of said signal electrodes, in accordance with said analog signal.

In a preferred embodiment, the output circuit comprises a capacitance for holding said analog signal.

In a preferred embodiment, the memory means stores a plurality of input digital video signals which are required for one horizontal scan.

According to a second aspect of the invention, a display apparatus comprises pixel electrodes arranged in matrix; a plurality of signal electrodes arranged in juxtaposition; and a drive device for outputting drive signals for driving said pixel electrodes through said signal electrodes. The drive device comprises: a signal electrode drive means for amplitude-modulating an input digital video signal by performing digital-analog conversion, and supplying the resulting analog signal to one of said signal electrodes; and a holding means for holding said analog signal, said holding means being at the output portion of said drive device.

In a preferred embodiment, the holding means is a capacitance formed between one of said signal electrodes and a counter electrode which opposes said pixel electrodes.

In a preferred embodiment, the signal electrode drive means further comprises; a memory means for storing said digital video signal; a pulsewidth conversion means for converting said digital video signal which is stored in said memory means, into a pulse signal, the width of said pulse signal corresponding to the information contained in said stored digital video signal; a pulsewidth-amplitude conversion means for converting said pulse signal into an analog signal, the amplitude of said analog signal corresponding to the pulsewidth of said pulse signal; and an output circuit for supplying a drive signal to said one of said signal electrodes, in accordance with said analog signal.

In a preferred embodiment, the memory means stores the plurality of input digital video signals which are required for one horizontal scan.

Thus, the invention described herein makes possible the provision of:

- (1) a drive device for a display apparatus in which deterioration of the frequency characteristics of video signals due to the sampling time constant can be avoided;
- (2) a drive device for a display apparatus in which amplitude attenuation due to the charge distribution between sampling capacitors and holding capacitors does not occur;
- (3) a drive device for a display apparatus in which delay in time due to the dispersion of circuits constants of circuit elements does not occur;
- (4) a drive device for a display apparatus in which processes are mainly conducted on digital signals, thereby enabling operations of various portions to be thoroughly synchronized;
- (5) a drive device for a display apparatus in which positional shift and bleeding of an image due to signal delay can be suppressed, thus greatly improving the accuracy and quality of display;
- (6) a drive device for a display apparatus in which can be produced at a low cost;
- (7) a display apparatus in which deterioration of the frequency characteristics of video signals due to the sampling time constant can be avoided;
- (8) a display apparatus in which amplitude attenuation due to the charge distribution between sampling capacitors and holding capacitors does not occur;
- (9) a display apparatus in which delay in time due to the dispersion of circuits constants of circuit elements does not occur;
- (10) a display apparatus in which processes are mainly conducted on digital signals, thereby enabling operations of various portions to be thoroughly synchronized;
- (11) a display apparatus in which positional shift and bleeding of an image due to signal delay can be suppressed, thus greatly improving the accuracy and quality of display;
- (12) a display apparatus which can be produced at a low cost;
- (13) a display apparatus in which the drive device does not require hold capacitors or output buffers;
- and
- (14) a display apparatus in which the deterioration of the display quality due to uneven offset values of output buffers can be eliminated.

The invention is described further hereinafter, by way of example only, with reference to the accom-

panying drawings, in which:

Figure 1 is a block diagram of a matrix-type liquid crystal display apparatus in which a drive device of the invention is used.

Figure 2 is a block diagram of a source driver of the device shown in Figure 1.

5 Figure 3 illustrates essential portions of a digital data memory and a bit comparison and pulsewidth conversion circuit of the device shown in Figure 1.

Figure 4 is a circuit diagram of a BPC circuit of the device shown in Figure 1.

Figure 5 illustrates essential portions of a D/A conversion and output circuit of the device shown in Figure 1.

10 Figure 6 is a timing chart showing the operation of the BPC circuit and the D/A conversion and output circuit of the device shown in Figure 1.

Figure 7 is a timing chart showing the display drive operation of the source driver of Figure 2.

Figure 8 is a block diagram of a matrix-type liquid crystal display apparatus according to the invention.

15 Figure 9 is a block diagram of a source driver of the apparatus of Figure 8.

Figure 10 illustrates essential portions of a digital data memory and a bit comparison and pulsewidth conversion circuit of the apparatus of Figure 8.

Figure 11 is a circuit diagram of a BPC circuit of the apparatus of Figure 8.

Figure 12 illustrates essential portions of a D/A conversion circuit of the apparatus of Figure 8.

20 Figure 13 is a timing chart showing the operation of the BPC circuit and the D/A conversion circuit of the apparatus of Figure 8.

Figure 14 is a timing chart showing the display drive operation of the source driver of Figure 9.

Figure 15 is a block diagram of a matrix-type liquid crystal display apparatus using a prior art drive device.

25 Figure 16 is a circuit diagram of a source driver of the conventional drive device shown in Figure 15.

Figure 17 is a timing chart showing the operation of the source driver of Figure 16.

Figure 1 shows a matrix liquid crystal display apparatus in which a drive device according to the invention is used. The display apparatus of Figure 1 has a TFT liquid crystal panel 100 as a display unit. The TFT liquid crystal panel 100 is driven by a drive device 1 comprising a source driver 2, a gate driver 300, and a control circuit 4. The TFT liquid crystal panel 100 and gate driver 300 have essentially the same configuration as those of the prior art shown in Figure 15, and their detailed description is omitted. The source driver 2 comprises an up-down counter and decoder circuit 20, a digital data memory 30, a bit comparison and pulsewidth conversion circuit 40, a level shifter circuit 60, and a D/A conversion and output circuit 50. The source driver 2 performs digital-analog conversion of input digital video signals, and sends the resulting amplitude-modulated analog signals to the signal electrodes 102 of the TFT liquid crystal panel 100. The various signals required by the source driver 2 are supplied from the control circuit 4.

The source driver 2 is illustrated in more detail in Figure 2. In the source driver 2 of Figure 2 which is designed for performing color display, the RGB video signals are expressed by 4-bit data $R_0 - R_3$, $G_0 - G_3$ and $B_0 - B_3$, respectively. The up-down counter and decoder circuit 20 has an up-down counter 21 and a decoder 22. The up-down counter 21 receives a U/D signal which specifies counting in the direction of increase or in the direction of decrease, and a clock signal CK which actuates the counter operation in the up-down counter 21. The output of the up-down counter 21 is decoded by the decoder 22. The up-down counter and decoder circuit 20 may be composed of shift registers.

The R signals ($R_0 - R_3$), G signals ($G_0 - G_3$) and B signals ($B_0 - B_3$) contained in input digital video signals are latched once by latches 31, 32 and 33, respectively, and, according to the output of the decoder 22, they are then stored in the corresponding memory regions in an R memory 34, a G memory 35 and a B memory 36 which constitute the digital data memory 30. After digital signals covering one horizontal scanning period have been stored in the digital data memory 30, a latch strobe signal LS is input so that the data in the digital data memory 30 are supplied to the bit comparison and pulsewidth conversion circuit 40 over parallel lines. The output of the bit comparison and pulsewidth conversion circuit 40 is supplied to the D/A conversion and output circuit 50 via the level shifter circuit 60.

Figure 3 shows a block diagram of the system which processes the R signals in the R memory 34 and the bit comparison and pulsewidth conversion circuit 40. The R memory 34 comprise memory units 341 which are arranged in a one-to-one correspondence to the signal electrodes 102 of the TFT liquid crystal panel 100. Each memory units 341 have four memory elements $R_0(i) - R_3(i)$ for storing 4-bit video signals. The bit comparison and pulsewidth conversion circuit 40 has bit pulsewidth converter (BPC) circuits 41 which correspond respectively to the memory units 341. Digital video signals stored in the memory units 341 are transferred to the corresponding BPC circuits 41, in response to a latch strobe signal LS from the

control circuit 4. Each BPC circuit 41 receives a start pulse ST and count signals $C_0 - C_3$ from the control circuits 4 in addition to the latch strobe signal LS. In the BPC circuits 41, video signals input from the memory units 341 are converted into pulses the width of which correspond respectively to the information born in the video signals, and the pulses are then supplied to the level shifter circuit 60 as outputs $R_{PW}(i)$. In order to process G and B signals, systems which are substantially the same as that shown in Figure 3 are provided.

The operation of the BPC circuits 41 will be described with reference to Figure 4. The BPC circuits 41 comprises latches $L_0 - L_3$, XOR gates 411, a NAND gate 412, and an RS flip-flop 413. In response to the latch strobe signal LS, the latches $L_0 - L_3$ latch video signals $R_0(i) - R_3(i)$ in 4 bit R signals. Then, the start pulse ST is input to the set terminal of the RS flip-flop 413 to set the flip-flop, thereby making the signal $R_{PW}(i)$ high. The count signals $C_0 - C_3$ gradually increase in the sequence of (0, 0, 0, 0), (0, 0, 0, 1), ..., (1, 1, 1, 1). The XOR gates 411 compare bit by bit the latched video signal ($R_0(i) - R_3(i)$) with the count signals $C_0 - C_3$. When the video signal ($R_0(i) - R_3(i)$) coincides with the count signals $C_0 - C_3$ (i.e., when the four bits of the video signal agree thoroughly with those of the count signals), the output RC(i) of the NAND gate 412 becomes low. The output RC(i) of low level is input to the reset terminal of the RS flip-flop 413 to return the signal $R_{PW}(i)$ to low level. In this way, input video signals are converted into pulses the width of which correspond respectively to the information born in the video signals.

The pulse width of the signal $R_{PW}(i)$ is converted to an amplitude of a voltage signal by the level shifter circuit 60 and the D/A conversion and output circuit 50. For each signal electrode 102 of the TFT liquid crystal panel 100, as shown in Figure 5, the level shifter circuit 60 comprises a level shifter 61, and the D/A conversion and output circuit 50 comprises an analog gate 52, a hold capacitor 53, and an output buffer 54. The level of the signal $R_{PW}(i)$ is converted to the $V_{CC} - V_{DD}$ power supply systems by the level shifter 61. The up-down counter 20, digital data memory 30, and bit comparison and pulsewidth conversion circuit 40 are logic circuits which can operate with the power supplies of $V_{CC} = 5\text{ V}$ and $V_{SS} = 0\text{ V}$. In order to drive the TFT liquid crystal panel 100, however, they generally require a power source voltage which is higher than that used for logic circuits. This is the reason why the above-mentioned level conversion must be performed.

The signal $R_{PW}(i)$ which has been level-shifted is used for operating the analog gate 52. The control circuit 4 supplies to the analog gate 52 a voltage signal AS the level of which increases or decreases stepwise in synchronization with the change of the count signals $C_0 - C_3$ (Figure 6). When the signal $R_{PW}(i)$ is high level, the analog gate 52 is closed so that the voltage of the hold capacitor 53 varies following the change of the voltage signal AS. When the signal $R_{PW}(i)$ becomes low level, the analog gate 52 is opened, thereby fixing the voltage of the hold capacitor 53 to the voltage level which appears at the terminal of the analog gate 52 (i.e., which is the level of the voltage signal AS) immediately before the analog gate 52 becomes opened. The hold capacitor 53 is coupled to the input of the output buffer 54 which then outputs a voltage signal R(i) for driving the signal electrode 102 of the TFT liquid crystal panel 100. The level of the signal R(i) corresponds to that of the hold capacitor 53. Each portions of the level shifter circuit 60 and D/A conversion and output circuits 50 which correspond to the signal electrodes 102 operate in parallel in a similar manner as described above.

Figure 6 illustrates the above operation by showing the waveforms of the voltage signal AS, the count signals $C_0 - C_3$, the start pulse ST, and the signals RC(i), $R_{PW}(i)$ and R(i) which are obtained when the input video signal ($R_0(i) - R_3(i)$) is (0, 1, 1, 1). When the start pulse ST is input, the signal $R_{PW}(i)$ becomes high. When the count signals $C_0 - C_3$ reach (0, 1, 1, 1), the signal $R_{PW}(i)$ returns to the low level, and the output signal R(i) is fixed to the level at this point.

The timing of display drive in the source driver 2 is shown in Figure 7. The relationships between the signal $G_{PW}(i)$ and voltage signal G(i) and the video signals $G_0 - G_3$, and the signal $B_{PW}(i)$ and voltage signal B(i) and the video signals $B_0 - B_3$ are the same as the above-described relationship between the signal $R_{PW}(i)$ and voltage signal R(i) and the video signals $R_0 - R_3$. As seen from Figure 7, the video signal for the jth horizontal scanning line are D/A-converted by utilizing the entire of the (j+1)th horizontal scanning period following the jth horizontal scanning period, and the obtained analog signals are transferred to the signal electrodes 102. Therefore, the process of storing the input video signals into the digital data memory 30 must be done quickly, but D/A conversion can be done at a slower rate.

Further, the TFT liquid crystal panel 100 and other display panels deteriorate more quickly when a DC component is contained in the impressed voltage. In this embodiment, the increase and decrease of the level of the signal AS from which the voltages applied to the liquid crystal panel 100 are generated occur alternately as each horizontal scanning period elapses, in order to prevent deterioration of the display panel.

Figure 8 shows a display apparatus according to the invention. The embodiment shown in Figure 8 is a matrix-type liquid crystal display apparatus comprising a TFT liquid crystal panel 100 as a display unit, and

has a similar configuration as the display apparatus of Figure 1 except that a D/A conversion circuit 55 is provided instead of the D/A conversion and output circuit 50. The configuration of the embodiment will be described regardless of repetition. The TFT liquid crystal panel 100 is driven by a drive device 1 comprising a source driver 2, a gate driver 300 and a control circuit 4. The TFT liquid crystal panel 100 and gate driver 300 have essentially the same configuration as those of the prior art shown in Figure 15. The source driver 2 comprises an up-down counter and decoder circuit 20, a digital data memory 30, a bit comparison and pulsewidth conversion circuit 40, a level shifter circuit 60, and the D/A conversion circuit 55. The various signals required by the source driver 2 are supplied from the control circuit 4.

The source driver 2 is illustrated in more detail in Figure 9. In the source driver 2 of Figure 9 which is designed for performing colour display, the RGB video signals are expressed by 4-bit data $R_0 - R_3$, $G_0 - G_3$ and $B_0 - B_3$, respectively. The up-down counter and decoder circuit 20 has an up-down counter 21 and a decoder 22. The up-down counter 21 receives a U/D signal which specifies counting in the direction of increase or in the direction of decrease, and a clock signal CK which actuates the count operation in the up-down counter 21. The output of the up-down counter 21 is decoded by the decoder 22. The up-down counter and decoder circuit 20 may be composed of shift registers.

The R signals ($R_0 - R_3$), G signals ($G_0 - G_3$) and B signals ($B_0 - B_3$) contained in input digital video signals are latched once by latches 31, 32 and 33, respectively, and, according to the output of the decoder 22, they are then stored in the corresponding memory regions in an R memory 34, a G memory 35 and a B memory 36 which constitute the digital data memory 30. After digital video signals covering one horizontal scanning period have been stored in the digital data memory 30, a latch strobe signal LS is input so that the data in the digital data memory 30 are supplied to the bit comparison and pulsewidth conversion circuit 40 over parallel lines. The output of the bit comparison and pulsewidth conversion circuit 40 is supplied to the D/A conversion circuit 55 via the level shifter circuit 60.

Figure 10 shows a block diagram of the system which processes the R signals in the R memory 34 and the bit comparison and pulsewidth conversion circuit 40. The R memory 34 comprise memory units 341 which are arranged in a one-to-one correspondence to the signal electrodes 102 of the TFT liquid crystal panel 100. Each memory units 341 have four memory elements $R_0(i) - R_3(i)$ for storing 4-bit video signals. The bit comparison and pulsewidth conversion circuit 40 has bit pulsewidth converter (BPC) circuits 41 which correspond respectively to the memory units 341. Digital video signals stored in the memory units 341 are transferred to the corresponding BPC circuits 41, in response to a latch strobe signal LS from the control circuit 4. Each BPC circuit 41 receives a start pulse ST and count signals $C_0 - C_3$ from the control circuits 4 in addition to the latch strobe signal LS. In the BPC circuits 41, video signals input from the memory units 341 are converted into pulses the width of which correspond respectively to the information born in the video signals, and the pulses are then supplied to the level shifter circuit 60 as outputs $R_{PW}(i)$. In order to process G and B signals, systems which are substantially the same as that shown in Figure 10 are provided.

The operation of the BPC circuits 41 will be described with reference to Figure 11. The BPC circuit 41 comprises latches $L_0 - L_3$, XOR gates 411, a NAND gate 412, and an RS flip-flop 413. In response to the latch strobe signal LS, the latches $L_0 - L_3$ latch video signals $R_0(i) - R_3(i)$ in 4-bit R signals. Then, the start pulse ST is input to the set terminal of the RS flip-flop 413 to set the flip-flop, thereby making the signal $R_{PW}(i)$ high. The count signals $C_0 - C_3$ gradually increase in the sequence of (0, 0, 0, 0), (0, 0, 0, 1), ..., (1, 1, 1, 1). The XOR gate 411 compares bit by bit the latched video signal ($R_0(i) - R_3(i)$) with the count signals $C_0 - C_3$. When the video signal ($R_0(i) - R_3(i)$) coincides with the count signals $C_0 - C_3$ (i.e., when the four bits of the video signal agree thoroughly with those of the count signals), the output RC(i) and the NAND gate 412 becomes low. The output RC(i) of low level is input to the reset terminal of the RS flip-flop 413 to return the signal $R_{PW}(i)$ to low level. In this way, input video signals are converted into pulses the width of which correspond respectively to the information born by the video signals.

The pulse width of the signal $R_{PW}(i)$ is converted to an amplitude of a voltage signal by the level shifter circuit 60 and the D/A conversion circuit 55. For each signal electrode 102 of the TFT liquid crystal panel 100, as shown in Figure 12, the level shifter circuit 60 comprises a level shifter 61, and the D/A conversion circuit 55 comprises an analog gate 52. In Figure 12, also shown are the jth scanning electrode 101, the TFT 104, the pixel electrode 103, and the counter electrode 105. The level of the signal $R_{PW}(i)$ is converted to the $V_{CC} - V_{DD}$ power supply systems by the level shifter 61. The up-down counter 20, digital data memory 30, and bit comparison and pulsewidth conversion circuit 40 are logic circuits which can operate with the power supplies of $V_{CC} = 5\text{ V}$ and $V_{SS} = 0\text{ V}$. In order to drive the TFT liquid crystal panel 100, however, they generally require a power source voltage which is higher than that used for logic circuits. This is the reason why the above-mentioned level conversion must be performed.

The signal $R_{PW}(i)$ which has been level-shifted is used for operating the analog gate 52. The control

circuit 4 supplies to the analog gate 52 a voltage signal AS the level of which increases or decreases stepwise in synchronization with the change of the count signals $C_0 - C_3$ (Figure 13). When the signal $R_{PW}(i)$ is high level, the analog gate 52 is closed so that the signal AS is applied to the signal electrode 102, thereby charging or discharging the signal electrode capacitance C_{SL} of the signal electrode 102. When the
 5 signal $R_{PW}(i)$ becomes low level, the analog gate 52 is opened, thereby fixing the voltage of the signal electrode capacitance C_{SL} to the voltage level which appears at the terminal of the analog gate 52 (i.e., which is the level of the voltage signal AS) immediately before the analog gate 52 becomes opened. The signal electrode capacitance C_{SL} consists mainly of: (1) the capacitance between the signal electrode 102 and the counter electrode 105; (2) the capacitance formed at the intersection of the signal electrode 102
 10 and the scanning electrode 101; and (3) the capacitance between the source electrode and gate electrode of the TFT 104. Among these capacitances (1) to (3), the capacitance (1) is the largest one. When the capacitance of one electrode is expressed as $C_{LC}(i,j)$, the following relation can be given.

$$C_{SL} \gg C_{LC}(i,j)$$

Therefore, the following inequality can be established:

$$15 \quad R_{ON} \times C_{LC}(i,j) < R_{SL} \times C_{SL}$$

where R_{ON} is the ON resistance of the TFT 104, and R_{SL} the resistance of the signal electrode 102. As seen from above, the pixel electrode 103 can be driven sufficiently by the charge accumulated in the signal electrode capacitance C_{SL} . Each portions of the level shifter circuit 60 and D/A conversion circuit 55 which correspond to the signal electrodes 102 operate in parallel and in a similar manner as described above.

20 Figure 13 illustrates the above operation by showing the waveforms of the voltage signal AS, the count signals $C_0 - C_3$, the start pulse ST, and the signals $RC(i)$, $R_{PW}(i)$ and $R(i)$ which are obtained when the input video signal ($R_0(i) - R_3(i)$) is (0, 1, 1, 1). When the start pulse ST is input, the signal $R_{PW}(i)$ becomes high. When the count signals $C_0 - C_3$ reach (0, 1, 1, 1), the signal $R_{PW}(i)$ returns to the low level, and the output signal $R(i)$ of the analog gate 52 is fixed to the level at this point.

25 The timing of display drive in the source driver 2 is shown in Figure 14. As seen from Figure 14, the video signal for the j th horizontal scanning line is D/A-converted by utilizing the entire of the $(j+1)$ th horizontal scanning period following the j th horizontal scanning period, and the obtained analog signals are transferred to the signal electrodes 102. Therefore, the process of storing the input video signals into the digital data memory 30 must be done quickly, but D/A conversion can be done at a slower rate.

30 Further, the TFT liquid crystal panel 100 and other display panels deteriorate more quickly when a DC component is contained in the impressed voltage. In the embodiment, the increase and decrease of the level of the signal AS from which the voltages applied to the liquid crystal panel 100 are generated occur alternately as each horizontal scanning period elapses, in order to prevent deterioration of the display panel.

35 According to the invention, improved drive devices for a display apparatus and improved display apparatuses are provided which solve the various problems involved in prior art systems in which the analog video signal sampling method is used.

In the drive device and the display apparatus of this invention, digitized video signals are once stored, and then transferred. Therefore, deterioration of the frequency characteristics of video signals due to the sampling time constant, which is a problem in prior art display systems of the analog video signal sampling
 40 type, can be avoided. Further, amplitude attenuation due to charge distribution between the sampling capacitor and the holding capacitor also does not occur.

In the drive device and the display apparatus of this invention, processes are performed mainly on digital signals, and operation of the various parts in the device can be thoroughly synchronized. Therefore, a shift in the display position of the image and image bleeding due to the delays, etc., occurring in the
 45 circuitry can be suppressed, thus greatly improving the display accuracy and display quality of the image. These advantages are highly effective in a high fidelity display of high-definition image data, so that even computer graphics can be accurately displayed.

The drive device and the display apparatus of this invention can accommodate display panels with increased capacity by basically speeding up the logic circuits constituting the memory circuit which stores
 50 input digital video signals. In one embodiment of the invention, the video signal memory circuit is capable of storing video signals for at least one horizontal scan, so the D/A conversion of the stored digital video signals can be performed relatively slowly by utilizing the next horizontal scanning period. This not only contributes to lowering the cost of the drive device, but it also improves display accuracy.

In the display apparatus of the invention, analog signals which have been obtained by D/A conversion
 55 can be stored by utilizing the capacitances formed by the signal electrodes formed in a display unit, thus eliminating the necessity of providing hold capacitors and output buffers in a drive device. According to the invention, therefore, the production cost of a display apparatus can be reduced, and the deterioration of the display quality due to uneven offset values of output buffers can be eliminated.

It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope of this invention as defined by the appended claims.

5 Claims

1. A drive device for driving a display apparatus having a display unit which includes a plurality of signal electrodes arranged in juxtaposition, said drive device being characterised by a signal electrode drive means for amplitude-modulating an input digital video signal by performing digital-analog conversion, and
 10 supplying the resulting analog signal to one of said signal electrodes.
2. A drive device according to claim 1, wherein said signal electrode drive means comprises;
 a memory means (30) for storing said input digital video signal;
 a pulsewidth conversion means for converting said digital video signal which is stored in said memory means, into a pulse signal, the width of said pulse signal corresponding to the information contained in said
 15 stored digital video signal;
 a pulsewidth-amplitude conversion means for converting said pulse signal into an analog signal, the amplitude of said analog signal corresponding to the pulsewidth of said pulse signal; and
 an output circuit for supplying a drive signal to said one of said signal electrodes, in accordance with said analog signal.
- 20 3. A drive circuit according to claim 2, wherein said output circuit comprises a capacitance for holding said analog signal.
4. A drive device according to claim 2, wherein said memory means stores a plurality of input digital video signals which are required for one horizontal scan.
5. A display apparatus comprising: pixel electrodes arranged in matrix; a plurality of signal electrodes
 25 arranged in juxtaposition; and a drive device for outputting drive signals for driving said pixel electrodes through said signal electrodes,
 said drive device being characterised by:
 a signal electrode drive means for amplitude-modulating an input digital video signal by performing digital-analog conversion, and supplying the resulting analog signal to one of said signal electrodes; and
 30 a holding means for holding said analog signal, said holding means being at the output portion of said drive device.
6. A display apparatus according to claim 5, wherein said holding means is a capacitance formed between one of said signal electrodes and a counter electrode which opposes said pixel electrodes.
7. A display apparatus according to claim 5, wherein said signal electrode drive means further
 35 comprises;
 a memory means for storing said digital video signal;
 a pulsewidth conversion means for converting said digital video signal which is stored in said memory means, into a pulse signal, the width of said pulse signal corresponding to the information contained in said stored digital video signal;
 40 a pulsewidth-amplitude conversion means for converting said pulse signal into an analog signal, the amplitude of said analog signal corresponding to the pulsewidth of said pulse signal; and
 an output circuit for supplying a drive signal to said one of said signal electrodes, in accordance with said analog signal.
8. A display apparatus according to claim 7, wherein said memory means stores the plurality of input
 45 digital video signals which are required for one horizontal scan.

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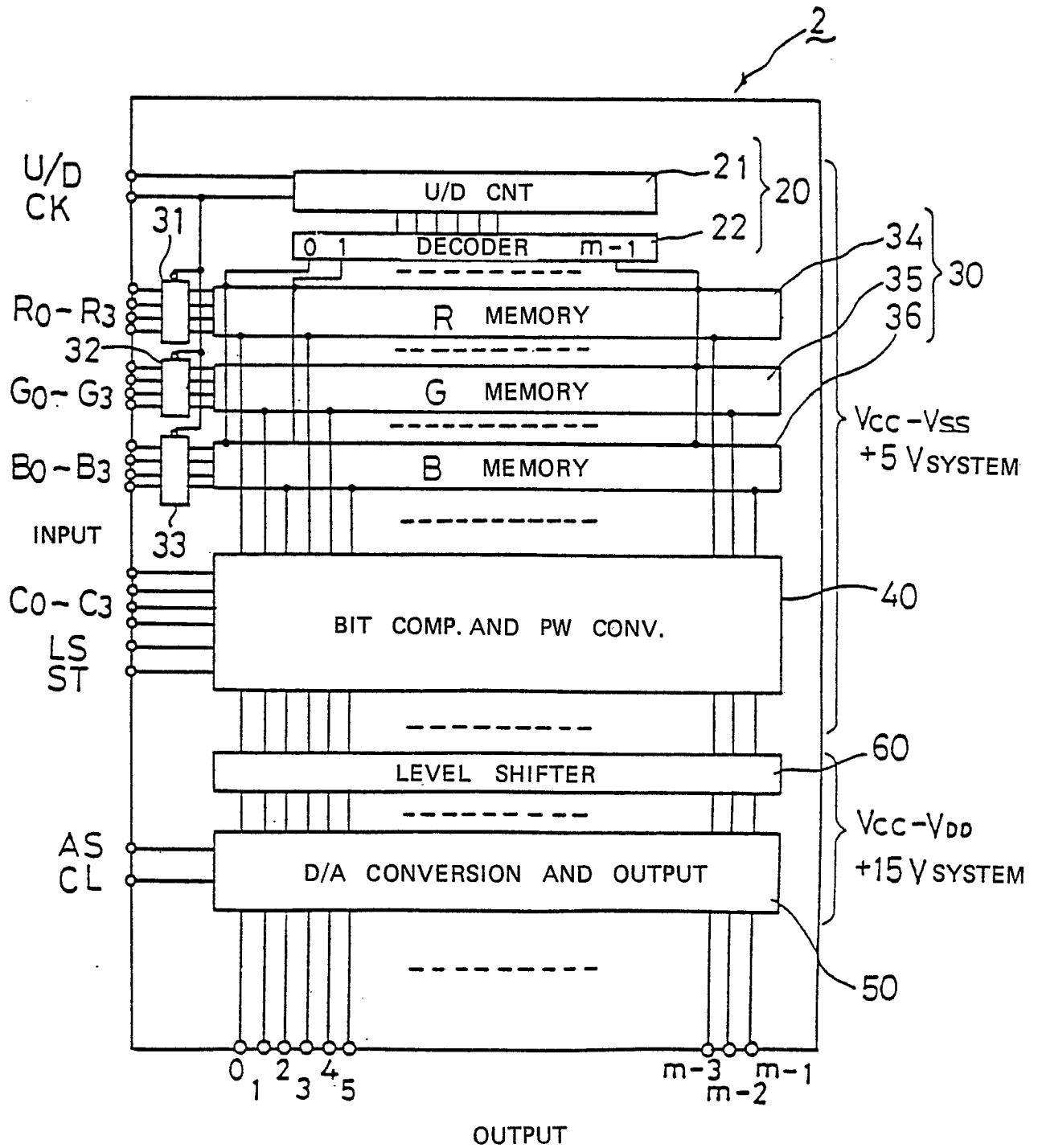
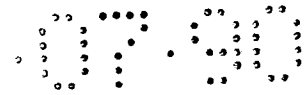


FIG. 2

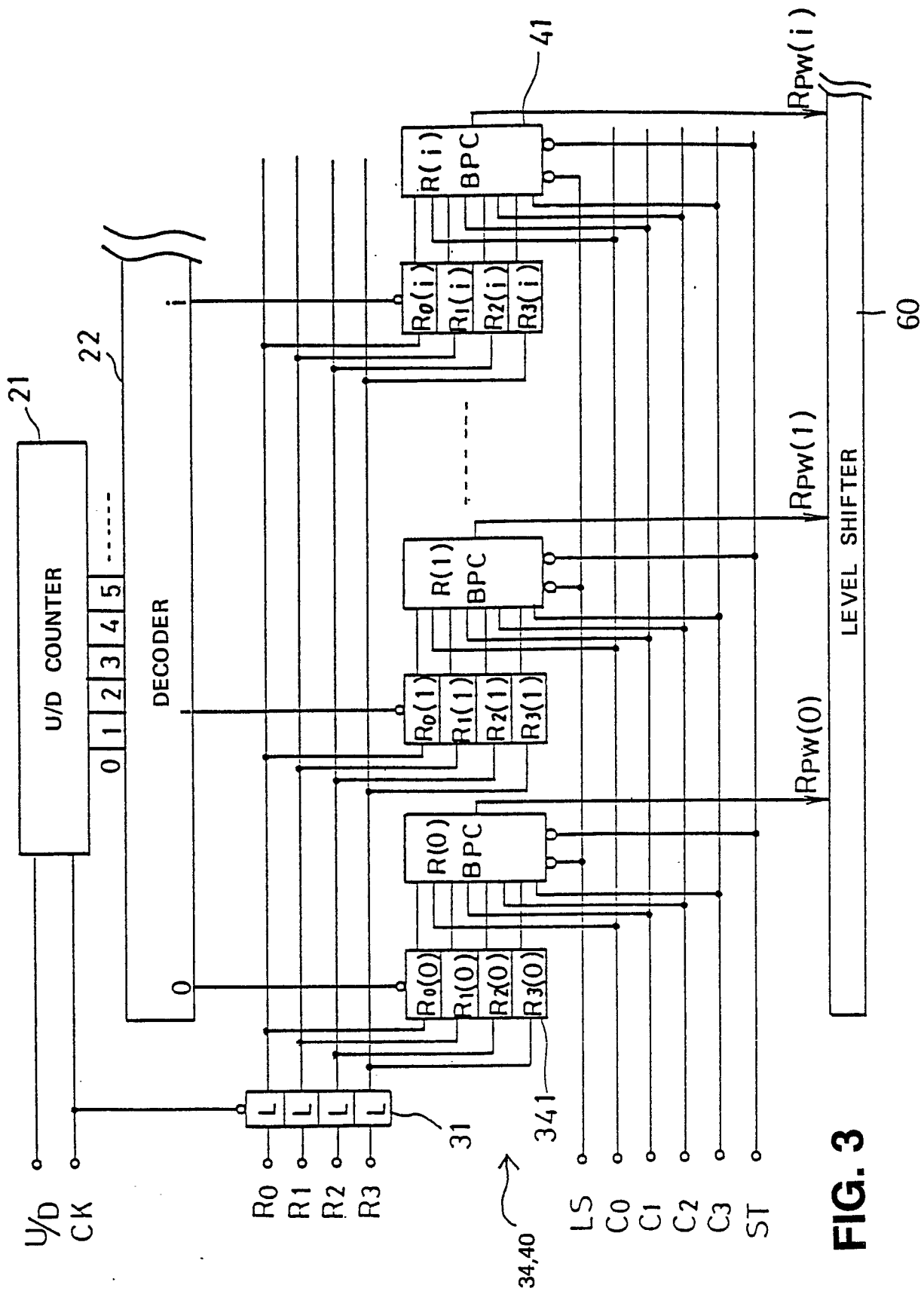
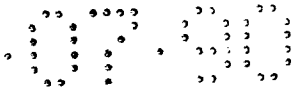
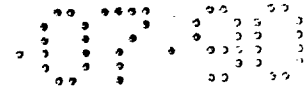
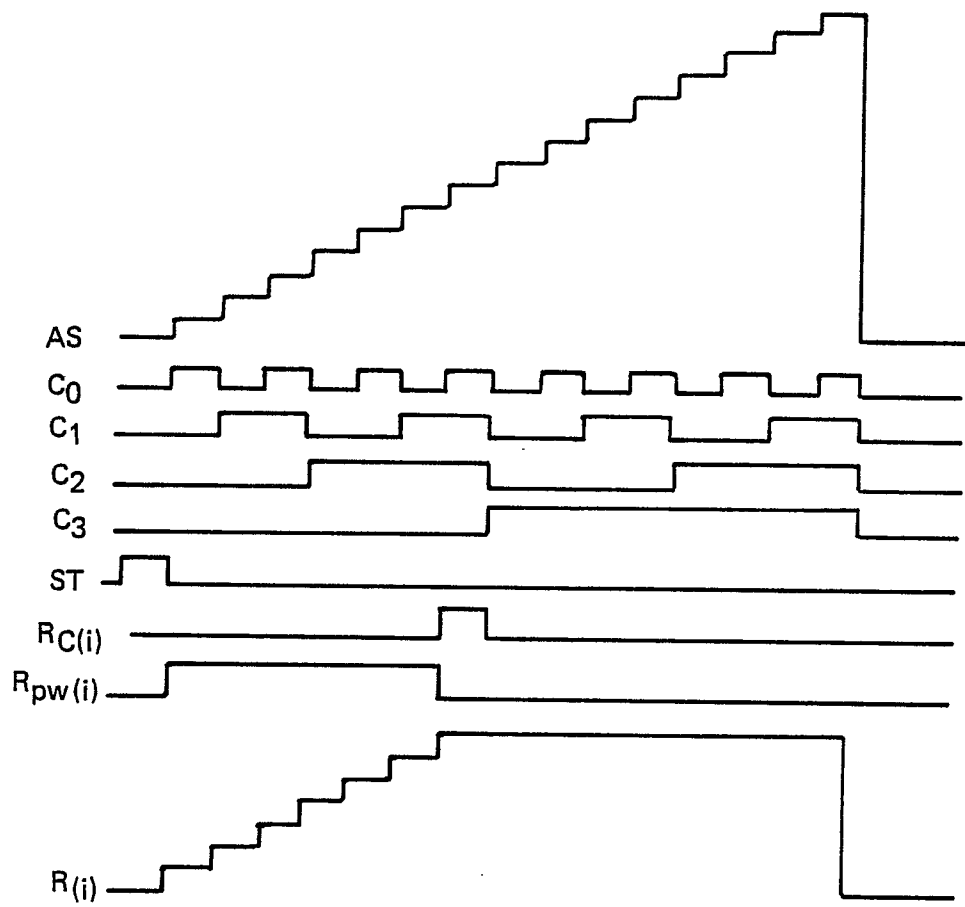
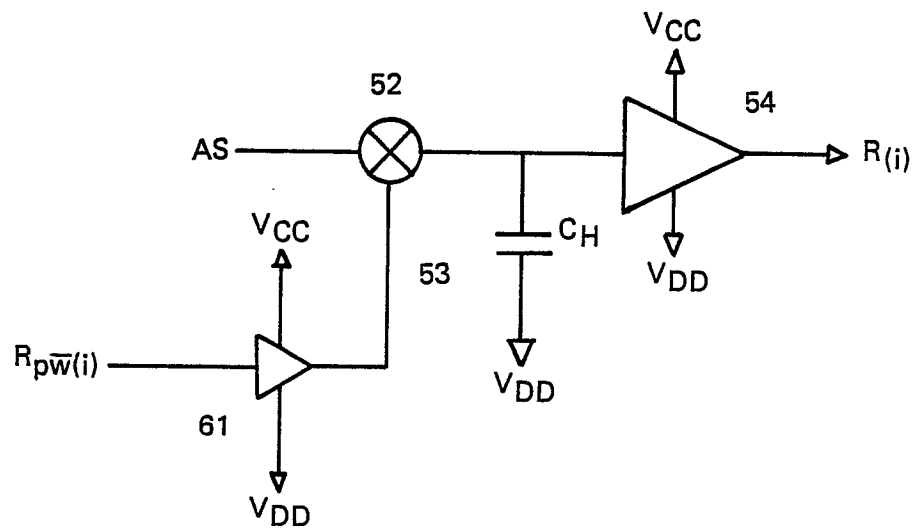


FIG. 3



**FIG. 5****FIG. 6**

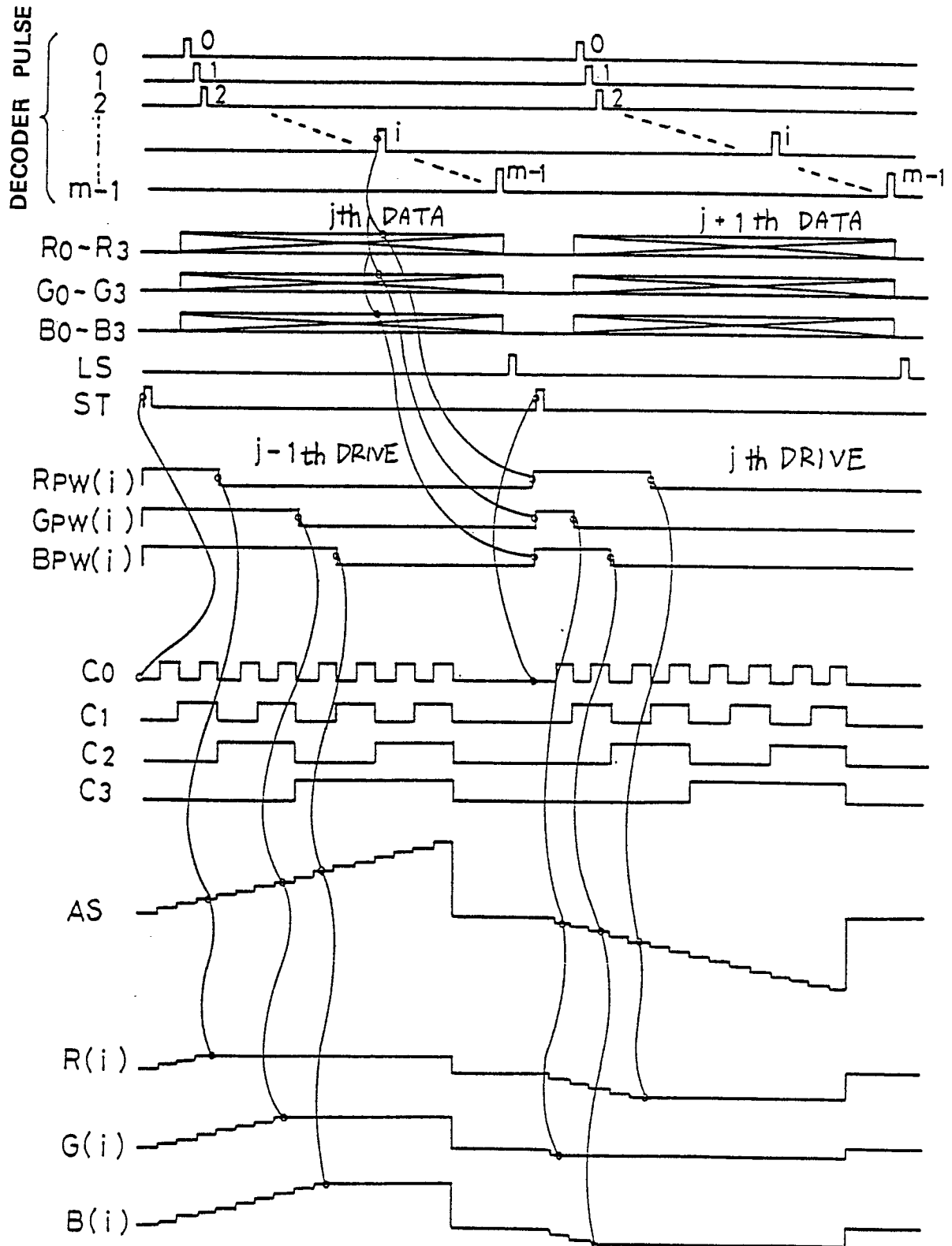


FIG. 7



FIG. 8

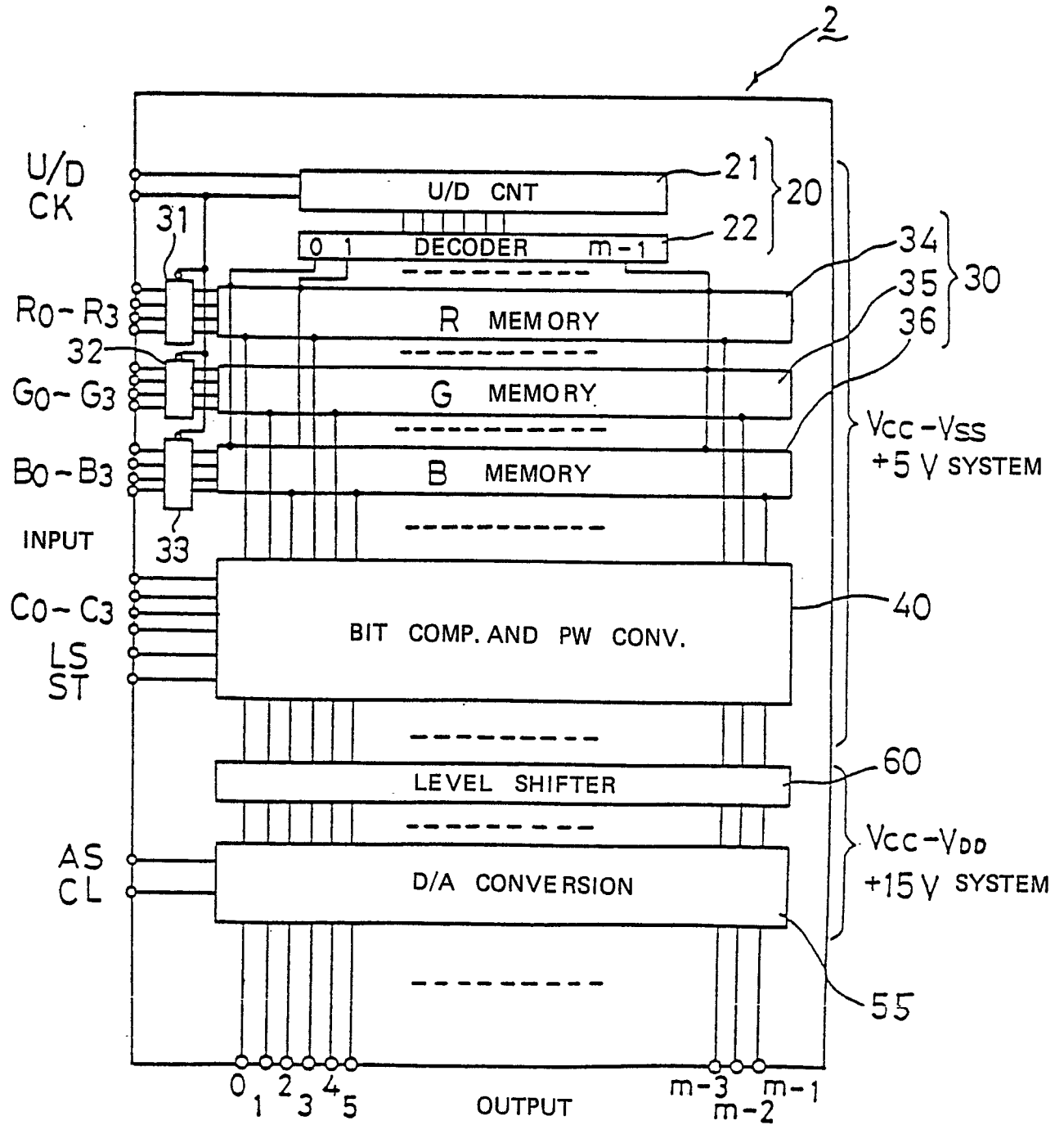
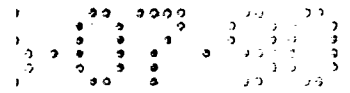


FIG. 9

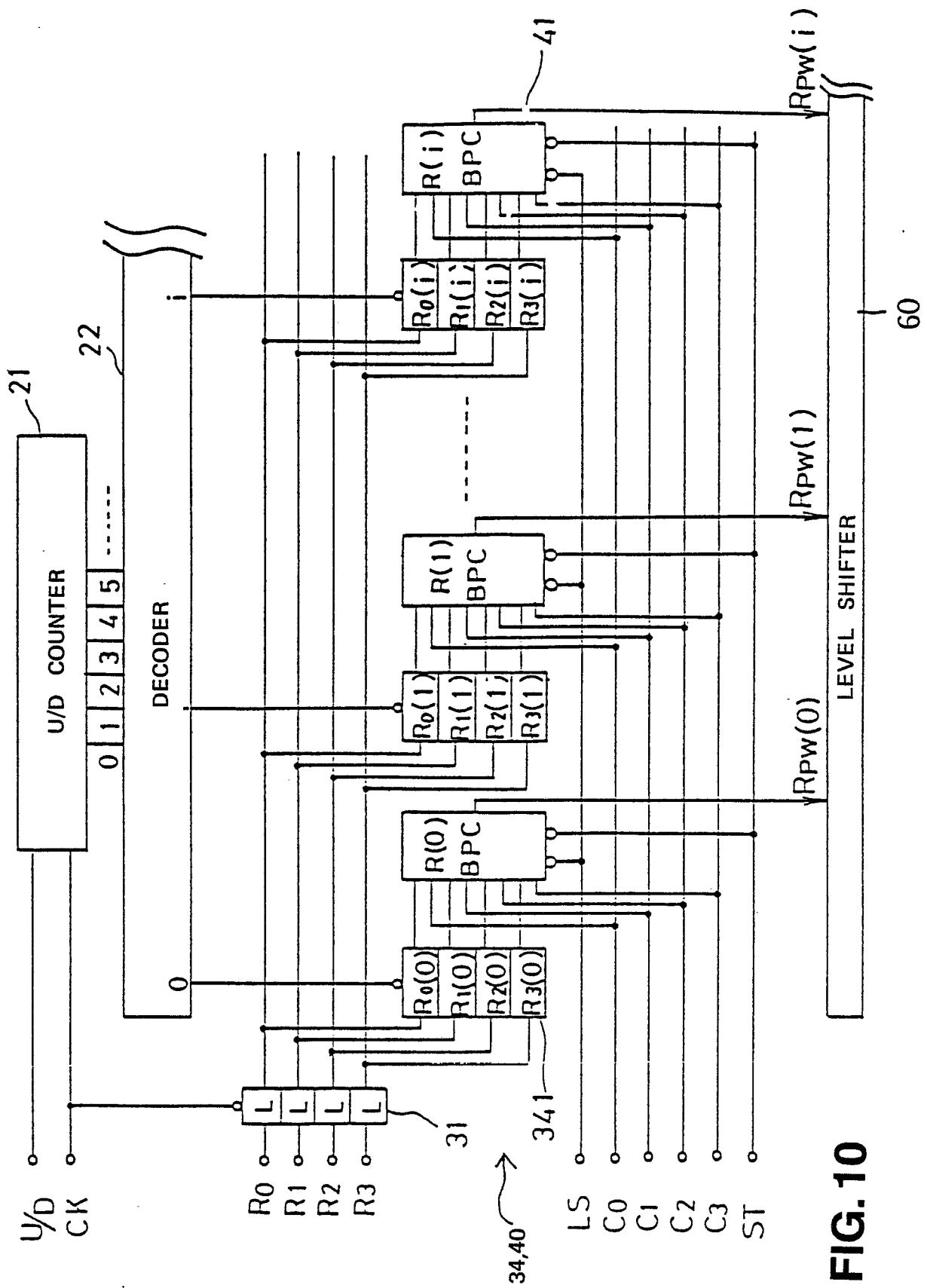


FIG. 10

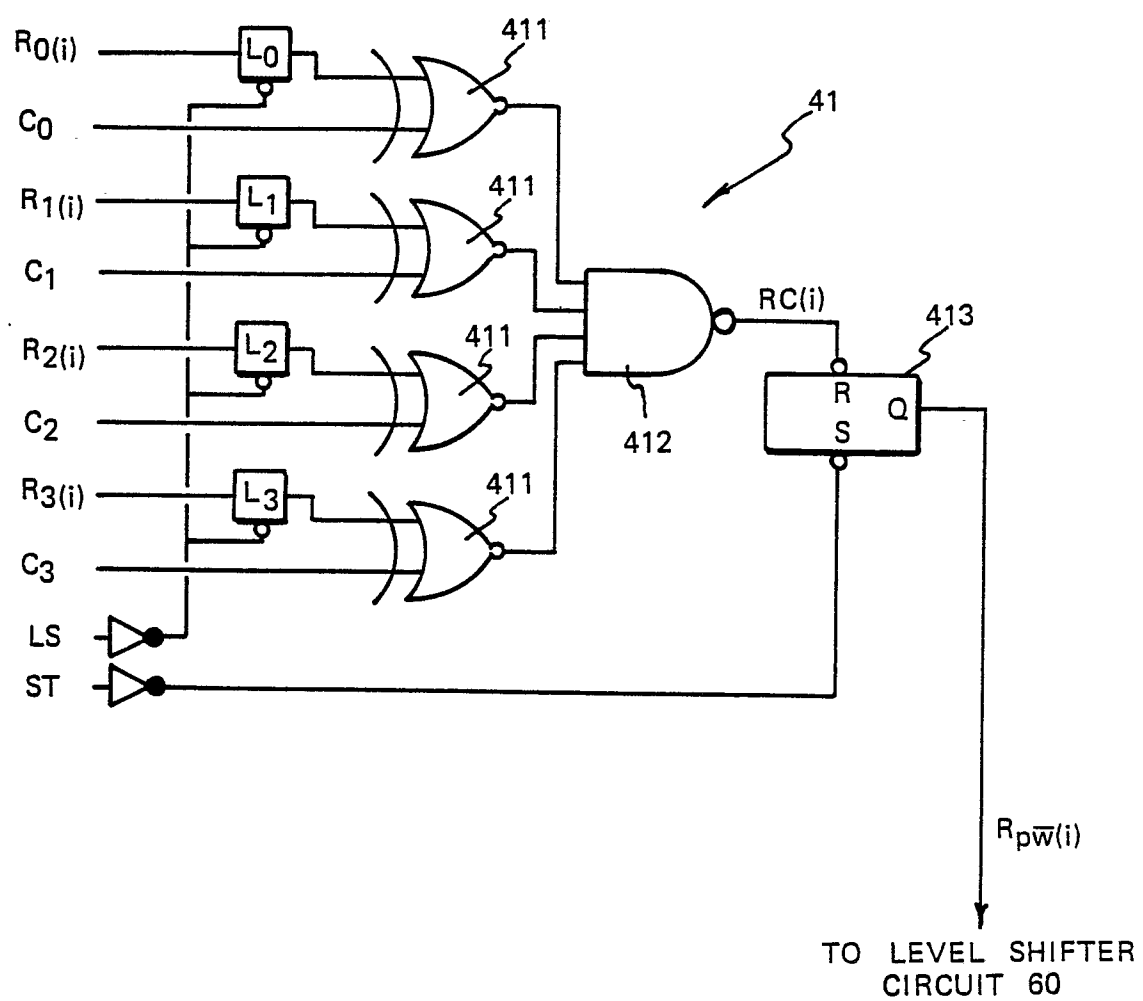
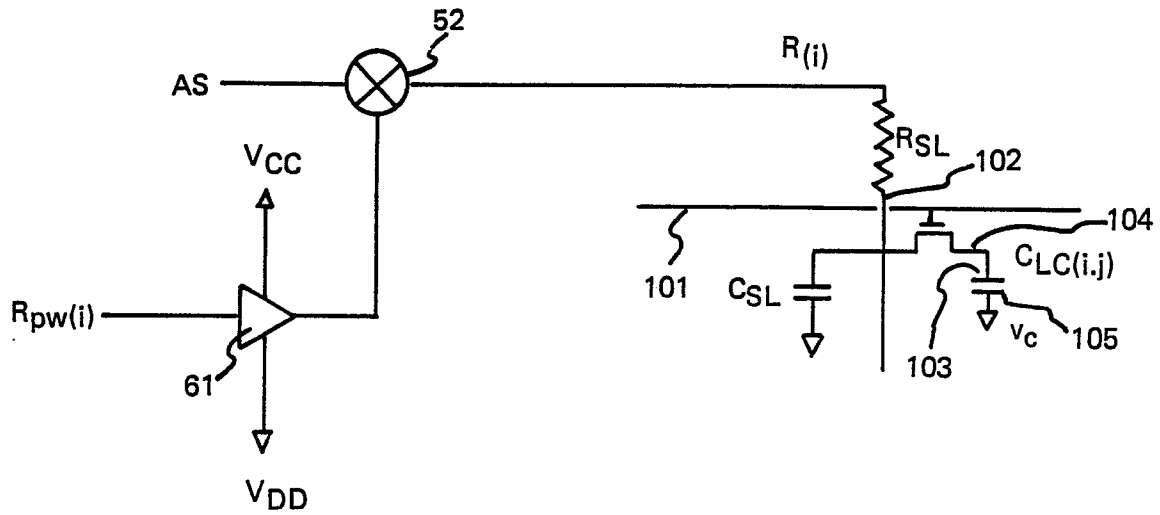
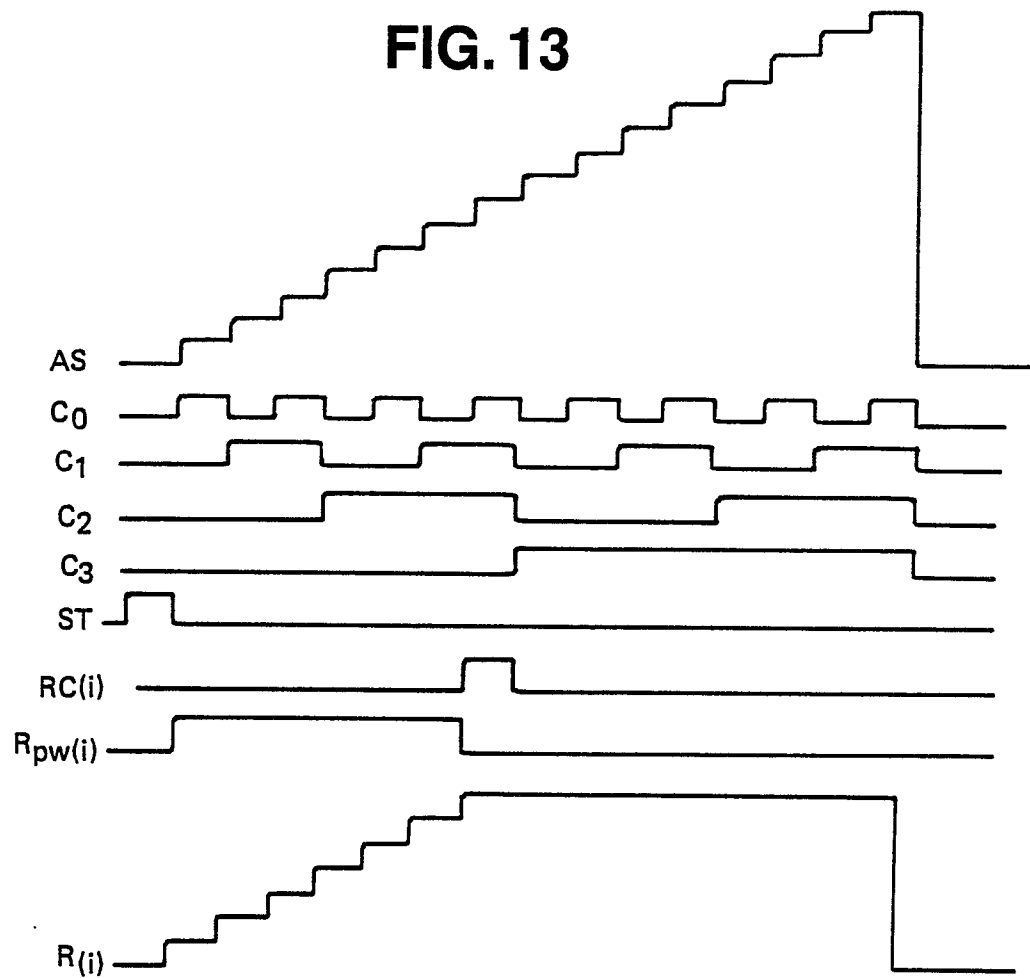


FIG. 11

FIG. 12**FIG. 13**

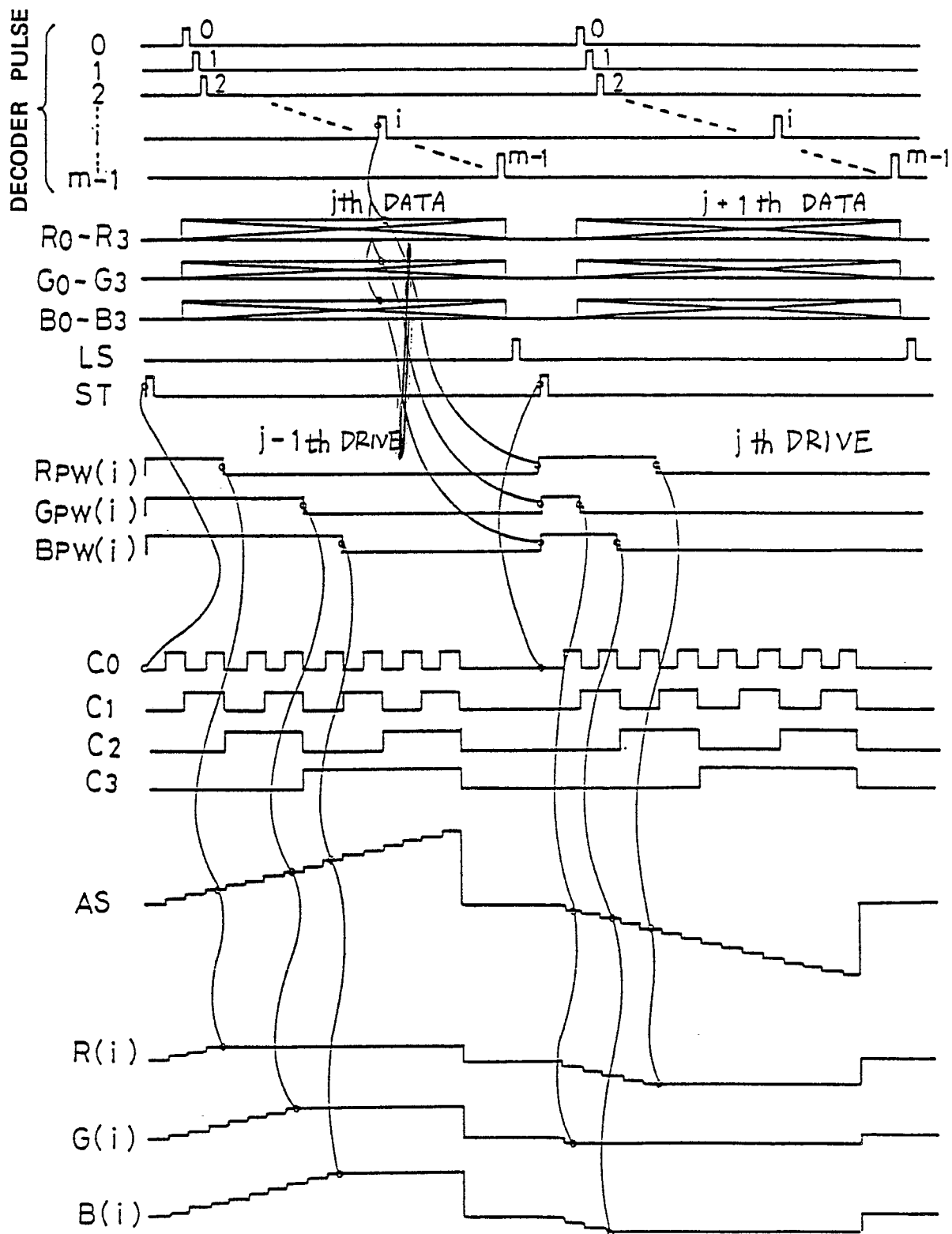


FIG. 14

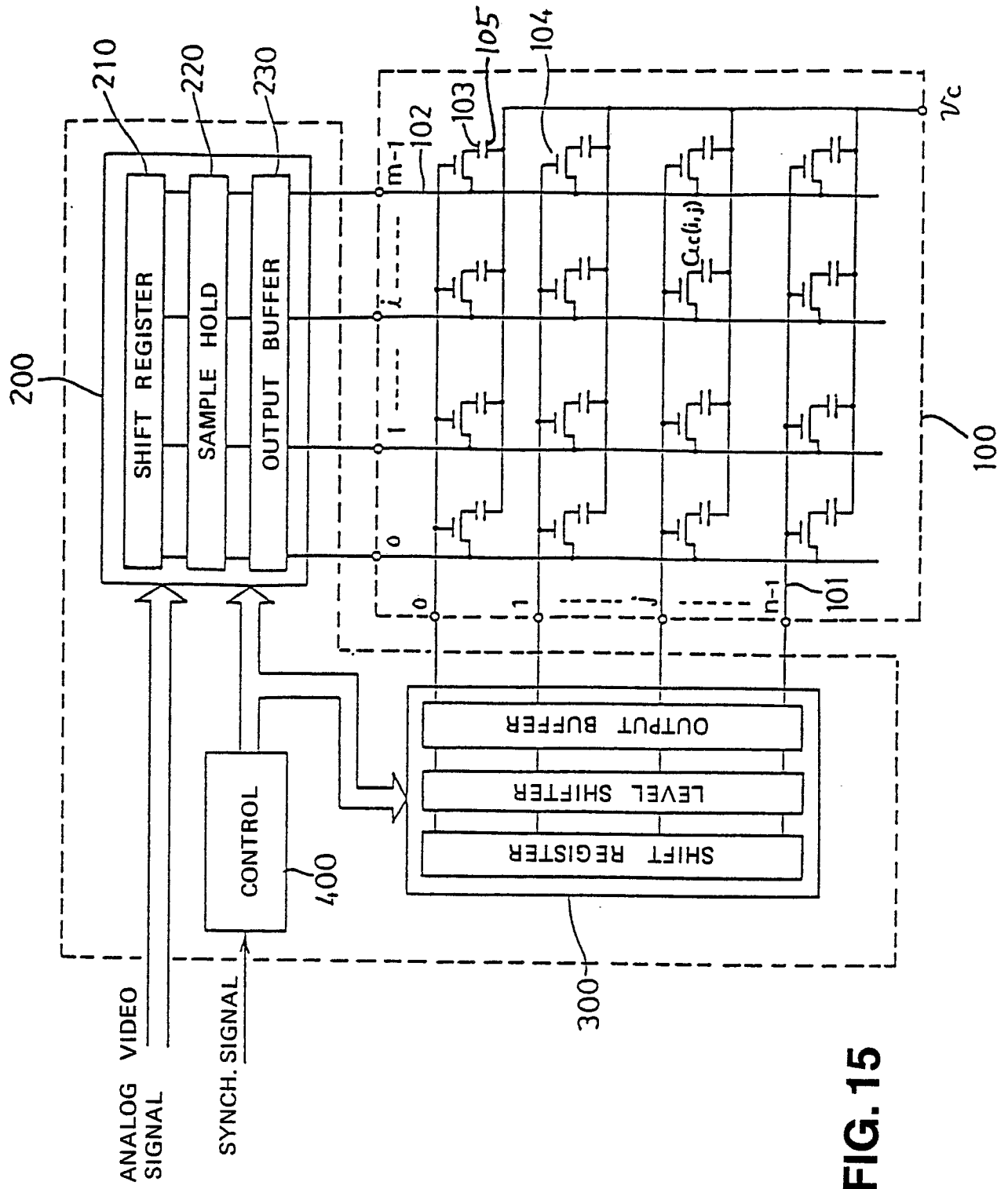
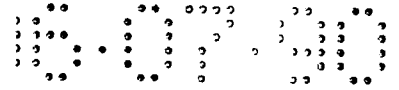




FIG. 16

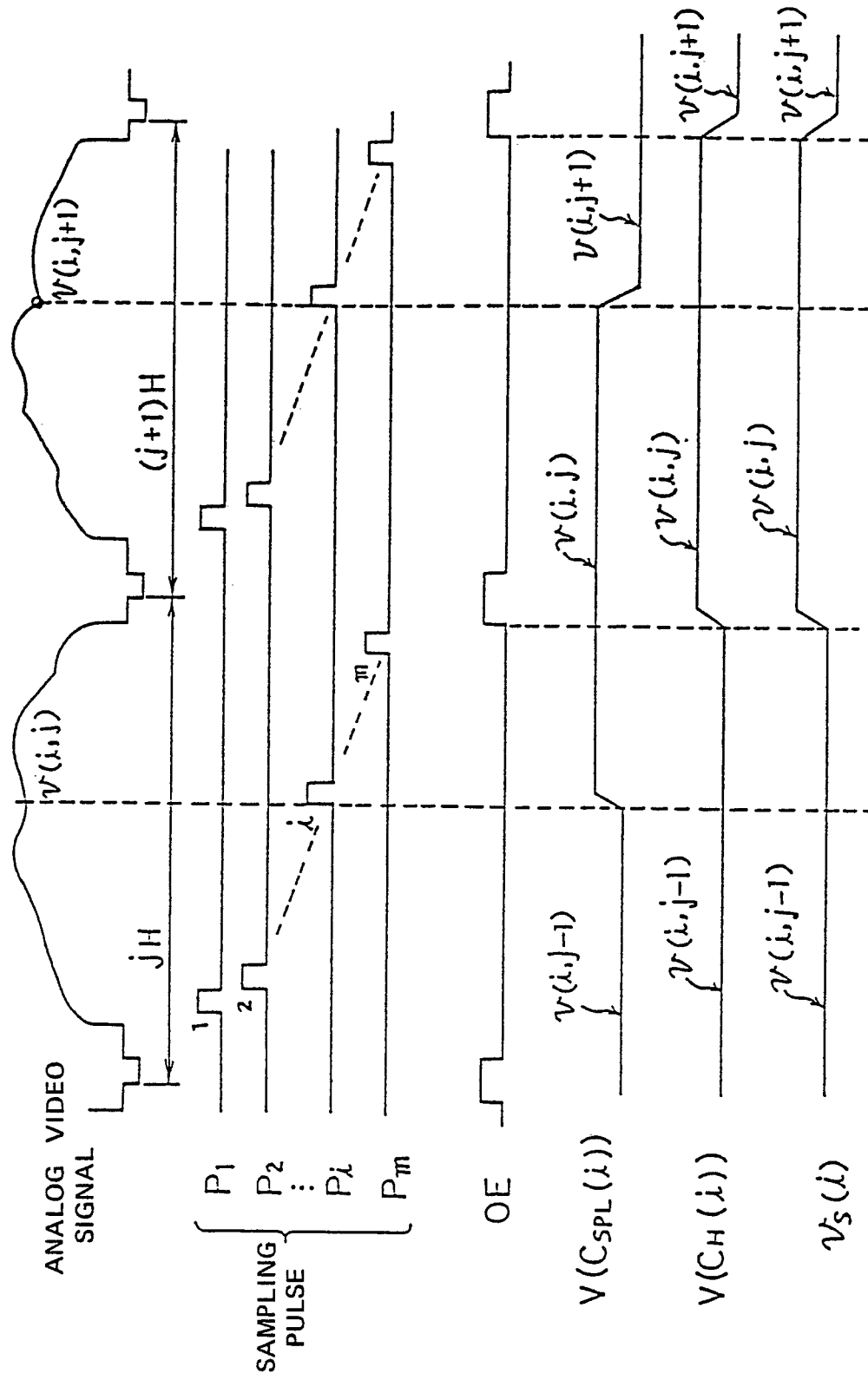


FIG. 17