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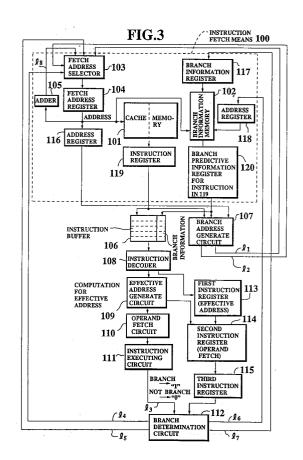
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- Branch instruction control unit based on a pipeline method.
- 57) Disclosed is a branch instruction control unit based on a pipeline method comprising cache memory means(101), branch information means(102), branch address generation means(107), fetch means(100), instruction decode means(108), and instruction executing means(111). In the unit, when the branch instructions are fetched, the branch is predicted in accordance with the branch predictive information in the branch information memory(102). Then, when establishment of the branch is judged, the target addresses are calculated by the branch address generation means 107) before decoding of the branch instructions, and the instructions designated by the target addresses are fetched from the cache memory means(101) to carry out a series of the pipeline processes.





EUROPEAN SEARCH REPORT

EP 90 10 6292

Category	Citation of document with in of relevant pas		Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
P,X	EP-A-0 320 098 (INTERNA 14 June 1989 * page 2, line 24 - line * page 3, line 26 - line * page 4, line 20 - page * page 5, line 55 - page	e 39 * e 5, line 29 *	1-7	G06F9/38
Y	PATENT ABSTRACTS OF JAPA vol. 7, no. 130 (P-202) & JP-A-58 048 144 (NIPP March 1983 * abstract *	7 June 1983	1-7	
Y	THE 8TH ANNUAL SYMPOSIUM ARCHITECTURE May 1981, MINNEAPOLIS, I pages 135 - 148; J. E. SMITH: 'A Study o Strategies' * page 139, left column	MINNESOTA, US f Branch Prediction	1-7	
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