(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 397 079 A3**

(12) **EUROPEAN PATENT APPLICATION**

(21) Application number: **90108555.5**

(51) Int. Cl.5: **H04L 25/49**

(22) Date of filing: **07.05.90**

(30) Priority: **12.05.89 US 351175**

(43) Date of publication of application:
14.11.90 Bulletin 90/46

(84) Designated Contracting States:
AT BE CH DE ES FR GB IT LI NL SE

(88) Date of deferred publication of the search report:
10.06.92 Bulletin 92/24

(71) Applicant: **ALCATEL N.V.**
Strawinskylaan 537 (World Trade Center)
NL-1077 XX Amsterdam(NL)

(72) Inventor: **Powell, William Edward**
201 Trotters Ridge Drive
Raleigh NC 27614(US)
Inventor: **Weeber, William Bernard**
7917 Blaney Franks Road
Apex NC 27502(US)
Inventor: **Roger, George André Charles**
Pavillon Marguerite, Parc de Lormoy
F-91240 Saint Michel Sur Orge(FR)

(74) Representative: **Weinmiller, Jürgen et al**
Lennéstrasse 9 Postfach 24
W-8133 Feldafing(DE)

(54) **Parallel pseudo-random generator for emulating a serial pseudo-random generator and method for carrying out same.**

(57) A parallel pseudo-random generator for emulating a serial pseudo-random generator that generates serial outputs such that the next serial output value is based upon an Exclusive OR combination of at least two preceding serial output values the maximum preceding serial output value defined as the Pth preceeding serial output value, where P is an integer greater than one; comprising:

A) at least P latches, each latch having an output having a logic value 1 or 0 and an input operable upon receipt of a clock signal, for receipt of data for controlling the next logic value on the latch output;

B) at least P Exclusive OR gates, each having at least two inputs and one output, each Exclusive OR gate output connected to a corresponding input of one latch so as to define the next value of the latch output upon receipt of the next clock signal; and

C) means for connecting each input of each Exclusive OR gate to one latch output so that the output of each Exclusive OR gate represents the corresponding next value of the latch to which This Exclusive Or gate output is connected.

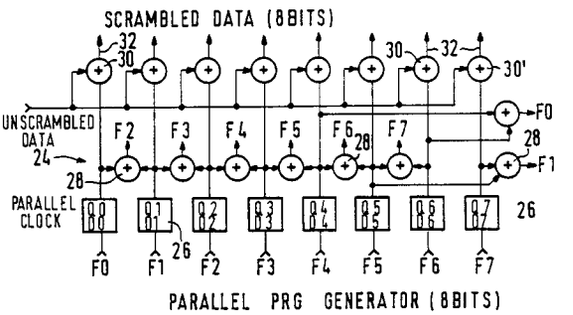

Fig. 2

EP 0 397 079 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 10 8555

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	ELEKTRONIK, vol. 32, no. 26, December 1983, pages 67-70; T. HERMES et al.: "Parallel arbeitende Scrambler, Descrambler und Zufallsfolgen-Generatoren" * Page 68, paragraph 3; page 69, paragraph 4; figure 5 * ---	1-4	H 04 L 25/49
T	THE RADIO AND ELECTRONIC ENGINEER, vol. 45, no. 4, April 1975, pages 171-176; J.J. O'REILLY: "Series-parallel generation of m-sequences" * Whole document * ---	1-4	
E	US-A-4 965 881 (DILLEY) * Whole document * -----	1-4	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H 04 L
H 03 K

The present search report has heen drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	17-03-1992	GRIES T.M.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in tbe application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P0401)